

# User Manual

**APM32F425xG\_F427xG**

**Arm® Cortex®-M4F based 32-bit MCU**

**Version: V1.0**

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# 1 Introduction and Document Description Rules

## 1.1 Introduction

This user manual provides application developers with all the information about how to use MCU (micro-controller) system architecture, memory and peripherals.

For information about Arm® Cortex®-M4F core, refer to *Arm® Cortex® -M4F Technical Reference Manual*. For detailed data such as model information, dimension and electrical characteristics of the device, refer to the corresponding datasheet. For memory mapping and peripherals of all MCU series models, refer to the corresponding datasheet.

It is hereby declared that Geehy Semiconductor Co., Ltd., hereinafter refer to as "Geehy".

## 1.2 Document description rules

### 1.2.1 "Register functional description" rules

- (1) Control (CTRL) registers are all "set to 1 and cleared to 0 by software", unless otherwise specified.
- (2) The control registers are usually followed by verb abbreviations to make a distinction. The verbs can be: EN-Enable, CFG-Configure, D-Disable, SET-Setup and SEL-Select
- (3) The state register abbreviation is usually followed by FLG to make a difference.
- (4) The value and data registers usually include V, VALUE, D and DATA, which are not followed by verbs, such as: xxPSC and CNT.

### 1.2.2 Full name and abbreviation description of terms

Table 1 Abbreviation and Description of R/W Modes

| R/W mode           | Description                                                                                                            | Abbreviation |
|--------------------|------------------------------------------------------------------------------------------------------------------------|--------------|
| read/write         | Software can read and write this bit.                                                                                  | R/W          |
| read-only          | Software can only read this bit.                                                                                       | R            |
| write-only         | Software can only write this bit, and after reading this bit, the reset value will be returned.                        | W            |
| read/clear         | The software can read this bit and clear it by writing 1.<br>Writing 0 has no effect on this bit.                      | RC_W1        |
| read/clear         | The software can read this bit and clear it by writing 0.<br>Writing 1 has no effect on this bit.                      | RC_W0        |
| read/clear by read | The software can read this bit and reading this bit will automatically clear it to 0, and writing this bit is invalid. | RC_R         |

| R/W mode                | Description                                                                                                        | Abbreviation |
|-------------------------|--------------------------------------------------------------------------------------------------------------------|--------------|
| read/set                | The software can read and set this bit, and writing 0 has no effect on this bit.                                   | R/S          |
| read-only write trigger | The software can read this bit and writing 0 or 1 can trigger an event but has no effect on the value of this bit. | RT_W         |
| toggle                  | The software can flip this bit only by writing 1 and writing 0 has no effect on this bit.                          | T            |

Table 2 Functional Description and Full Name and Abbreviation of Terms of Commonly Used Registers

| Full name in English | English abbreviation |
|----------------------|----------------------|
| Enable               | EN                   |
| Disable              | D                    |
| Clear                | CLR                  |
| Select               | SEL                  |
| Configure            | CFG                  |
| Contrl               | CTRL                 |
| Controller           | C                    |
| Reset                | RST                  |
| Stop                 | STOP                 |
| Set                  | SET                  |
| Load                 | LD                   |
| Calibration          | CAL                  |
| Initialize           | INIT                 |
| Error                | ERR                  |
| Status               | STS                  |
| Ready                | RDY                  |
| Software             | SW                   |
| Hardware             | HW                   |
| Source               | SRC                  |
| System               | SYS                  |
| Peripheral           | PER                  |
| Address              | ADDR                 |
| Direction            | DIR                  |
| Clock                | CLK                  |
| Input                | I                    |

| Full name in English | English abbreviation |
|----------------------|----------------------|
| Output               | O                    |
| Interrupt            | INT                  |
| Data                 | DATA                 |
| Size                 | SIZE                 |
| Divider              | DIV                  |
| Prescaler            | PSC                  |
| Multiplier           | MUL                  |
| Period               | PRD                  |

Table 3 Full Name and Abbreviation of Modules

| Full name in English                                    | English abbreviation |
|---------------------------------------------------------|----------------------|
| External Memory Controller                              | EMMC                 |
| Static Memory Controller                                | SMC                  |
| Dynamic memory Controller                               | DMC                  |
| Reset and Clock Management Unit                         | RCM                  |
| Power Management Unit                                   | PMU                  |
| Backup Register                                         | BAKPR                |
| Nested Vector Interrupt Controller                      | NVIC                 |
| External Interrupt /Event Controller                    | EINT                 |
| Direct Memory Access                                    | DMA                  |
| Debug MCU                                               | DBG MCU              |
| General-Purpose Input Output Pin                        | GPIO                 |
| Alternate Function Input Output Pin                     | AFIO                 |
| Timer                                                   | TMR                  |
| Watchdog Timer                                          | WDT                  |
| Independent Watchdog Timer                              | IWDT                 |
| Windows Watchdog Timer                                  | WWDT                 |
| Real-Time Clock                                         | RTC                  |
| Universal Synchronous Asynchronous Receiver Transmitter | USART                |
| Inter-Integrated Circuit Interface                      | I2C                  |
| Serial Peripheral Interface                             | SPI                  |
| Inter-IC Sound Interface                                | I2S                  |
| Quad Serial Peripheral Interface                        | QSPI                 |

| Full name in English                     | English abbreviation |
|------------------------------------------|----------------------|
| Controller Area Network                  | CAN                  |
| Secure Digital Input and Output          | SDIO                 |
| Universal Serial Bus Full-Speed Device   | USB                  |
| Analog-to-Digital Converter              | ADC                  |
| Digital-to-Analog Converter              | DAC                  |
| Cyclic Redundancy Check Calculation Unit | CRC                  |
| Float Point Unit                         | FPU                  |



## 2 System Architecture

### 2.1 Full name and abbreviation description of terms

Table 4 Full name and abbreviation description of terms

| Full name in English          | English abbreviation |
|-------------------------------|----------------------|
| Advanced High-Performance Bus | AHB                  |
| Advanced Peripheral Bus       | APB                  |
| Core Couple Memory            | CCM                  |

### 2.2 System architecture block diagram

Arm® Cortex®-M4F core in the product has FPU, while the FPU of other series of products (unless otherwise specified) is out of the core.

The system mainly consists of eight master modules and seven slave modules.

The master modules are I-bus, D-bus and S-bus of Arm® Cortex®-M4F core with FPU, general-purpose DMA1, general-purpose DMA2, and DMA2 peripheral bus, Ethernet DMA bus and USB OTG bus.

The slave modules are internal Flash I-bus, D-bus, main internal memory SRAM1, auxiliary internal memory SRAM2 and SRAM3, all peripheral devices connected via the AHB1 bus and AHB1/APB bridge, peripherals on the AHB2 bus, and QSPI and EMMC on the AHB3 bus.

The bus matrix provides a platform to support the master module to access the slave module. The matrix can achieve concurrent access, and the CPU still has efficient processing capacity when multiple peripherals are running at high speed. It also has a 64-bit core couple memory which can be accessed only through CPU.

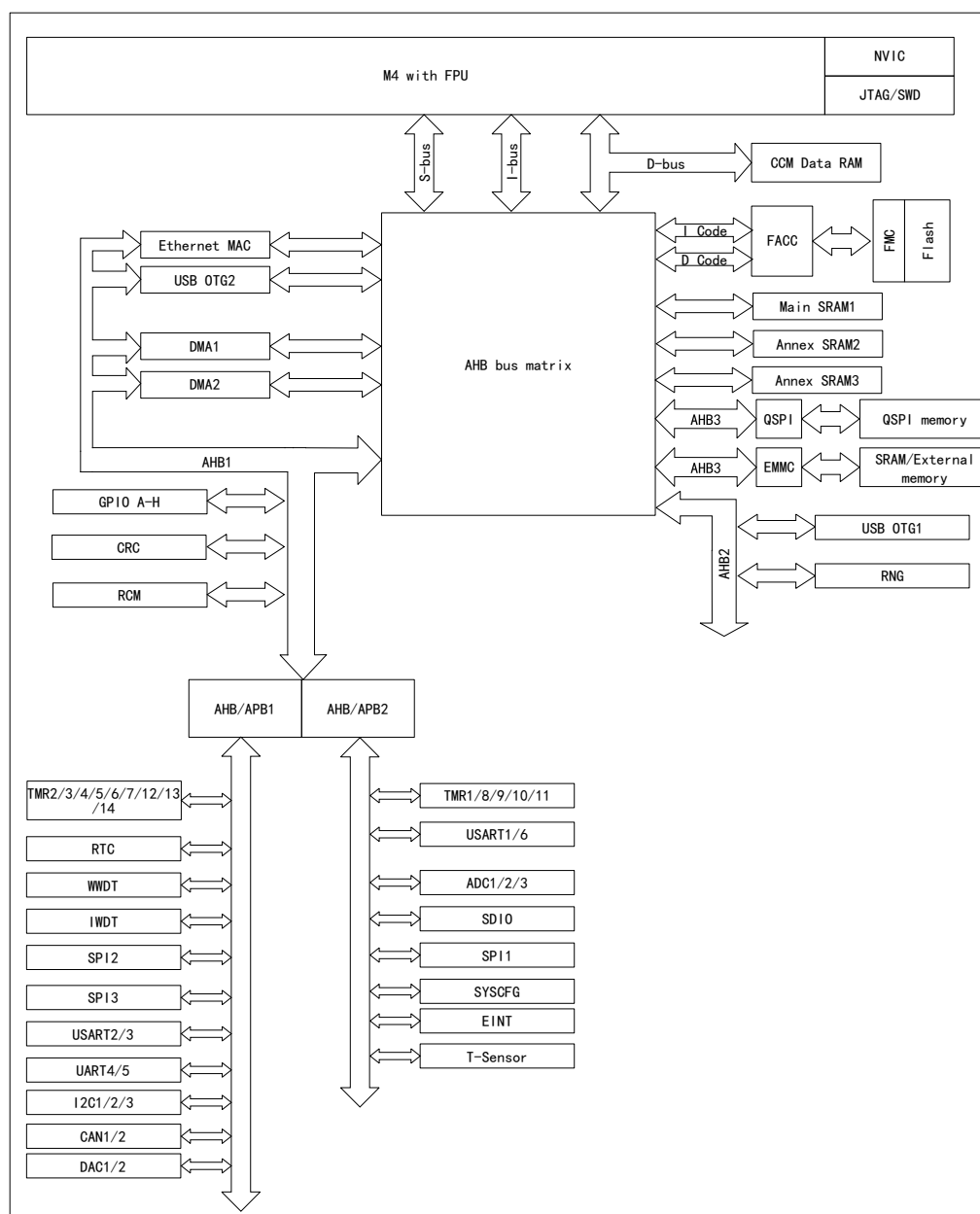
The name and description of the bus are shown in the following table.

Table 5 Bus Name

| Name           | Description                                                                                                                  |
|----------------|------------------------------------------------------------------------------------------------------------------------------|
| I-bus          | Connect the instruction bus of Arm® Cortex® -M4F core and the bus matrix.<br>Used for obtaining instructions.                |
| D-bus          | Connect the data bus of Arm® Cortex® -M4F core and the bus matrix.<br>Used for text loading and debugging access.            |
| S-bus          | Connect the system bus of Arm® Cortex® -M4F core and the bus matrix.<br>Used for accessing the data in peripherals and SRAM. |
| DMA memory bus | Connect the main interface of DMA memory and the bus matrix.<br>Achieve transmission related to the memory through DMA.      |

| Name               | Description                                                                                                                                                                      |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DMA peripheral bus | Connect the main interface of DMA peripherals and the bus matrix.<br>It can not only achieve DMA access to the peripherals on AHB, but also enable data transfer among memories. |
| Ethernet DMA bus   | Connect the main interface of Ethernet DMA and the bus matrix.<br>The data are loaded/stored in the memory through Ethernet DMA.                                                 |
| Bus matrix         | Coordinate the access among modules, and roll polling algorithm is used during arbitration.                                                                                      |
| AHB/APB bridge     | The bridge provides synchronous connection between AHB and APB buses.<br>When accessing APB registers with non-32-bit data, it will be automatically converted to 32-bit.        |

Figure 1 APM32F425xG\_F427xG System Architecture Block Diagram



## 2.3 Memory mapping

The assigned addresses of memory mapping include the core (including core peripherals), on-chip Flash (including main memory area, system memory area and option bytes), on-chip SRAM, and bus peripherals (including AHB and APB peripherals). For specific information of various addresses, refer to the data manual of the corresponding model.

### 2.3.1 Embedded SRAM

The APM32F425 product includes backup SRAM (4KB) and system SRAM (192KB). The system SRAM is divided into three blocks: SRAM1 (112KB), SRAM2 (16KB), and CCM (64KB).

The APM32F427 product includes backup SRAM (4KB) and system SRAM (448KB). The system SRAM is divided into four blocks: SRAM1 (112KB), SRAM2 (16KB), SRAM3 (256KB), and CCM (64KB).

#### SRAM1, SRAM2 and SRAM3

The main SRAM1, auxiliary SRAM2, auxiliary SRAM3 can be accessed by byte, half word (16 bits) or full word (32 bits). The mapping address of SRAM1, SRAM2, and SRAM3 is 0x2000 xxxx, which can be accessed by all AHB master modules.

#### Core couple memory (CCM)

The mapping address of CCM (64KB) is 0x1000 0000, and it can only be accessed by CPU through D-bus.

### 2.3.2 Bit band

Arm® Cortex®-M4F memory is mapped with two bit-band areas, and it maps each word in the alias memory area to one bit in the bit-band memory. Write a word to the alias memory and there will be the same effect as the read-change-write operation on the target of the bit-band area. Both peripheral register and SRAM are mapped into a bit band area, and it is allowed to perform single bit-band write and read operations.

The following gives a mapping formula:

$$\text{bit\_word\_addr} = \text{bit\_band\_base} + (\text{byte\_offset} \times 32) + (\text{bit\_number} \times 4)$$

## 2.4 Startup configuration

APM32F425xG\_F427xG series MCU achieve a special mechanism. By configuring the BOOT[1:0] pin, there are three different startup modes, and the system can not only start from Flash memory or system memory, but also start

from the built-in SRAM. The memory selected as the start zone is determined by the selected startup mode.

Table 6 Startup Mode Configuration and Access Mode

| Startup mode configuration |           | Startup mode              | Access mode                                                                                                                                                                                   |
|----------------------------|-----------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BOOT1 pin                  | BOOT0 pin |                           |                                                                                                                                                                                               |
| X                          | 0         | Main flash memory (Flash) | The main flash memory is mapped to the boot space, but it can still be accessed at its original address. It means that the contents of the flash memory can be accessed in two address areas. |
| 0                          | 1         | System memory             | The system memory is mapped to the boot space (0x0000 0000), but it can still be accessed at its original address.                                                                            |
| 1                          | 1         | Built-in SRAM             | SRAM can be accessed only at the starting address.                                                                                                                                            |

Note:

- (1) The boot space address is 0x0000 0000.
- (2) The original address of Flash is 0x0800 0000.
- (3) The original address of the system memory is 0x1FFF 0000.
- (4) The starting address of SRAM is 0x2000 0000.
- (5) The user can select the startup mode after reset by setting the state of BOOT[1:0] pin.
- (6) BOOT pin should keep the user's required startup configuration in standby mode. When exiting from the standby mode, the value of boot pin will be latched.
- (7) If you choose to start from built-in SRAM, you must use NVIC's exception table and offset register to remap the vector table to SRAM when writing the application code.

### Physical remapping

After BOOT pin is selected, MMSEL bit of SYSCFG\_MMSEL register can be modified through software program to configure some registers to allow access from I-Code bus. See SYSCFG register for specific configuration.

### Embedded BootLoader

The embedded BootLoader mode will be selected to reprogram Flash through one of the following serial ports:

- USART1
- USART3
- CAN2
- USB OTG\_FS slave mode

## 3 FLASH Memory

### 3.1 Full name and abbreviation description of terms

Table 7 Full name and abbreviation description of terms

| Full name in English    | English abbreviation |
|-------------------------|----------------------|
| Flash Memory Controller | FMC                  |
| One-time Programmable   | OTP                  |
| Flash Accelerator       | FACC                 |

### 3.2 Introduction

This chapter mainly introduces the storage structure, read, erase, write, read/write protection, unlock/lock characteristics of Flash, and the involved register functional description.

### 3.3 Main characteristics

- (1) Flash memory structure:
  - Contain main memory area and information block
  - The capacity of main memory area is up to 1MB
  - The information block is divided into system memory, OTP area and option byte three areas
  - The capacity of the system memory area is 30KB, for storing BootLoader program
  - 96-bit unique UID, and main memory area capacity information are stored in the information block
  - The OTP area is 528Bytes, in which 512 OTP bytes are used for storing user data, and the remaining 16 bytes are used for locking the corresponding OTP data block
  - The capacity of the option byte area is 16Bytes
- (2) Functional Description:
  - Operate the Flash:
    - Read
    - Sector/Mass Erase
    - Write
    - Read/Write protection
  - Operate the option byte:
    - Read
    - Erase
    - Write

- Read/Write protection

## 3.4 Flash memory structure

Table 8 Flash Memory Structure

| Block             | Name                | Address range             | Size (byte) | Sector    |
|-------------------|---------------------|---------------------------|-------------|-----------|
| Main memory block |                     | 0x0800 0000–0x0800 3FFF   | 16K         | Sector 0  |
|                   |                     | 0x0800 4000–0x0800 7FFF   | 16K         | Sector 1  |
|                   |                     | 0x0800 8000–0x0800 BFFF   | 16K         | Sector 2  |
|                   |                     | 0x0800 C000–0x0800 FFFF   | 16K         | Sector 3  |
|                   |                     | 0x0801 0000 – 0x0801 FFFF | 64K         | Sector 4  |
|                   |                     | 0x0802 0000 – 0x0803 FFFF | 128K        | Sector 5  |
|                   |                     | ...                       | ...         | ...       |
|                   |                     | 0x080E 0000–0x080F FFFF   | 128K        | Sector 11 |
| Information block | System memory (ROM) | 0x1FFF 0000–0x1FFF 77FF   | 30K         | -         |
|                   | OTP area            | 0x1FFF 7800–0x1FFF 7A0F   | 528         | -         |
|                   | Option byte         | 0x1FFF C000–0x1FFF C00F   | 16          | -         |

## 3.5 Flash memory functional description

### 3.5.1 Read Flash

The reading speed of Flash is affected by the number of wait cycles, and the number of wait cycles is affected by HCLK. Assuming the wait cycle is n, and the rising base of HCLK range is X.

- When  $(n+1) X$  is less than the maximum value:  
 $nX < HCLK \leq (n+1) X$
- When  $(n-1) X$  is greater than the maximum value:  
 $nX < HCLK \leq \text{maximum value}$

Table 9 X Affected by Voltage Range and Maximum Value of HCLK

| Voltage range | 1.8V-2.1V | 2.1V-2.4V | 2.4V-2.7V | 2.7V-3.6V |
|---------------|-----------|-----------|-----------|-----------|
| X             | 20MHz     | 22MHz     | 24MHz     | 30MHz     |
| Maximum value | 160MHz    | 240MHz    | 240MHz    | 240MHz    |

Note: When VOSSEL=0 is set in the PMU\_CTRL register, the maximum HCLK frequency is 144MHz; when VOSSEL=1 is set, the maximum HCLK frequency is 240MHz.

CPU frequency can be adjusted by selecting different wait cycles, so as to adjust the reading speed of Flash.

### 3.5.1.1 Flash accelerator (FACC)

FACC accelerator can improve the execution speed of Flash, so that the Flash can execute programs with fewer wait cycles at high CPU frequency.

#### Prefetch buffer area

When accessing Flash requires inserting wait cycles, the next instruction line of the Flash can be pre-loaded through the I-Code bus to improve access speed.

#### I-cache

I-cache is an instruction buffer memory. The instructions in I-cache can be obtained without delay. The system can store 64 lines of 128-bit instructions in I-cache and the I-cache function can be enabled through ICACHEEN bit of FMC\_ACCTRL register.

#### D-cache

D-cache is a data buffer memory. The system accesses the data buffer area of Flash through D-Bus to reduce the waiting time. Access of D-bus is prior to I-bus. The system can store 8 lines of 128-bit instructions in D-cache and the D-cache function can be enabled through DCACHEEN bit of FMC\_ACCTRL register.

### 3.5.2 Main memory block

When erasing/writing to the main memory, Flash can no longer be read.

#### Number of parallel bits

The parallel bits refers to the number of bytes processed during Flash erase/write operations and is configured by programming the PGSIZE bits in the FMC\_CTRL register. The determinant factors and the parallel bits are shown in the table below:

Table 10 Relationship between Determinant Factors and Number of Parallel Bits

| Voltage range (V)       | 1.8-2.1 | 2.1-2.4 | 2.4-2.7 | 2.7-3.6 | 2.7-3.6 (external VPP is used) |
|-------------------------|---------|---------|---------|---------|--------------------------------|
| Number of parallel bits | 8-bit   | 16-bit  |         | 32-bit  | 64-bit                         |

#### 3.5.2.1 Erase main memory block

Flash can support sector erase and mass erase (erase all). Mass erase does not affect OTP sector or configuration sector.

#### Main memory page erase

Page erase is an independent erase according to the main memory area page

selected by the program, which will not have any impact on the page not selected for erasure.

After the correct page erase (or flash write operation) is completed, OPRCMP bit of FMC\_STS register will be set. If OPCINTEN interrupt is enabled, an operation completion interrupt will be triggered. Users need to note that the page to be erased must be a valid page (the valid address of the main memory area and the address not protected by write).

### **Main memory mass erase**

The mass erase operation will erase all the contents in the main storage area of Flash, so the users need to pay special attention when using it to avoid the loss of important data caused by misoperation.

Mass erase does not affect OTP sector or configuration sector.

#### **3.5.2.2 Write main memory block**

Flash supports byte, half-word, word, and double-word write operation, specifically depending on the number of parallel bits.

Note: It is important to check whether the destination address has been erased before writing to ensure correct writing. Flash unit must be erased into 1 before writing.

If the destination address has write protection, the written data is invalid and a write protection error will be triggered (WPROTERR bit of FMC\_STS register is set to "1").

In FMC\_STS register, there are three write error bits, which are PGALGERR (programming alignment error), PGPRLERR (programming parallelism error) and PGSEQERR (programming sequence error).

#### **Programming alignment error**

To program more than 128-bit lines of data to the Flash, a programming alignment error will occur, and the PGALGERR bit will be set to 1.

#### **Programming parallelism error**

If the width of the write operation is inconsistent with the number of parallel bits, the write operation will be suspended. A programming parallelism error will be generated, and the PGPRLERR bit will be set to 1.

#### **Programming sequence error**

The correct programming sequence is:

- (1) Ensure that no Flash operations are being performed currently through FMC\_STS[BUSY].



- (2) Set FMC\_CTRL[PG] to 1.
- (3) Perform write operation.
- (4) Operation is completed, waiting for BUSY bit to be cleared to zero.

If the programming sequence is wrong, a programming sequence error will occur, and the PGSEQERR bit will be set to 1.

### 3.5.2.3 Lock/unlock

FMC\_CTRL[LOCK] can only be set to 1, so as to lock Flash control register, and the main memory block area can not be programmed.

Write the keywords 0x4567 0123 and 0xCDEF 89AB to the FMC\_KEY register, and when the system detects unlocking sequence, it will clear the LOCK bit of FMC\_CTRL register to zero, then Flash control register and the main memory block will be unlocked.

### 3.5.2.4 Buffer

If the write operation of Flash involves some data in D-cache, the data in Flash and D-cache will be modified.

If the erase operation of Flash involves the data in D-cache or I-cache, the data shall be written to the cache beforehand, and the cache should be reset after the operation.

### 3.5.2.5 Interrupt

An interrupt will occur in case of any of the following events:

- End of operation: End of erase/write operation
- Write protection error: Perform erase/write operation for the write protection area
- Programming error: An error occurs during erase/write/read

When OPCINTEN bit or ERRINTEN bit in FMC\_CTRL register is set to 1 and the corresponding interrupt event occurs, an interrupt will be generated.

## 3.5.3 Option byte

The address and composition of the option byte are shown in the following table, and the specific meaning description can be seen in the corresponding bit of FMC\_OPTCTRL register.

Table 11 Instructions for Option Bytes

| Address     | Bit field | Option byte | Functional description |
|-------------|-----------|-------------|------------------------|
| 0x1FFF C000 | 1:0       | -           | -                      |
|             | 3:2       | BORLVL      | Brownout reset level   |
|             | 4         | -           | -                      |

| Address     | Bit field | Option byte | Functional description                      |
|-------------|-----------|-------------|---------------------------------------------|
|             | 5         | WDTSEL      | Select the watchdog                         |
|             | 6         | RSTSTOP     | Reset occurs when entering the stop mode    |
|             | 7         | RSTSTDB     | Reset occurs when entering the standby mode |
|             | 15:8      | RPROT       | Read protection                             |
| 0x1FFF C008 | 11:0      | NWPROT      | No write protection                         |
|             | 15:12     | -           | -                                           |

### 3.5.3.1 Erase/write option byte

The option byte must be unlocked before erasing/writing.

The programming sequence of option byte is:

- (1) Ensure that no Flash operations are being performed currently through FMC\_STS[BUSY].
- (2) Write the programming value to FMC\_OPTCTRL.
- (3) Set FMC\_OPTCTRL[OPTSTART] to 1.
- (4) Operation is completed, waiting for BUSY bit to be cleared to zero.

### 3.5.3.2 Lock/unlock

FMC\_OPTCTRL[OPTLOCK] can only be set to 1, so as to lock the option byte area.

Sequentially write the keywords 0x0819 2A3B and 0x4C5D 6E7F to the FMC\_OPTKEY register, and when the system detects unlocking sequence, it will clear the OPTLOCK bit of FMC\_OPTCTRL register to zero and the option byte will be unlocked.

### 3.5.4 Write protection

In order to prevent accidental rewriting of Flash due to program disorder, in default state, the Flash supports write protection function of up to 12 user sectors. When the corresponding bit of the FMC\_OPTCTRL[NWPROT] bit field is at low level, the corresponding sector will be write-protected, and the sector cannot be erased/written.

#### 3.5.4.1 Write protection error

FMC\_STS[WPROTERR] is a write protection error bit, and it will be set to 1 when any of the following events occurs:

- Perform erase/write operation for the write protection area
- Execute page erase/mass erase for invalid sector
- Flash is under read protection but detects erase/write request

- Perform write operation for the locked OTP area

### 3.5.5 Read protection

In order to prevent untrusted code from reading Flash data, you can choose to use the read protection function for the Flash. The read protection level can be selected by configuring the value of the FMC\_OPTCTRL[RPROT] bit field. The read protection has three levels, which are Level 0, Level 1 and Level 2.

The access restriction at different read protection levels is shown in the following table.

Table 12 Restrictions at Different Read Levels

| Storage area          | Level   | Bootstrap from Flash |       |       | Debugging function, bootstrap from RAM or system memory |       |                  |
|-----------------------|---------|----------------------|-------|-------|---------------------------------------------------------|-------|------------------|
|                       |         | Read                 | Write | Erase | Read                                                    | Write | Erase            |
| OTP                   | Level 1 | √                    |       | -     | ×                                                       |       | -                |
|                       | Level 2 |                      |       |       |                                                         |       |                  |
| Option byte           | Level 1 | √                    |       |       |                                                         |       |                  |
|                       | Level 2 | ×                    |       |       |                                                         |       |                  |
| Flash and backup SRAM | Level 1 | √                    |       |       | ×                                                       |       | x <sup>(1)</sup> |
|                       | Level 2 |                      |       |       | ×                                                       |       |                  |

Note:

(1) means that only when Level 1 changes to Level 0, can the data of Flash and backup SRAM be erased.

(2) "√" means the operation is allowed, "×" means not allowed, and "-" means undefined.

#### 3.5.5.1 Level 0

When FMC\_OPTCTRL[RPROT]=0xAA, the read protection function is not used for Flash.

#### 3.5.5.2 Level 1

When FMC\_OPTCTRL[RPROT]=any value (except 0xAA and 0xCC), the read protection level is 1. At this time, if the level is adjusted to Level 0, mass erase operation will be performed to erase all data of Flash and backup SRAM. Mass erase only affects user code area. Other option bytes and OTP that are write-protected will not be affected.

#### 3.5.5.3 Level 2

When FMC\_OPTCTRL[RPROT]=0xCC, the read protection level is 2. Under this condition:

- Reserve the read protection function of Level 1

- It is not allowed to bootstrap from RAM or system memory
- JTAG, SWV, ETM and boundary scan is disabled
- The option byte is locked

Note: When the read protection level is set to 2, it cannot be degraded any more.

### 3.5.6 OTP

The following table shows OTP structure.

Table 13 OTP Structure

| Address     | [31:0] | [63:32] | [95:64] | [127:96] | Block         |
|-------------|--------|---------|---------|----------|---------------|
| 0x1FFF 7800 | OTP0   | OTP0    | OTP0    | OTP0     | Data block 0  |
| 0x1FFF 7810 | OTP0   | OTP0    | OTP0    | OTP0     |               |
| 0x1FFF 7820 | OTP1   | OTP1    | OTP1    | OTP1     | Data block 1  |
| 0x1FFF 7830 | OTP1   | OTP1    | OTP1    | OTP1     |               |
| 0x1FFF 7840 | OTP2   | OTP2    | OTP2    | OTP2     | Data block 2  |
| 0x1FFF 7850 | OTP2   | OTP2    | OTP2    | OTP2     |               |
| .....       | .....  |         |         |          | .....         |
| 0x1FFF 79E0 | OTP15  | OTP15   | OTP15   | OTP15    | Data block 15 |
| 0x1FFF 79F0 | OTP15  | OTP15   | OTP15   | OTP15    |               |
| 0x1FFF 7A00 | LOCKB0 | LOCKB4  | LOCKB8  | LOCKB12  | Lock block    |
|             | ...    | ...     | ...     | ...      |               |
|             | LOCKB3 | LOCKB7  | LOCKB11 | LOCKB15  |               |

OTP consists of 16 32-byte data blocks and 1 16-byte lock block. The lock block n is used to lock the data block n (n=0...15), and the data block of each OTP is programmable unless the corresponding lock block has a value of 0x00. The value of the lock block can only be 0x00 or 0xFF; otherwise, the OTP byte cannot be used normally.

Note: Both OTP data blocks and lock blocks cannot be erased.

## 3.6 Register address mapping

Table 14 FMC Register Address Mapping

| Register name | Description                   | Offset address |
|---------------|-------------------------------|----------------|
| FMC_ACCTRL    | Flash access control register | 0x00           |
| FMC_KEY       | Flash key register            | 0x04           |
| FMC_OPTKEY    | Flash option key register     | 0x08           |
| FMC_STS       | Flash state register          | 0x0C           |
| FMC_CTRL      | Flash control register        | 0x10           |

| Register name | Description                   | Offset address |
|---------------|-------------------------------|----------------|
| FMC_OPTCTRL   | Flash option control register | 0x14           |

## 3.7 Register functional description

### 3.7.1 Flash access control register (FMC\_ACCTRL)

Offset address: 0x00

Reset value: 0x0000 0000

| Field | Name          | R/W | Description                                                                                                                                                             |
|-------|---------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0   | WAITP         | R/W | Wait Period<br>This bit means the number of wait cycles.<br>000: 0<br>001: 1<br>010: 2<br>011: 3<br>100: 4<br>101: 5<br>...<br>1111111: 127                             |
| 7     | Reserved      |     |                                                                                                                                                                         |
| 8     | PREFEN        | R/W | Prefetch Enable<br>0: Disable<br>1: Enable                                                                                                                              |
| 9     | ICACHEEN      | R/W | Instruction Cache Enable<br>0: Disable<br>1: Enable                                                                                                                     |
| 10    | DCACHEEN      | R/W | Data Cache Enable<br>0: Disable<br>1: Enable                                                                                                                            |
| 11    | ICACHERST     | R/W | Instruction Cache Reset<br>0: Invalid<br>1: Reset                                                                                                                       |
| 12    | DCACHERST     | R/W | Data Cache Reset<br>0: Invalid<br>1: Reset                                                                                                                              |
| 14:13 | Reserved      |     |                                                                                                                                                                         |
| 15    | Prefetch more | R/W | Prefetch More<br>1: Initiate the next prefetch after the prefetch buffer/cache is accessed<br>0: Initiate the next prefetch after the same cache line is accessed twice |
| 31:16 | Reserved      |     |                                                                                                                                                                         |

### 3.7.2 Flash key register (FMC\_KEY)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                             |
|-------|------|-----|-------------------------------------------------------------------------|
| 31:0  | KEY  | W   | Key<br>When unlocking, this key needs to be written into this register. |

### 3.7.3 Flash option key register (FMC\_OPTKEY)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name   | R/W | Description                                                                    |
|-------|--------|-----|--------------------------------------------------------------------------------|
| 31:0  | OPTKEY | W   | Option Key<br>When unlocking, this key needs to be written into this register. |

### 3.7.4 Flash state register (FMC\_STS)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field | Name     | R/W   | Description                                                                                                                  |
|-------|----------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0     | OPRCMP   | RC_W1 | Operation Complete<br>This bit will be set to 1 when the operation for Flash is completed.                                   |
| 1     | OPRERR   | RC_W1 | Operation Error<br>This bit will be set to 1 when an error occurs in operation process.                                      |
| 3:2   | Reserved |       |                                                                                                                              |
| 4     | WPROTERR | RC_W1 | Write Protection Error<br>This bit will be set to 1 when erase/write operation is performed for Flash write protection area. |
| 5     | PGALGERR | RC_W1 | Programming Alignment Error<br>This bit will be set to 1 when a programming alignment error occurs.                          |
| 6     | PGPRLERR | RC_W1 | Programming Parallelism Error<br>This bit will be set to 1 when a programming parallelism error occurs.                      |
| 7     | PGSEQERR | RC_W1 | Programming Sequence Error<br>This bit will be set to 1 when a programming sequence error occurs.                            |
| 15:8  | Reserved |       |                                                                                                                              |
| 16    | BUSY     | R     | Busy<br>This bit will be set to 1 when operation is performed for Flash.                                                     |
| 31:17 | Reserved |       |                                                                                                                              |

### 3.7.5 Flash control register (FMC\_CTRL)

Offset address: 0x10

Reset value: 0x8000 0000

This register can be accessed only when there is no ongoing Flash operation.

| Field | Name     | R/W | Description                                                                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PG       | R/W | Programming<br>When this bit is set to 1, Flash programming can be enabled.                                                                                                   |
| 1     | SERS     | R/W | Sector Erase<br>When this bit is set to 1, sector erase can be enabled.                                                                                                       |
| 2     | MERS     | R/W | Mass Erase<br>When this bit is set to 1, mass erase can be enabled.                                                                                                           |
| 6:3   | SNUM     | R/W | Sector Number<br>This bit field is used for the specified erase sector.<br>0000: Sector 0<br>0001: Sector 1<br>0010: Sector 2<br>.....<br>1011: Sector 11<br>Others: Reserved |
| 7     | Reserved |     |                                                                                                                                                                               |
| 10:8  | PGSIZE   | R/W | Program Size<br>This bit field is used to select the number of parallel bits.<br>000: 8-bit<br>001: 16-bit<br>010: 32-bit<br>011: 64-bit                                      |
| 15:11 | Reserved |     |                                                                                                                                                                               |
| 16    | START    | R/S | Start<br>When this bit is set to 1, the erase operation can be started. This bit will be cleared to zero when BUSY bit is cleared to zero.                                    |
| 23:17 | Reserved |     |                                                                                                                                                                               |
| 24    | OPCINTEN | R/W | Operation Complete Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                |
| 25    | ERRINTEN | R/W | Error Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                             |
| 30:26 | Reserved |     |                                                                                                                                                                               |
| 31    | LOCK     | R/S | Lock<br>When this bit is set to 1, it means that this register is locked. When the unlocking sequence is detected, it will be cleared to zero by the hardware.                |

### 3.7.6 Flash option control register (FMC\_OPTCTRL)

Offset address: 0x14

Reset value: 0x0FFF AAED

This register can be accessed only when there is no ongoing Flash operation.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                  |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OPTLOCK  | R/S | Option Lock<br>When this bit is set to 1, it means that this register is locked.<br>When the unlocking sequence is detected, it will be cleared to zero by the hardware.                                                                                                                                     |
| 1     | OPTSTART | R/S | Option Start<br>After this bit is set to 1 by the software, the option byte can be operated and it can be cleared to zero when the BUSY bit is set to zero.                                                                                                                                                  |
| 3:2   | BORLVL   | R/W | Brownout Reset Level<br>When the power supply voltage is less than the threshold of the brownout reset level, a reset will be generated.<br>00: Level 3, voltage range: 2.7V-3.6V<br>01: Level 2, voltage range: 2.4V-2.7V<br>10: Level 1, voltage range: 2.1V-2.4V<br>11: Disable, voltage range: 1.8V-2.1V |
| 4     | Reserved |     |                                                                                                                                                                                                                                                                                                              |
| 5     | WDTSEL   | R/W | Watchdog Select<br>0: Hardware watchdog<br>1: Software watchdog<br>Note: When WDTSEL mode switches from hardware to software or from software to hardware, a system reset is required for the change to take effect.                                                                                         |
| 6     | RSTSTOP  | R/W | Reset in STOP Mode<br>0: Reset occurs when entering the Stop mode<br>1: Reset does not occur when entering the Stop mode                                                                                                                                                                                     |
| 7     | RSTSTDB  | R/W | Reset in STANDBY Mode<br>0: Reset occurs when entering the Standby mode<br>1: Reset does not occur when entering the Standby mode                                                                                                                                                                            |
| 15:8  | RPROT    | R/W | Read Protect<br>This bit field is used to select the e-read protection level.<br>0xAA: Level 0<br>0xCC: Level 2<br>Others: Level 1                                                                                                                                                                           |
| 27:16 | NWPROT   | R/W | No Write Protect<br>0: Write protection is enabled<br>1: Write protection is disabled                                                                                                                                                                                                                        |
| 31:28 | Reserved |     |                                                                                                                                                                                                                                                                                                              |



## 4 External Memory Controller (EMMC)

### 4.1 Full name and abbreviation description of terms

Table 15 Full name and abbreviation description of terms

| Full name in English                     | English abbreviation |
|------------------------------------------|----------------------|
| Static Random Access Memory              | SRAM                 |
| Read Only Memory                         | ROM                  |
| Pseudo Static Random Access Memory       | PSRAM                |
| Random Access Memory                     | RAM                  |
| Synchronous Dynamic Random Access Memory | SDRAM                |
| Multiplex                                | MUX                  |
| Width                                    | WID                  |
| Flash Memory                             | FM                   |
| Access                                   | ACC                  |
| Wait                                     | W                    |
| Signal                                   | S                    |
| Polarity                                 | POL                  |
| Asynchronous                             | ASYN                 |
| Burst                                    | BURST                |
| Timing                                   | TIM                  |
| Setup                                    | SET                  |
| Hold                                     | HLD                  |
| Empty                                    | E                    |

### 4.2 EMMC Overview

EMMC includes SMC (static memory controller) and DMC (dynamic memory controller). SMC is responsible for controlling SRAM, PSRAM, NandFlash, NorFlash and PCCard; DMC is responsible for controlling SDRAM.

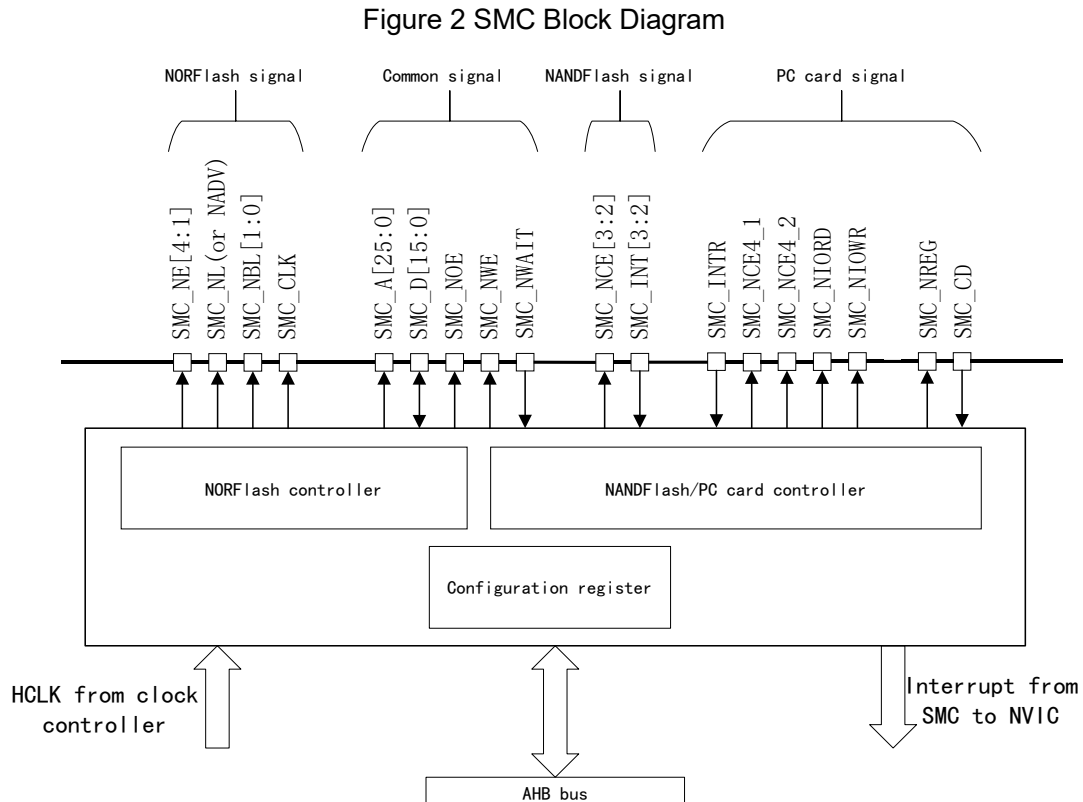
### 4.3 SMC Introduction

SMC is used to manage the extended static memory peripherals. AHB transmission signals can be converted to the appropriate external devices. There are four internal memory blocks, each of which controls different types of

memory and is distinguished by chip selection signal. Only one external device can be accessed at any moment. Each memory block can be configured separately, and the timing can be programmed for external devices.

## 4.4 SMC Structure Block Diagram

SMC consists of five parts: AHB bus interface, configuration register, NORFlash controller, NANDFlash/PC card controller and external device interface, specifically as shown in the figure below:



## 4.5 SMC Functional Description

### 4.5.1 SMC Access Rules

SMC is an interface for internal CPU to access external static memory through AHB bus. On AHB bus, the operation of 32-bit data will be converted into continuous 16 or 8-bit operation. In order to ensure the consistency of data transmission, SMC needs to comply with the following rules in external read-write operation:

- (1) When the width of AHB accessing external data is equal to that of memory data, the data can be transmitted normally without any problem.

- (2) When the width of AHB accessing external data is larger than that of memory data, the access operation will be automatically cut to be consistent with the width of external data for transmission.
- (3) When the width of AHB accessing external data is less than that of memory data, if the external memory has the function of byte selection, it can transmit data normally through byte channel. If it does not have such function, it does not allow write operation, and only allows read operation.

## 4.5.2 External device address mapping

SMC divides external devices into multiple memory blocks, and different memory blocks control different external devices. The specific classification is shown in the table below:

Table 16 External Device Address Mapping Table

| Start address | End address | Memory block            | Memory type supported |
|---------------|-------------|-------------------------|-----------------------|
| 0x6000 0000   | 0x6FFF FFFF | Memory block 1 (4*64MB) | NOR/PSRAM             |
| 0x7000 0000   | 0x7FFF FFFF | Memory block 2 (4*64MB) | NAND                  |
| 0x8000 0000   | 0x8FFF FFFF | Memory block 3 (4*64MB) | NAND                  |
| 0x9000 0000   | 0x9FFF FFFF | Memory block 4 (4*64MB) | PC card               |

## 4.5.3 NOR flash memory and PSRAM

### 4.5.3.1 Address mapping

Memory block 1 is used to control NOR/PSRAM memory, which is divided into four 64MB areas of the same size. The selection of each area depends on the value of HADDR [27:26], and the specific information is as follows:

Table 17 Address Mapping of Memory Block 1

| HADDR[27:26] | Start address | End address | Area block   |
|--------------|---------------|-------------|--------------|
| 00           | 0x6000 0000   | 0x63FF FFFF | Area block 1 |
| 01           | 0x6400 0000   | 0x67FF FFFF | Area block 2 |
| 10           | 0x6800 0000   | 0x6BFF FFFF | Area block 3 |
| 11           | 0x6C00 0000   | 0x6FFF FFFF | Area block 4 |

HADDR is the internal AHB address line that needs to be converted to the external memory. It is a byte address. However, some external memories are not accessed by byte, so the address may be inconsistent. In order to avoid the error caused by this situation, SMC will be adjusted according to the following rules:

- When the width of external memory data is 8 bits, HADDR[25:0] is connected to SMC\_A [25:0], while SMC\_A[25:0] is connected to the external memory address line.
- When the width of external memory data is 16 bits, HADDR[25:1] is connected to SMC\_A [24:0], while SMC\_A[24:0] is connected to the external memory address line.

#### 4.5.3.2 Interface signal and controller

The memory block 1 supports NOR Flash, PSRAM, SRAM and ROM external memory. There are corresponding chip selection signals NE[x] (x=1...4) in the four areas of the memory block 1. All other signals are shared. The specific interface signals and functions are as follows:

Table 18 NOR Flash Interface Signal

| SMC signal name | Signal direction | Function                                          |
|-----------------|------------------|---------------------------------------------------|
| CLK             | Output           | Synchronous clock signal                          |
| NE[x]           | Output           | Chip selection signal, x=1...4                    |
| NOE             | Output           | Read enable signal                                |
| NEW             | Output           | Write enable signal                               |
| NWAIT           | Input            | Signal that NOR flash memory requires SMC to wait |
| A[25:0]         | Output           | Non-multiplexing: A[25:0] all are address bus     |
|                 | Output           | Multiplexing: A[25:16] is address bus             |
| AD[15:0]        | Input/Output     | Non-multiplexing: Bidirectional data bus          |
|                 | Input/Output     | Multiplexing: Bidirectional address/Data bus      |
| NL (=NADV)      | Output           | Effective address signal                          |

Table 19 PSRAM Interface Signal

| SMC signal name | Signal direction | Function                               |
|-----------------|------------------|----------------------------------------|
| CLK             | Output           | Synchronous clock signal               |
| NE[x]           | Output           | Chip selection signal, x=1...4         |
| NOE             | Output           | Read enable signal                     |
| NEW             | Output           | Write enable signal                    |
| NWAIT           | Input            | Signal that PSRAM requires SMC to wait |
| A[25:0]         | Output           | Address bus                            |
| D[15:0]         | Input/Output     | Bidirectional data bus                 |
| NL (=NADV)      | Output           | Effective address signal               |

| SMC signal name | Signal direction | Function          |
|-----------------|------------------|-------------------|
| NBL[1]          | Output           | High bytes enable |
| NBL[0]          | Output           | Low bytes enable  |

Note: The output signal of the controller changes at the rising edge of the internal clock. In the synchronous write mode, the output data changes at the falling edge of the memory clock.

NOR Flash/PSRAM controller provides programmable timing parameters for external memory, including the parameters in the following table:

Table 20 Programmable NOR/PSRAM Timing Parameters

| Parameter             | Function                                                               | Access mode                      | Unit                     | Minimum | Maximum |
|-----------------------|------------------------------------------------------------------------|----------------------------------|--------------------------|---------|---------|
| Data generation time  | The number of clocks required to generate the first data in burst mode | Synchronous                      | Memory clock cycle (CLK) | 2       | 17      |
| Clock division factor | The ratio of memory access clock cycle (CLK) to AHB clock cycle        | Synchronous                      | AHB clock cycle (HCLK)   | 2       | 16      |
| Bus recovery time     | Duration of Bus recovery phase                                         | Asynchronous or synchronous read |                          | 1       | 16      |
| Data setup time       | Duration of data setup phase                                           | Asynchronous                     |                          | 2       | 256     |
| Address hold time     | Duration of address hold phase                                         | Synchronous, multiplexing IO     |                          | 2       | 16      |
| Address setup time    | Duration of address setup phase                                        | Asynchronous                     |                          | 1       | 16      |

#### 4.5.4 NAND flash memory and PC card

##### 4.5.4.1 Address mapping

Memory blocks 2, 3 and 4 are used to access NAND flash memory and PC card. Each memory block is also divided into different areas, the corresponding effect of different areas is different, and the specific distribution is as follows:

Table 21 Address Mapping of Memory Blocks 2 3 and 4

| SMC memory block                 | Storage space | Start address | End address |
|----------------------------------|---------------|---------------|-------------|
| Memory block 2-NAND flash memory | General       | 0x7000 0000   | 0x73FF FFFF |
|                                  | Attributes    | 0x7800 0000   | 0x7BFF FFFF |
|                                  | General       | 0x8000 0000   | 0x83FF FFFF |

| SMC memory block                 | Storage space | Start address | End address |
|----------------------------------|---------------|---------------|-------------|
| Memory block 3-NAND flash memory | Attributes    | 0x8800 0000   | 0x8BFF FFFF |
| Memory block 4-PC card           | General       | 0x9000 0000   | 0x93FF FFFF |
|                                  | Attributes    | 0x9800 0000   | 0x9BFF FFFF |
|                                  | I/O           | 0x9C00 0000   | 0x9FFF FFFF |

NAND flash memory block is divided into three blocks in part of the low-byte area, and different blocks can be accessed through HADDR [17:16]. The specific division and selection of these three blocks are shown in the table below:

Table 22 NAND Memory Block Division

| HADDR[17:16] | Address range     | Block name    |
|--------------|-------------------|---------------|
| 00           | 0x000000-0x00FFFF | Data block    |
| 01           | 0x010000-0x01FFFF | Command block |
| 1X           | 0x020000-0x03FFFF | Address block |

In order to read and write NAND memory normally, the following steps are needed:

- (1) Transmit command to the memory
- (2) Transmit the address for reading and writing to the memory
- (3) Read/Write data

The three steps correspond to specific addresses, each of which maps to one of the three divided blocks within the memory. To transmit a command to the memory is to write the corresponding command value to the command block. To transmit an address to the memory is to transmit the corresponding address value to the address block. To read and write data is to read and write in the data block. Finally, write or read out the internal unit of NAND, and the address of the corresponding unit is the address written in the address block.

#### 4.5.4.2 Interface signal and controller

NAND/PC card controller can control three memory blocks. The memory blocks 2 and 3 support NAND Flash, and the memory block 4 supports PC card devices. Three memory blocks have their own chip selection signals, and the specific interfaces and functions are as follows:

Table 23 NAND Flash Interface Signal

| SMC signal name | Signal direction | Function                      |
|-----------------|------------------|-------------------------------|
| NCE[x]          | Output           | Chip selection signal, x=2, 3 |

| SMC signal name | Signal direction | Function                                                    |
|-----------------|------------------|-------------------------------------------------------------|
| NOE (=NRE)      | Output           | Read enable signal                                          |
| NEW             | Output           | Write enable signal                                         |
| NWAIT/INT[3:2]  | Input            | NAND Flash ready/busy input signal                          |
| A[17]           | Output           | NAND Flash address latch signal (ALE)                       |
| A[16]           | Output           | NAND Flash command latch signal (CLE)                       |
| D[15:0]         | Input/Output     | 8-bit multiplexing: D[7:0] bidirectional address/data bus   |
|                 | Input/Output     | 16-bit multiplexing: D[15:0] bidirectional address/data bus |

Table 24 PC Card Interface Signal

| SMC signal name | Signal direction | Function                                                                    |
|-----------------|------------------|-----------------------------------------------------------------------------|
| NCE4_1          | Output           | Chip selection signal 1                                                     |
| NCE4_2          | Output           | Chip selection signal 2 (select 16-bit or 8-bit operation)                  |
| NOE             | Output           | Read enable signal                                                          |
| NEW             | Output           | Write enable signal                                                         |
| NWAIT           | Input            | PC card wait signal                                                         |
| INTR            | Input            | PC card interrupt signal                                                    |
| CD              | Input            | PC card detection signal                                                    |
| A[10:0]         | Output           | Address bus                                                                 |
| NIOS16          | Input            | Data transmission width of 16-bit transmission I/O space (must be grounded) |
| NIORD           | Output           | I/O space output enable                                                     |
| NIOWR           | Output           | I/O space write enable                                                      |
| NREG            | Output           | Selection of common space or attribute space access                         |
| D[15:0]         | Output/Input     | Bidirectional data bus                                                      |

NAND Flash/PC card controller provides programmable timing parameters for external memory, including the parameters in the following table:

Table 25 Programmable NAND/PC Card Timing Parameters

| Parameter                           | Function                                                                                                  | Operation mode | Unit                   | Minimum | Maximum |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------|----------------|------------------------|---------|---------|
| Memory data bus high-impedance time | The duration for which the data bus remains in high-impedance state after initiating the write operation. | Write          | AHB clock cycle (HCLK) | 0       | 255     |

| Parameter           | Function                                                                                                                                         | Operation mode | Unit | Minimum | Maximum |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|----------------|------|---------|---------|
| Memory hold time    | The number of clock cycles the address is held after the command is transmitted. During a write operation, it also serves as the data hold time. | Read/Write     |      | 1       | 254     |
| Memory waiting time | Minimum transmitting duration                                                                                                                    |                |      | 2       | 256     |
| Memory setup time   | The number of clock cycles for the address setup before sending the command.                                                                     |                |      | 1       | 255     |

## 4.6 SMC register address mapping

Table 26 SMC Register Address Mapping

| Register name   | Description                                                 | Offset address                       |
|-----------------|-------------------------------------------------------------|--------------------------------------|
| SMC_CSCTRL1...4 | SRAM/NOR flash memory chip selection control register 1...4 | $8*(x-1)$ , $x=1...4$                |
| SMC_CSTIM1...4  | SRAM/NOR flash memory chip selection timing register 1...4  | $0x04 + 8*(x-1)$ , $x=1...4$         |
| SMC_WRTTIM1...4 | SRAM/NOR flash memory write timing register 1...4           | $0x104 + 8*(x-1)$ , $x=1...4$        |
| SMC_CTRL2...4   | PC card/NAND flash memory control register 2...4            | $0x40 + 0x20 * (x-1)$ , $x=2...4$    |
| SMC_STSINT2...4 | FIFO state and interrupt register 2...4                     | $0x44 + 0x20 * (x-1)$ , $x=2...4$    |
| SMC_CMSTIM2...4 | General-purpose memory space timing register 2...4          | $0x48 + 0x20 * (x-1)$ , $x=2...4$    |
| SMC_AMSTIM2...4 | Attribute memory space timing register 2...4                | $0x4C + 0x20 * (x-1)$ , $x=2...4$    |
| SMC_IOSTIM4     | I/O space timing register 4                                 | 0XB0                                 |
| SMC_ECCRS2/3    | ECC result register 2/3                                     | $0x54 + 0x20 * (x-1)$ , $x=2$ or $3$ |

## 4.7 SMC register functional description

### 4.7.1 NOR flash memory and PSRAM control register

#### 4.7.1.1 SRAM/NOR flash memory chip selection control register 1...4

##### (SMC\_CSCTRL1...4)

Offset address:  $0x8*(x-1)$ ,  $x=1...4$

Reset value: 0x0000 30DX



| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                             |
|-------|------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | MBKEN      | R/W | Enable the Corresponding Memory Bank<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                         |
| 1     | ADMUXEN    | R/W | Address/Data Multiplexing Enable<br>This bit is effective only for NORFlash and PSRAM.<br>0: Disable<br>1: Address low 16-bit and data sharing data bus                                                                                                                                                                                 |
| 3:2   | MTYPECFG   | R/W | Memory Type Configure<br>00: SRAM, ROM (default value of Bank2~Bank4 after reset)<br>01: PSRAM<br>10: NORFlash (default value after Bank1 reset)<br>Others: Reserved                                                                                                                                                                    |
| 5:4   | MDBWIDCFG  | R/W | Memory Data Bus Width Configure<br>00: 8 bits<br>01: 16 bits<br>Others: Reserved                                                                                                                                                                                                                                                        |
| 6     | NORFMACCEN | R/W | NORFlash Memory Access Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                |
| 7     | Reserved   |     |                                                                                                                                                                                                                                                                                                                                         |
| 8     | BURSTEN    | R/W | Burst Mode Enable<br>In synchronous mode, use the burst mode to access the memory.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                           |
| 9     | WSPOLCFG   | R/W | Wait Signal Polarity Configure<br>This bit is effective only in burst mode.<br>0: Low effective<br>1: High effective                                                                                                                                                                                                                    |
| 10    | WRAPBEN    | R/W | Wrapped Burst Mode Enable<br>This bit is effective only in burst mode.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                       |
| 11    | WTIMCFG    | R/W | Wait Timing Configure<br>This bit is used to configure whether the memory generates NWAIT signal in the period before the waiting state or during the waiting period; this bit is effective only in burst mode.<br>0: NWAIT signal is effective in the data period before waiting<br>1: NWAIT signal is effective in the waiting period |
| 12    | WREN       | R/W | Write Memory Enable<br>This bit is used to enable write operation of SMC for the memory.<br>0: Disable write; otherwise, an AHB error will be generated<br>1: Allow write                                                                                                                                                               |
| 13    | WAITEN     | R/W | Wait Enable                                                                                                                                                                                                                                                                                                                             |

| Field | Name         | R/W | Description                                                                                                                                                                                                  |
|-------|--------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |              |     | This bit is used to enable NWAIT signal to insert the wait state; this bit is effective only in burst mode.<br>0: Disable<br>1: Enable                                                                       |
| 14    | EXTMODEEN    | R/W | Extended Mode Enable<br>In extended mode, SMC_WRTTIM register can be used to achieve read and write using different timing function.<br>0: Disable<br>1: Enable                                              |
| 15    | WSASYNCEN    | R/W | Wait Signal During Asynchronous Transfers Enable<br>This bit is used to enable SMC to use NWAIT signal during asynchronous protocol period.<br>0: Disable<br>1: Enable                                       |
| 18:16 | CRAMPSIZECFG | R/W | CRAM Page Size Configure<br>000: There is no burst split when crossing the page boundary<br>001: 128 bytes<br>010: 256 bytes<br>011: 512 bytes<br>100: 1024 bytes<br>Others: Reserved                        |
| 19    | WRBURSTEN    | R/W | Write PSRAM Burst Enable<br>This bit is used to enable the synchronous burst transmission protocol for write operation.<br>0: Write operation is asynchronous mode<br>1: Write operation is synchronous mode |
| 31:20 | Reserved     |     |                                                                                                                                                                                                              |

#### 4.7.1.2 SRAM/NOR flash memory chip selection timing register 1...4 (SMC\_CSTIM1...4)

Offset address:  $0x04 + 8 \times (x-1)$ ,  $x=1 \dots 4$

Reset value: 0x0FFF FFFF

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                          |
|-------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | ADDRSETCFG | R/W | Address Setup Time Configure<br>Only apply to NOR flash memory operation in SRAM, ROM and asynchronous bus multiplexing mode.<br>0000: One HCLK clock cycle<br>0001: 2 HCLK clock cycles<br>.....<br>1111: 16 HCLK clock cycles<br>Note: In synchronous operation, this parameter is meaningless and is always 1 memory clock cycle. |
| 7:4   | ADDRHLDCFG | R/W | Address-Hold Time Configure<br>Only apply to NOR flash memory operation in SRAM, ROM and asynchronous bus multiplexing mode.<br>0000: Reserved                                                                                                                                                                                       |

| Field | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |             |     | 0001: 2 HCLK clock cycles<br>.....<br>1111: 16 HCLK clock cycles<br>Note: In synchronous operation, this parameter is meaningless and is always 1 memory clock cycle.                                                                                                                                                                                                                                                                                      |
| 15:8  | DATASETCFG  | R/W | Data Setup Time Configure<br>Only apply to NOR flash memory operation in SRAM, ROM and asynchronous bus multiplexing mode.<br>0000 0000: Reserved<br>0000 0001: 2 HCLK clock cycles<br>0000 0010: 3 HCLK clock cycles<br>.....<br>1111 1111: 256 HCLK clock cycles                                                                                                                                                                                         |
| 19:16 | BUSTURNCFG  | R/W | Bus Turnaround Phase Duration Configure<br>These bits are used to configure the delay time on the bus after a read operation. They are only applicable to NOR flash memory operation in bus multiplexing mode.<br>0000: 1 HCLK clock cycle<br>0001: 2 HCLK clock cycles<br>.....<br>1111: 16 HCLK clock cycles                                                                                                                                             |
| 23:20 | CLKDIVCFG   | R/W | Clock Divide Factor Configure<br>CLK comes from HCLK frequency division. These bits are used to configure the frequency of CLK clock output signal. They are only applicable to synchronous mode.<br>0000: Reserved<br>0001: 2 divided frequency<br>0010: 3 divided frequency<br>.....<br>1111: 16 divided frequency<br>Note: This parameter is ineffective when accessing asynchronous NOR flash memory, SRAM or ROM.                                     |
| 27:24 | DATALATCFG  | R/W | Data Latency Configure<br>These bits are used to configure the number of memory cycles for waiting before reading the first data. They are only applicable to NOR flash memory operation in synchronous burst mode.<br>0000: 2 CLK clock cycles<br>0001: 3 CLK clock cycles<br>.....<br>1111: 17 CLK clock cycles<br>Note: When accessing asynchronous NOR flash memory, SRAM or ROM, this parameter is invalid. When operating CRAM, this parameter is 0. |
| 29:28 | ASYNCAACCFG | R/W | Asynchronous Access Mode Configure<br>Valid only when EXTMODEEN bit of SMC_CSCTRLX register is 1.<br>00: Access mode A<br>01: Access mode B<br>10: Access mode C                                                                                                                                                                                                                                                                                           |

| Field | Name     | R/W | Description       |
|-------|----------|-----|-------------------|
|       |          |     | 11: Access mode D |
| 31:30 | Reserved |     |                   |

#### 4.7.1.3 SRAM/NOR flash memory write timing register 1...4 (SMC\_WRTTIM1...4)

Offset address:  $0x104 + 8 \times (x-1)$ ,  $x=1 \dots 4$

Reset value: 0x0FFF FFFF

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | ADDRSETCFG | R/W | <p>Address Setup Time Configure</p> <p>Only apply to NOR flash memory operation in SRAM, ROM and asynchronous bus multiplexing mode.</p> <p>0000: 1 HCLK clock cycle</p> <p>0001: 2 HCLK clock cycles</p> <p>.....</p> <p>1111: 16 HCLK clock cycles</p> <p>Note: In synchronous operation, this parameter is meaningless and is always 1 memory clock cycle.</p> |
| 7:4   | ADDRHLDCFG | R/W | <p>Address-Hold Time Configure</p> <p>Only apply to NOR flash memory operation in SRAM, ROM and asynchronous bus multiplexing mode.</p> <p>0000: Reserved</p> <p>0001: 2 HCLK clock cycles</p> <p>.....</p> <p>1111: 16 HCLK clock cycles</p> <p>Note: In synchronous operation, this parameter is meaningless and is always 1 memory clock cycle.</p>            |
| 15:8  | DATASETCFG | R/W | <p>Data-Setup Time Configure</p> <p>Only apply to NOR flash memory operation in SRAM, ROM and asynchronous bus multiplexing mode.</p> <p>0000 0000: Reserved</p> <p>0000 0001: 2 HCLK clock cycles</p> <p>0000 0010: 3 HCLK clock cycles</p> <p>.....</p> <p>1111 1111: 256 HCLK clock cycles</p>                                                                 |
| 19:16 | BUSTURNCFG | R/W | <p>Bus Turnaround Phase Duration Configure</p> <p>These bits are used to configure the delay time on the bus after a read operation. They are only applicable to NOR flash memory operation in bus multiplexing mode.</p> <p>0000: 1 HCLK clock cycle</p> <p>0001: 2 HCLK clock cycles</p> <p>.....</p> <p>1111: 16 HCLK clock cycles</p>                         |
| 23:20 | CLKDIVCFG  | R/W | <p>Clock Divide Ratio for CLK Signal Configure</p> <p>Cycle of CLK clock output signal, expressed by the number of HCLK cycles.</p> <p>0000: Reserved</p> <p>0001: CLK cycle=2×HCLK cycle</p>                                                                                                                                                                     |

| Field | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|-------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |             |     | 0010: CLK cycle = 3×HCLK cycle<br>1111: CLK cycle = 16×HCLK cycle (default value after reset)<br>This bit is invalid in asynchronous NOR Flash, SRAM or ROM access mode.                                                                                                                                                                                                                                                    |
| 27:24 | DATLATCFG   | R/W | Data Latency Configure<br>This bit is used to define the memory clock to be transmitted to the memory before obtaining the first data<br>Period number (+2).<br>0000: Data delay of 2 CLK clock cycles during the first burst access<br>...<br>1111: Data delay of 17 CLK clock cycles during the first burst access (default value after reset)<br>This bit is invalid in asynchronous NOR Flash, SRAM or ROM access mode. |
| 29:28 | ASYNCAACCFG | R/W | Asynchronous Access Mode Configure<br>These bits are used to configure asynchronous access mode, and are valid only when EXTMODEEN bit of SMC_CSCTRLX register is 1.<br>00: Access mode A<br>01: Access mode B<br>10: Access mode C<br>11: Access mode D                                                                                                                                                                    |
| 31:30 | Reserved    |     |                                                                                                                                                                                                                                                                                                                                                                                                                             |

## 4.7.2 NAND flash memory and PC card control register

### 4.7.2.1 PC card/NAND flash control register 2...4 (SMC\_CTRL2...4)

Offset address: 0x40 + 0x20 \* (x-1), x=2...4

Reset value: 0x0000 0018

| Field | Name     | R/W | Description                                                                                                  |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------|
| 0     | Reserved |     |                                                                                                              |
| 1     | WAITFEN  | R/W | PC Card/NANDFlash Wait Feature Enable<br>0: Disable<br>1: Enable                                             |
| 2     | MBKEN    | R/W | (PC Card/NAND Flash Memory Bank Enable<br>0: Disable<br>1: Enable                                            |
| 3     | MTYPECFG | R/W | Memory Type Configure<br>0: PC card, CF card, CF+ card or PCMCIA<br>1: NAND flash memory                     |
| 5:4   | DBWIDCFG | R/W | Databus Width Configure<br>16 bits must be used for PC Card.<br>00: 8 bits<br>01: 16 bits<br>Others reserved |

| Field | Name     | R/W | Description                                                                                                                                                                               |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6     | ECCEN    | R/W | ECC Computation Logic Enable<br>0: Disable and reset ECC<br>1: Enable                                                                                                                     |
| 8:7   | Reserved |     |                                                                                                                                                                                           |
| 12:9  | C2RDCFG  | R/W | CLE To RE Delay Configure<br>Configure the duration from "CLE becomes low level" to "RE becomes low level".<br>0000: 1 HCLK cycle<br>0000: 2 HCLK cycles<br>.....<br>1111: 16 HCLK cycles |
| 16:13 | A2RDCFG  | R/W | ALE To RE Delay Configure<br>Configure the duration from "ALE becomes low level" to "RE becomes low level"<br>0000: 1 HCLK cycle<br>0000: 2 HCLK cycles<br>.....<br>1111: 16 HCLK cycles  |
| 19:17 | ECCPSCFG | R/W | ECC Page Size Configure<br>000: 256 bytes<br>001: 512 bytes<br>010: 1024 bytes<br>011: 2048 bytes<br>100: 4096 bytes<br>101: 8192 bytes                                                   |
| 31:20 | Reserved |     |                                                                                                                                                                                           |

#### 4.7.2.2 FIFO state and interrupt register 2...4 (SMC\_STSINT2...4)

Offset address:  $0x44 + 0x20 * (x-1)$ ,  $x=2...4$

Reset value: 0x0000 0040

| Field | Name   | R/W | Description                                                                                                                         |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------|
| 0     | IREFLG | R/W | Interrupt Rising Edge Generate Flag<br>This bit is set to 1 by hardware and cleared by software.<br>0: Not generate<br>1: Generate  |
| 1     | IHLFLG | R/W | Interrupt High-Level Generate Flag<br>This bit is set to 1 by hardware and cleared by software.<br>0: Not generate<br>1: Generate   |
| 2     | IFEFLG | R/W | Interrupt Falling Edge Generate Flag<br>This bit is set to 1 by hardware and cleared by software.<br>0: Not generate<br>1: Generate |

| Field | Name     | R/W | Description                                                        |
|-------|----------|-----|--------------------------------------------------------------------|
| 3     | IREDEN   | R/W | Interrupt Rising Edge Detection Enable<br>0: Disable<br>1: Enable  |
| 4     | IHLDEN   | R/W | Interrupt High-Level Detection Enable<br>0: Disable<br>1: Enable   |
| 5     | IFEDEN   | R/W | Interrupt Falling Edge Detection Enable<br>0: Disable<br>1: Enable |
| 6     | FEFLG    | R   | FIFO Empty Flag<br>0: Not empty<br>1: Empty                        |
| 31:7  | Reserved |     |                                                                    |

#### 4.7.2.3 General-purpose memory space timing register 2...4 (SMC\_CMSTIM2...4)

Offset address:  $0x48 + 0x20 * (x-1)$ ,  $x=2...4$

Reset value: 0xFCFC FCFC

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | SETx  | R/W | Common Memory x Setup Time Configure<br>This bit takes HCLK as the clock cycle, and defines the time of setting up the address before sending the command.<br>0000 0000: 1 HCLK cycle<br>0000 0001: 2 HCLK cycles<br>.....<br>1111 1110: 255 HCLK cycles<br>1111 1111: Reserved                                                                                                                                                                                                                   |
| 15:8  | WAITx | R/W | Common Memory x Wait Time Configure<br>This bit takes HCLK as the clock cycle and defines the minimum hold time of the command. After the defined time, if the waiting signal is effective low, the hold time of the command will become longer.<br>0000 0000: Reserved<br>0000 0001: 2 HCLK cycles (+ wait cycles introduced by the NWAIT going low)<br>0000 0010: 3 HCLK cycles<br>.....<br>1111 1110: 255 HCLK cycles (+ wait cycles introduced by the NWAIT going low)<br>1111 1111: Reserved |

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:16 | HLDx | R/W | <p>Common Memory x Hold Time Configure</p> <p>This bit takes HCLK as the clock cycle, and defines the hold time of address signal after sending the command.</p> <p>0000 0000: Reserved</p> <p>0000 0001: 1 HCLK cycle for write accesses, 3 HCLK cycles for read accesses</p> <p>.....</p> <p>1111 1110: 254 HCLK cycles for write accesses, 256 HCLK cycles for read accesses</p> <p>1111 1111: Reserved</p> |
| 31:24 | HIZx | R/W | <p>Common Memory x Databus Hiz Time Configure</p> <p>This bit takes HCLK as the clock cycle and defines the time of high-impedance state of data bus, which is only effective for write operation.</p> <p>0000 0000: 1 HCLK cycle</p> <p>0000 0001: 2 HCLK cycles</p> <p>.....</p> <p>1111 1110: 255 HCLK cycles</p> <p>1111 1111: Reserved</p>                                                                |

#### 4.7.2.4 Attribute memory space timing register 2...4 (SMC\_AMSTIM2...4)

Offset address:  $0x4C + 0x20 * (x-1)$ ,  $x=2...4$

Reset value: 0xFCFC FCFC

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | SETx  | R/W | <p>Attribute Memory x Setup Time Configure</p> <p>This bit takes HCLK as the clock cycle, and defines the time of setting up the address signal before sending the command.</p> <p>0000 0000: 1 HCLK cycle</p> <p>0000 0001: 2 HCLK cycles</p> <p>.....</p> <p>1111 1110: 255 HCLK cycles</p> <p>1111 1111: Reserved</p>                                                                                                                                                                                                              |
| 15:8  | WAITx | R/W | <p>Attribute Memory x Wait Time Configure</p> <p>This bit takes HCLK as the clock cycle and defines the minimum hold time of the command. After the defined time, if the waiting signal is effective low, the hold time of the command will become longer.</p> <p>0000 0000: Reserved</p> <p>0000 0001: 2 HCLK cycles (+ wait cycle introduced by the NWAIT going low)</p> <p>0000 0010: 3 HCLK cycles</p> <p>.....</p> <p>1111 1110: 255 HCLK cycles (+ wait cycle introduced by the NWAIT going low)</p> <p>1111 1111: Reserved</p> |



| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:16 | HLDx | R/W | <p>Attribute Memory x Hold Time Configure</p> <p>This bit takes HCLK as the clock cycle, and defines the hold time of address signal after sending the command.</p> <p>0000 0000: Reserved</p> <p>0000 0001: 1 HCLK cycle for write accesses, 3 HCLK cycles for read accesses</p> <p>.....</p> <p>1111 1110: 254 HCLK cycles for write accesses, 256 HCLK cycles for read accesses</p> <p>1111 1111: Reserved</p> |
| 31:24 | HIZx | R/W | <p>Attribute Memory x Databus Hiz Time Configure</p> <p>This bit takes HCLK as the clock cycle and defines the time of high-impedance state of data bus, which is only effective for write operation.</p> <p>0000 0000: 0 HCLK cycle</p> <p>0000 0001: 1 HCLK cycle</p> <p>.....</p> <p>1111 1111: 255 HCLK cycles</p>                                                                                            |

#### 4.7.2.5 I/O space timing register 4 (SMC\_IOSTIM4)

Offset address: 0xB0

Reset value: 0xFCFC FCFC

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | SET  | R/W | <p>I/O x Setup Time Configure</p> <p>This bit takes CLK as the clock cycle, and defines the time of setting up the address signal before sending the command.</p> <p>0000 0000: 1 HCLK cycle</p> <p>0000 0001: 2 HCLK cycles</p> <p>.....</p> <p>1111 1111: 256 HCLK cycles</p>                                                                                                                                                                                                                            |
| 15:8  | WAIT | R/W | <p>I/O x Wait Time Configure</p> <p>This bit takes HCLK as the clock cycle and defines the minimum hold time of the command. After the defined time, if the waiting signal is effective low, the hold time of the command will become longer.</p> <p>0000 0000: Reserved</p> <p>0000 0001: 2 HCLK cycles (+ wait cycle introduced by the NWAIT going low)</p> <p>0000 0010: 3 HCLK cycles</p> <p>.....</p> <p>1111 1111: 256 HCLK cycles(+ wait cycle introduced by the card's NWAIT signal going low)</p> |

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                    |
|-------|------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:16 | HLD  | R/W | I/O x Hold Time Configure<br>This bit takes HCLK as the clock cycle, and defines the hold time of address signal after sending the command.<br>0000 0000: Reserved<br>0000 0001: 1 HCLK cycle<br>0000 0010: 2 HCLK cycles<br>.....<br>1111 1111: 255 HCLK cycles               |
| 31:24 | HIZ  | R/W | I/O x Databus Hiz Time Configure<br>This bit takes HCLK as the clock cycle and defines the time of high-impedance state of data bus, which is only effective for write operation.<br>0000 0000: 0 HCLK cycle<br>0000 0001: 1 HCLK cycle<br>.....<br>1111 1111: 255 HCLK cycles |

#### 4.7.2.6 ECC result register 2/3 (SMC\_ECCRS2/3)

Offset address:  $0x54 + 0x20 * (x-1)$ ,  $x=2$  or  $3$

Reset value: 0x0000 0000

| Field | Name  | R/W | Description |
|-------|-------|-----|-------------|
| 31:0  | ECCRS | R   | ECC result  |

## 4.8 DMC introduction

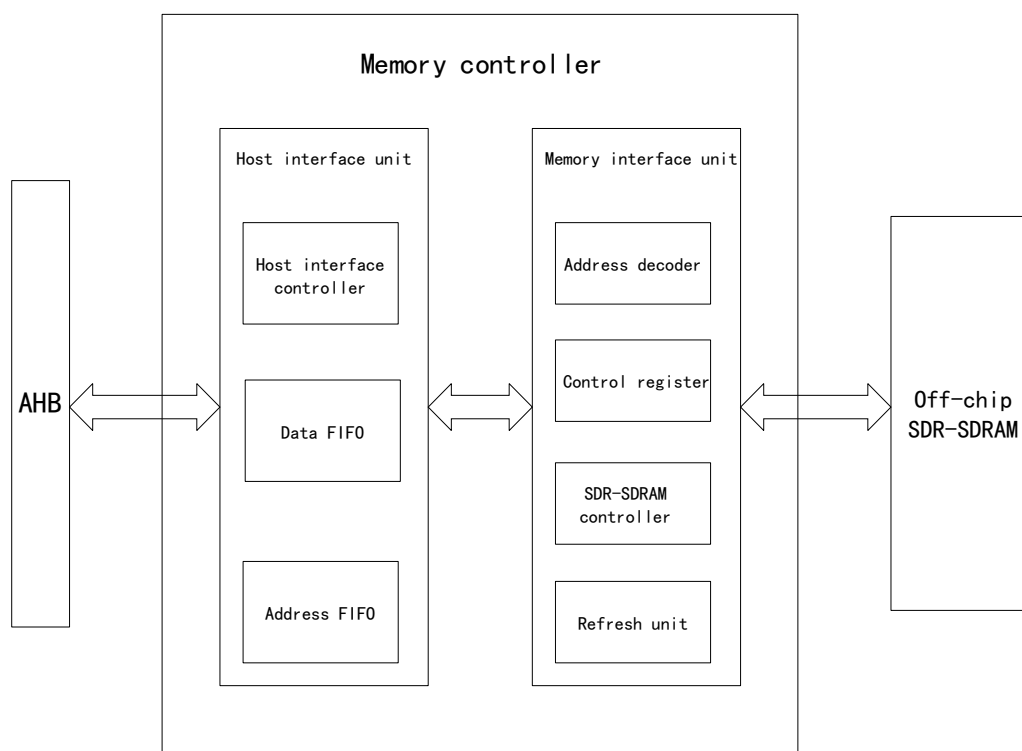
DMC is a dynamic memory controller, connected to off-chip SDR-SDRAM.

## 4.9 Main characteristics of DMC

- 16-bit data width
- Support 256MB external SDR-SDRAM, with a maximum of 13-bit row address, 12-bit column address, and 16-bit SDRAM with 4 banks
- SDR-SDRAM timing and size are configurable
- SDR-SDRAM power-down mode supported
- SDR-SDRAM auto-refresh and self-refresh mode supported

## 4.10 DMC structure block diagram

Figure 3 DMC structure block diagram



## 4.11 DMC functional description

### 4.11.1 DMC external memory interface

The signal with the prefix "N" means low effective signal.

Table 27 DMC Pins

| Signal Name | Input/Output | Pin  | Function |
|-------------|--------------|------|----------|
| A0          | Output       | PF0  | Address  |
| A1          | Output       | PF1  | Address  |
| A2          | Output       | PF2  | Address  |
| A3          | Output       | PF3  | Address  |
| A4          | Output       | PF4  | Address  |
| A5          | Output       | PF5  | Address  |
| A6          | Output       | PF12 | Address  |
| A7          | Output       | PF13 | Address  |

| Signal Name | Input/Output | Pin                | Function           |
|-------------|--------------|--------------------|--------------------|
| A8          | Output       | PF14               | Address            |
| A9          | Output       | PF15               | Address            |
| A10         | Output       | PG0                | Address            |
| A11         | Output       | PG1                | Address            |
| A12         | Output       | PG2                | Address            |
| A13         | Output       | PG3                | Address            |
| D0          | Input/Output | PD14               | Bidirectional data |
| D1          | Input/Output | PD15               | Bidirectional data |
| D2          | Input/Output | PD0                | Bidirectional data |
| D3          | Input/Output | PD1                | Bidirectional data |
| D4          | Input/Output | PE7                | Bidirectional data |
| D5          | Input/Output | PE8                | Bidirectional data |
| D6          | Input/Output | PE9                | Bidirectional data |
| D7          | Input/Output | PE10               | Bidirectional data |
| D8          | Input/Output | PE11               | Bidirectional data |
| D9          | Input/Output | PE12               | Bidirectional data |
| D10         | Input/Output | PE13               | Bidirectional data |
| D11         | Input/Output | PE14               | Bidirectional data |
| D12         | Input/Output | PE15               | Bidirectional data |
| D13         | Input/Output | PD8                | Bidirectional data |
| D14         | Input/Output | PD9                | Bidirectional data |
| D15         | Input/Output | PD10               | Bidirectional data |
| BA0         | Output       | PG4                | Bank address       |
| BA1         | Output       | PG5                | Bank address       |
| CKE         | Output       | PC3 <sup>(1)</sup> | Clock enable       |
| CLK/CK      | Output       | PG8                | Clock              |
| LDQM        | Input        | PE0                | 16-bit data write  |

| Signal Name | Input/Output | Pin  | Function                             |
|-------------|--------------|------|--------------------------------------|
| UNQM        | Input        | PE1  | 16-bit data read                     |
| NWE         | Output       | PC0  | Write enable                         |
| NCAS        | Output       | PG15 | Row address bit selection command    |
| NRAS        | Output       | PF11 | Column address bit selection command |
| NCS         | Output       | PC2  | Chip select                          |

Note: (1) See the datasheet for DMC\_CKE mapping pin.

#### 4.11.2 DMC configuration example

Configure switch register DMC\_SW as 1 to enable DMC.

The maximum value of SDRAM clock frequency is 120MHZ.

Configure the bit [9:8] of register RCM\_CFG to decide the clock frequency of SDRAM.

Example: 16M × 2 Banks × 16-bit SDRAM

- Corresponding pin of row address: A0-A13, total 14 bits
- Corresponding pin of column address: A0-A9, total 10 bits
- Corresponding pin of Bank: BA0, BA1, total 2 bits

The row address width bit of the configuration register DMC\_CFG is set to 1101.

The column address width bit of the configuration register DMC\_CFG is set to 1001;

The Bank address width bit of the configuration register DMC\_CFG is set to 01.

#### 4.12 DMC register address mapping

Table 28 DMC Register Address Mapping

| Register name | Description            | Offset address |
|---------------|------------------------|----------------|
| DMC_CFG       | Configuration register | 0x0000         |
| DMC_TIM0      | Timing register 0      | 0x0004         |
| DMC_TIM1      | Timing register 1      | 0x0008         |
| DMC_CTRL1     | Control register 1     | 0x000C         |
| DMC_REF       | Refresh register       | 0x0010         |
| DMC_SW        | Switch register        | 0x0400         |

| Register name | Description        | Offset address |
|---------------|--------------------|----------------|
| DMC_CTRL2     | Control register 2 | 0x0404         |

## 4.13 DMC register functional description

### 4.13.1 Configuration register (DMC\_CFG)

Offset address: 0x0000

Reset value: 0x0014 1388

| Field | Name   | R/W | Description                                                                                                                                                                                        |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   |        |     | Reserved                                                                                                                                                                                           |
| 4:3   | BAWCFG | R/W | Bank Address Width Configure<br>00: The bank is 1 (2 banks valid)<br>01: The bank is 2 (4 banks valid)<br>Others: Reserved                                                                         |
| 8:5   | RAWCFG | R/W | Row Address Width Configure<br>0000-1001: Reserved<br>1010: The row address is 11 bits<br>1011: The row address is 12 bits<br>...<br>1101: The row address is 14 bits<br>Others: Reserved          |
| 12:9  | CAWCFG | R/W | Column Address Width Configure<br>0000-0110: Reserved<br>0111: The column address is 8 bits<br>1000: The column address is 9 bits<br>...<br>1011: The column address is 12bits<br>Others: Reserved |
| 14:13 | DWCFG  | R/W | Data Width Configure<br>Support external SDRAM devices with 8-bit and 16-bit data bus width.<br>00: SDRAM data is 8 bits<br>01: SDRAM data is 16 bits<br>Others: Reserved                          |
| 31:15 |        |     | Reserved                                                                                                                                                                                           |

### 4.13.2 Timing register 0 (DMC\_TIM0)

Offset address: 0x0004

Reset value: 0x019A 5252

| Field | Name       | R/W | Description                                                                                                                                                                                             |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CASLSEL0   | R/W | CAS Latency Select<br>$CAS = CASLSEL0 + (ECASLSEL1 \ll 2)$<br>00: 1 clock cycle<br>01: 2 clock cycles<br>10: 3 clock cycles<br>11: 4 clock cycles<br>Others: Reserved                                   |
| 5:2   | RASMINTSEL | R/W | RAS Minimum Time Select<br>These bits are used to select the minimum time between row activation and precharge.<br>0000: 1 clock cycle<br>0001: 2 clock cycles<br>...<br>1111: 16 clock cycles          |
| 8:6   | DTIMSEL    | R/W | RAS To CAS Delay Time Select<br>000: 1 clock cycle<br>001: 2 clock cycles<br>...<br>111: 8 clock cycles                                                                                                 |
| 11:9  | PCPSEL     | R/W | Precharge Period Select<br>000: 1 clock cycle<br>001: 2 clock cycles<br>...<br>111: 8 clock cycles                                                                                                      |
| 13:12 | WRTIMSEL   | R/W | Select Time Between the Last Data and The Next Precharge for Write Operation<br>00: 1 clock cycle<br>01: 2 clock cycles<br>10: 3 clock cycles<br>11: 4 clock cycles                                     |
| 17:14 | ARPSEL     | R/W | Auto-Refresh Period Select<br>These bits are used to define the minimum time interval between two auto-refresh commands.<br>0000: 1 clock cycle<br>0001: 2 clock cycles<br>...<br>1111: 16 clock cycles |
| 21:18 | XSR0       | R/W | Minimum interval time from exiting self-refresh switch to activation command or auto-refresh read command<br>$XSR = XSR0 + (EXSR1 \ll 4)$<br>XSR = 0 ~ 511 corresponds to 1 ~ 512 SDCLK clock cycles    |

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                      |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:22 | ATACP     | R/W | Delay Period from Refresh Command to Active Command<br>This bit defines the delay between the refresh command and the activation command, and the delay between two consecutive refresh commands.<br>0000: 1 clock cycle<br>0001: 2 clock cycles<br>...<br>1111: 16 clock cycles |
| 26    | ECASLSEL1 | R/W | Extended CAS Latency<br>See CASLSEL0 descriptions.                                                                                                                                                                                                                               |
| 31:27 | EXSR1     | R/W | Minimum interval time from exiting self-refresh switch to activation command or auto-refresh read command<br>See XSR0 descriptions.                                                                                                                                              |

#### 4.13.3 Timing register 1 (DMC\_TIM1)

Offset address: 0x0008

Reset value: 0x0007 4E20

| Field | Name     | R/W | Description                                                                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | STBTIM   | R/W | Stable Time<br>After the SDRAM is powered on, clock cycles for receiving other commands.                                               |
| 19:16 | ARNUMCFG | R/W | Number Of Auto-Refresh During Initialization Configure<br>0000: 1 auto-refresh<br>0001: 2 auto-refresh<br>...<br>1111: 16 auto-refresh |
| 31:20 | Reserved |     |                                                                                                                                        |

#### 4.13.4 Control register 1 (DMC\_CTRL1)

Offset address: 0x000C

Reset value: 0x0000 3048

| Field | Name   | R/W | Description                                                                                                                                                                |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | INIT   | R/W | SDRAM Initialize<br>0: Invalid<br>1: Initialize SDRAM, and after SDRAM initialization, the hardware will automatically set 0 to this bit.                                  |
| 1     | SRMEN  | R/W | Put SDRM in Self-Refresh Mode Enable<br>0: Invalid<br>1: Enable                                                                                                            |
| 2     | PDMEN  | R/W | Put SDRM in Power-Down Mode Enable<br>0: Disable<br>1: Enable                                                                                                              |
| 3     | PCACFG | R/W | Precharge Algorithm Configure<br>0: Precharge the row immediately after read operation.<br>1: Precharge the row after a period of delay upon completion of read operation. |



| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                             |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4     | FRBSREN    | R/W | Full Refresh Before Entering Self-Refresh Mode<br>0: Only refresh one row before entering self-refresh mode<br>1: Refresh all rows before entering self-refresh mode                                                                                                                                    |
| 5     | FRASREN    | R/W | Full Refresh After Exit Self-Refresh Mode<br>0: Only refresh one row before after exiting self-refresh mode<br>1: Refresh all rows after exiting self-refresh mode                                                                                                                                      |
| 8:6   | RDNUMCFG   | R/W | Configure Number of Registers Inserted in Read Data Path<br>RDNUMCFG has a coarse delay adjustment function for read latency. When combined with the delay control bits in Control Register 2, it can correctly latch the read data.<br>000: 0 register<br>001: 1 register<br>.....<br>111: 7 registers |
| 9     | MODESET    | R/W | Mode Setup<br>1: Update SDRAM mode register. After the mode register is updated, the hardware will clear the bit automatically.                                                                                                                                                                         |
| 10    | Reserved   |     |                                                                                                                                                                                                                                                                                                         |
| 11    | SRMFLG     | R   | Self-refresh mode flag<br>0: SDRAM is not currently in self-refresh mode.<br>1: SDRAM is currently in the self-refresh mode. This bit is valid when FRBSREN is 1.                                                                                                                                       |
| 15:12 | BANKNUMCFG | R/W | Number of Open Banks Configure<br>The quantity of opened banks in the SDRAM.<br>0000: 1 bank<br>0001: 2 banks<br>.....<br>1111: 16 banks                                                                                                                                                                |
| 31:16 | Reserved   |     |                                                                                                                                                                                                                                                                                                         |

#### 4.13.5 Refresh register (DMC\_REF)

Offset address: 0x0010

Reset value: 0x0000 00C3

| Field | Name     | R/W | Description                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------|
| 15:0  | RCYCCFG  | R/W | Refresh Cycle Configure<br>Specify the number of clock cycles between two consecutive refreshes. |
| 31:16 | Reserved |     |                                                                                                  |

#### 4.13.6 Switch register (DMC\_SW)

Offset address: 0x0400

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                        |
|-------|------|-----|----------------------------------------------------|
| 0     | MCSW | R/W | Memory Controller Function Switch<br>0: Select SMC |

| Field | Name     | R/W | Description   |
|-------|----------|-----|---------------|
|       |          |     | 1: Select DMC |
| 31:1  | Reserved |     |               |

#### 4.13.7 Control register 2 (DMC\_CTRL2)

Offset address: 0x0404

Reset value: 0x0000 002E

| Field | Name     | R/W | Description                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CPHACFG  | R/W | Clock Phase Configure<br>0: The system clock is not reverse<br>1: The system clock is reverse                                                                                                                   |
| 1     | RDDEN    | R/W | RD Delay Function Enable<br>0: Enable<br>1: Disable                                                                                                                                                             |
| 4:2   | RDDCFG   | R/W | RD Clock Delay Configure<br>This bit field represents the lowest 3 bits of RDDCFG, used in combination with bits [11:10].<br>00000: 0 system clock<br>00001: 1 system clock<br>.....<br>11111: 32 system clocks |
| 5     | WPEN     | R/W | Write Pipe Enable<br>0: Disable<br>1: Enable                                                                                                                                                                    |
| 6     | BUFFEN   | R/W | DMC Accelerate Module Enable<br>By opening the buffer area, wrap the burst data transmission, and improve the SDRAM read performance.                                                                           |
| 7     | WRPSEL   | R/W | WRAP Burst Type Selection<br>0: The wrap burst length is 4 ticks of transmission<br>1: The wrap burst length is 8 ticks of transmission                                                                         |
| 9:8   | Reserved |     |                                                                                                                                                                                                                 |
| 11:10 | RDDCFG2  | R/W | RD Clock Delay Configure<br>This bit field represents the highest 2 bits of RDDCFG, used in combination with bits [4:2].                                                                                        |
| 31:12 | Reserved |     |                                                                                                                                                                                                                 |

## 5 System Configuration Controller (SYSCFG)

### 5.1 Full name and abbreviation description of terms

Table 29 Full name and abbreviation description of terms

| Full name in English | English abbreviation |
|----------------------|----------------------|
| System Configure     | SYSCFG               |

### 5.2 Main characteristics

- (1) Remapping of configuration memory
- (2) Select MAC PHY interface
- (3) Configure external interrupt of GPIO
- (4) Control I/O compensation cell

### 5.3 I/O compensation cell

When the I/O output buffer speed is configured as 50MHz or 100MHz, the I/O port noise will affect the power supply voltage. Therefore, when the power supply voltage is 2.4~3.6V, the compensation cell can be enabled to control the  $t_{r(I/O)out}/t_{f(I/O)out}$  slope to reduce the impact on the power supply.

### 5.4 Register address mapping

Table 30 SYSCFG Register Address Mapping

| Register name   | Description                            | Offset address |
|-----------------|----------------------------------------|----------------|
| SYSCFG_MMSEL    | Memory mapping selection register      | 0x00           |
| SYSCFG_PMCFG    | Peripheral mode configuration register | 0x04           |
| SYSCFG_EINTCFG1 | External interrupt register 1          | 0x08           |
| SYSCFG_EINTCFG2 | External interrupt register 2          | 0x0C           |
| SYSCFG_EINTCFG3 | External interrupt register 3          | 0x10           |
| SYSCFG_EINTCFG4 | External interrupt register 4          | 0x14           |
| SYSCFG_CCCTRL   | Compensation cell control register     | 0x20           |

### 5.5 Register functional description

#### 5.5.1 Memory mapping selection register (SYSCFG\_MMSEL)

Offset address: 0x00

Reset value: 0x0000 000X (after reset, the value of X is the same as the setting of BOOT pin)

This register is used to configure the memory area accessed at the address 0x0000 0000 through the software so as to bypass BOOT pin.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | MMSEL    | R/W | Memory Mapping Select<br>Control the memory mapping address 0x0000 0000. After reset, the parameters of these bits are determined by actual BOOT.<br>00: Main Flash mapping address: 0x0000 0000<br>01: System Flash mapping address: 0x0000 0000<br>10: SMC Bank1 (NOR/PSRAM1 and 2) mapping address: 0x0000 0000<br>DMC SDRAM Bank 1 mapping address: 0x0000 0000<br>11: Embedded SRAM1 mapping address: 0x0000 0000 |
| 31:2  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 5.5.2 Peripheral mode configuration register (SYSCFG\_PMCFG)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                  |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22:0  | Reserved |     |                                                                                                                                                                                                              |
| 23    | ENETSEL  | R/W | Ethernet PHY Interface Select<br>Control the physical layer interface.<br>0: MII interface<br>1: RMII PHY interface<br>Note: This bit shall be operated when ENET is reset and before ENET clock is enabled. |
| 31:24 | Reserved |     |                                                                                                                                                                                                              |

### 5.5.3 External interrupt register 1 (SYSCFG\_EINTCFG1)

The selected external interrupt sources represented by values of the EINTx [3:0] of the following several SYSCFG external interrupt registers are shown in the table below.

Table 31 External Interrupt Sources Selected for Different Values

| EINTx [3:0] | External interrupt source |
|-------------|---------------------------|
| 0000        | PA[x] pin                 |
| 0001        | PB[x] pin                 |
| 0010        | PC[x] pin                 |
| 0011        | PD[x] pin                 |
| 0100        | PE[x] pin                 |
| 0101        | PF[x] pin                 |
| 0110        | PG[x] pin                 |

| EINTx [3:0] | External interrupt source |
|-------------|---------------------------|
| 0111        | PH[x] pin                 |
| Others      | Reserved                  |

Offset address: 0x08

Reset value: 0x0000 0000

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=0...3).

| Field | Name     | R/W | Description                                                                                                                |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------|
| 3:0   | EINT0    | R/W | EINT0 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT0. |
| 7:4   | EINT1    | R/W | EINT1 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT1. |
| 11:8  | EINT2    | R/W | EINT2 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT2. |
| 15:12 | EINT3    | R/W | EINT3 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT3. |
| 31:16 | Reserved |     |                                                                                                                            |

#### 5.5.4 External interrupt register 2 (SYSCFG\_EINTCFG2)

Offset address: 0x0C

Reset value: 0x0000 0000

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=4...7).

| Field | Name     | R/W | Description                                                                                                                |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------|
| 3:0   | EINT4    | R/W | EINT4 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT4. |
| 7:4   | EINT5    | R/W | EINT5 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT5. |
| 11:8  | EINT6    | R/W | EINT6 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT6. |
| 15:12 | EINT7    | R/W | EINT7 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT7. |
| 31:16 | Reserved |     |                                                                                                                            |

#### 5.5.5 External interrupt register 3 (SYSCFG\_EINTCFG3)

Offset address: 0x10

Reset value: 0x0000 0000

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=8...11).

| Field | Name     | R/W | Description                                                                                                                  |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | EINT8    | R/W | EINT8 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT8.   |
| 7:4   | EINT9    | R/W | EINT9 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT9.   |
| 11:8  | EINT10   | R/W | EINT10 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT10. |
| 15:12 | EINT11   | R/W | EINT11 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT11. |
| 31:16 | Reserved |     |                                                                                                                              |

#### 5.5.6 External interrupt register 4 (SYSCFG\_EINTCFG4)

Offset address: 0x14

Reset value: 0x0000 0000

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=12...15).

Note: When the value of each bit of the register is 0x1000, this bit is reserved bit. It means that PI[15:12] is unused.

| Field | Name     | R/W | Description                                                                                                                  |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | EINT12   | R/W | EINT12 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT12. |
| 7:4   | EINT13   | R/W | EINT13 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT13. |
| 11:8  | EINT14   | R/W | EINT14 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT14. |
| 15:12 | EINT15   | R/W | EINT15 Configure<br>These bits are controlled by software to be rewritten to select the external interrupt source of EINT15. |
| 31:16 | Reserved |     |                                                                                                                              |

#### 5.5.7 Compensation cell control register (SYSCFG\_CCCTRL)

Offset address: 0x20

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                            |
|-------|------|-----|------------------------------------------------------------------------------------------------------------------------|
| 0     | CCPD | R/W | Compensation Cell Power-down<br>0: I/O compensation cell enters power-down mode<br>1: I/O compensation cell is enabled |

| Field | Name     | R/W | Description                                              |
|-------|----------|-----|----------------------------------------------------------|
| 7:1   | Reserved |     |                                                          |
| 8     | RDYFLG   | R   | Compensation Cell Ready Flag<br>0: Not ready<br>1: Ready |
| 31:9  | Reserved |     |                                                          |

## 6 Reset and Clock (RCM)

### 6.1 Full name and abbreviation description of terms

Table 32 Full name and abbreviation description of terms

| Full name in English       | English abbreviation |
|----------------------------|----------------------|
| Reset and Clock Management | RCM                  |
| Reset                      | RST                  |
| Power-On Reset             | POR                  |
| Power-Down Reset           | PDR                  |
| High Speed External Clock  | HSECLK               |
| Low Speed External Clock   | LSECLK               |
| High Speed Internal Clock  | HSICKL               |
| Low Speed Internal Clock   | LSICKL               |
| Phase Locked Loop          | PLL                  |
| Main clock output          | MCO                  |
| Calibrate                  | CAL                  |
| Trim                       | TRM                  |
| Clock Security System      | CSS                  |
| Non Maskable Interrupt     | NMI                  |

### 6.2 Reset management unit (RMU)

The reset is divided into three forms, namely, system reset, power reset and backup domain reset.

#### 6.2.1 System reset

##### 6.2.1.1 "System reset" reset source

The reset source is divided into external reset source and internal reset source.

External reset source:

- Low level on NRST pin.

Internal reset source:

- Window watchdog termination count (WWDT reset)
- Independent watchdog termination count (IWDT reset)
- Software reset (SW reset)
- Power reset
- Low-power management reset



A system reset will occur in case of any of the above events. Besides, the reset event source can be identified by viewing the reset flag bit in RCM\_CSTS (control/state register).

When the system is reset, all registers except the registers in RCM\_CSTS (control/state register) reset flag bit and backup domain will be reset to the reset state.

### **Software reset**

Software can be reset by setting SYSRESETREQ in Arm® Cortex® -M4F interrupt application and reset control register to "1".

### **Low-power management reset**

Low-power management may reset in two cases, one is when entering the standby mode, and the other is when entering the stop mode. In these two cases, if RSTSTDB (in standby mode) or RSTSTOP (in stop mode) in user selection byte is set to "0", the system will be reset rather than entering the standby or stop mode.

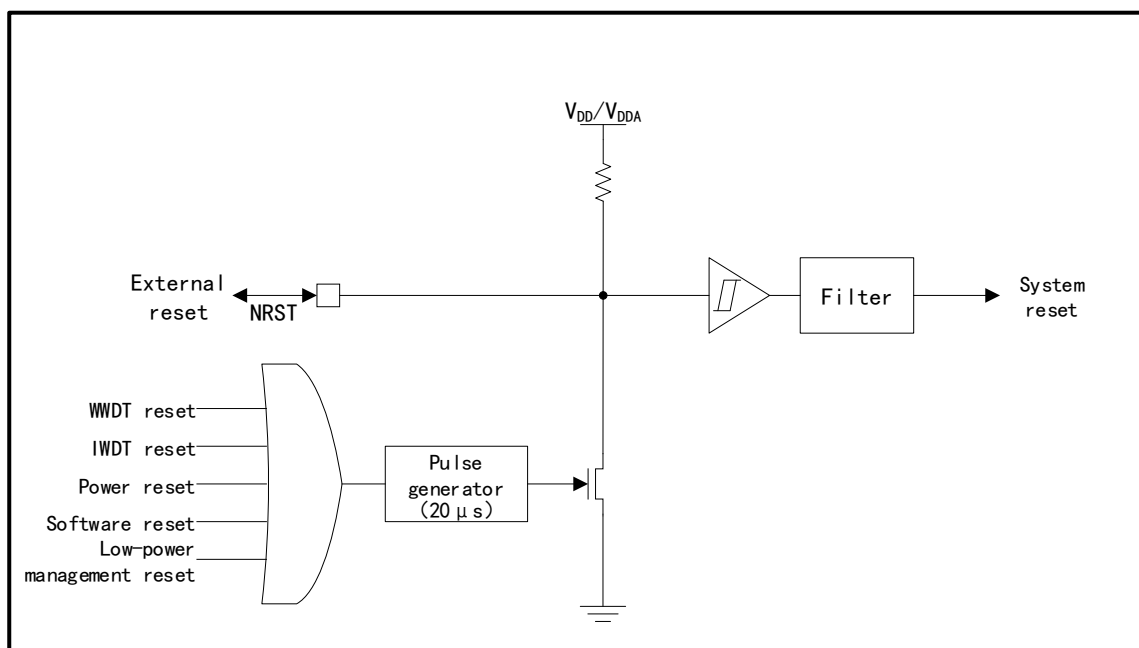
#### **6.2.1.2 "System Reset" reset circuit**

The reset source is used in the NRST pin, which remains low in reset process.

The internal reset source generates a delay of at least 20μs pulse on the NRST pin through the pulse generator, which causes the NRST to maintain the level to generate reset. The external reset source directly pulls down the NRST pin level to generate reset.

The "system reset" reset circuit is shown in the figure below.

Figure 4 "System Reset" Reset Circuit



## 6.2.2 Power reset

### "Power reset" reset source

"Power reset" reset source is as follows:

- Power-on reset (POR)
- Power-down reset (PDR)
- Brownout reset (BOR)
- Exit (wake up) from standby mode

A power reset will occur in case of any of the above events.

Power reset will reset all registers except that in backup domain.

## 6.2.3 Backup domain reset

### "Backup domain reset" reset source

"Backup domain reset" reset source is as follows:

- Software resets and sets the BDRST bit in RCM\_BDCTRL (backup domain control register)
- $V_{DD}$  or  $V_{BAT}$  is powered on again when  $V_{DD}$  and  $V_{BAT}$  is powered down

A backup domain reset will occur in case of any of the above events.

The backup domain reset has two special resets, which only affect backup domain.

## 6.3 Clock management unit (CMU)

The clock sources of the whole system are: HSECLK, LSECLK, HSICLK, LSICLK, and PLL1. For the characteristics of the clock source, refer to the relevant chapter of "Electrical Characteristics" in the datasheet.

### 6.3.1 External clock source

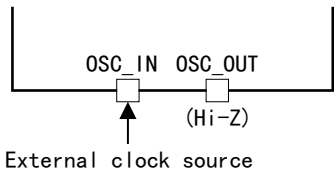
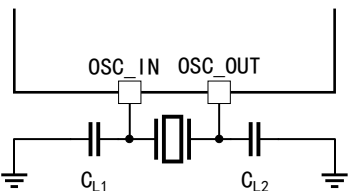
The external clock signal includes HSECLK (high-speed external clock signal) and LSECLK (low-speed external clock signal).

There are two kinds of external clock sources:

- External crystal/ceramic resonator
- External clock of user

The hardware configuration of the two kinds of clock sources is shown in the figure below.

Figure 5 HSECLK/LSECLK Clock Source Hardware Configuration

| Clock source              | Hardware configuration                                                               |
|---------------------------|--------------------------------------------------------------------------------------|
| External clock            |  |
| Crystal/ceramic resonator |  |

In order to reduce the distortion of clock output and shorten the start-up stabilization time, the crystal/ceramic resonator and load capacitor must be as close to the oscillator pin as possible. The value of load capacitance ( $C_{L1}$ ,  $C_{L2}$ ) must be adjusted according to the selected oscillator.

#### 6.3.1.1 HSECLK high-speed external clock signal

HSECLK clock signal is generated by HSECLK external crystal/ceramic resonator and HSECLK external clock two kinds of clock sources.

Table 33 Clock Source Generating HSECLK

| Name                                                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External clock source<br>(HSECLK bypass)               | <p>Provide clock to MCU through OSC_IN pin.</p> <p>The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators. The waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the maximum frequency is up to 26MHz.</p> <p>For hardware connection, it must be connected to OSC_IN pin, ensuring OSC_OUT pin is suspended (in high-impedance state). For MCU configuration, the user can select this mode by setting HSEBCFG and HSEEN bits in RCM_CTRL (clock control register).</p>                                                                                                              |
| External crystal/ceramic resonator<br>(HSECLK crystal) | <p>The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator.</p> <p>The frequency range is 4-26MHz.</p> <p>When OSC_IN and OSC_OUT are connected to a resonator, the HSEEN bit in the RCM_CTRL (Clock Control Register) can be set to enable or disable the connection.</p> <p>HSERDYFLG bit in the clock control register RCM_CTRL (clock control register) is used to indicate whether the high-speed external oscillator is stable. After startup, the clock is not released until this bit is set to "1" by hardware. If interrupt is allowed in RCM_INT (clock interrupt register), corresponding interrupt will be generated.</p> |

### 6.3.1.2 LSECLK low-speed external clock signal

LSECLK clock signal is generated by LSECLK external crystal/ceramic resonator and LSECLK external clock two kinds of clock sources.

Table 34 Clock Source Generating LSECLK

| Name                                     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External clock source<br>(LSECLK bypass) | <p>The clock is provided to MCU through OSC32_IN pin.</p> <p>The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators. The waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the signal frequency needs to be 32.768kHz.</p> <p>For hardware connection, it must be connected to OSC32_IN pin, ensuring OSC32_OUT pin is suspended. For MCU configuration, the user can select this mode by setting LSEBCFG and LSEEN bits in RCM_BDCTRL (backup domain control register).</p> |

| Name                                                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External crystal/ceramic resonator<br>(LSECLK crystal) | <p>The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency is 32.768kHz.</p> <p>When OSC32_IN and OSC32_OUT are connected to a resonator, it can be enabled or disabled by setting the LSEEN bit in the RCM_BDCTRL (Backup Domain Control Register).</p> <p>LSERDYFLG in RCM_BDCTRL indicates whether LSECLK crystal oscillator is stable. At startup stage, LSECLK clock signal is not released until this bit is set to "1" by hardware. If it is allowed in the clock interrupt register, an interrupt request can be generated.</p> |

### 6.3.2 Internal clock source

The internal clock includes HSICLK (high-speed internal clock signal) and LSICLK (low-speed internal clock signal).

#### 6.3.2.1 HSICLK high-speed internal clock signal

HSICLK clock signal is generated by internal 16MHz RC oscillator.

The RC oscillator frequency of different chips is different, and that of the same chip may be different with the change of temperature and voltage; the HSICLK clock frequency of each chip has been calibrated to 1% (25°C,  $V_{DD}=V_{DDA}=3.3V$ ) by the manufacturer before leaving the factory. When the system is reset, the value calibrated by the manufacturer will be loaded to RCM\_CTRL register; in addition, the users can further adjust the frequency by setting HSITRM bit in RCM\_CTRL register according to the actual environment (temperature and voltage).

HSIRDYFLG bit can be used to indicate whether HSICLK RC oscillator is stable. In the clock startup process, HSICLK RC output clock is not released until the HSIRDYFLG bit is set to 1 by hardware. HSICLK RC can be enabled or disabled by HSIEN bit in RCM\_CTRL.

Compared with HSECLK crystal oscillator, RC oscillator can provide system clock without any external device. The start time of RC oscillator is shorter than that of HSECLK crystal oscillator. Even after calibration, its clock frequency accuracy is still inferior to that of HSECLK crystal oscillator.

#### 6.3.2.2 LSICLK low-speed internal clock signal

##### Main characteristics of LSICLK

LSICLK is generated by RC oscillator, within the range of 28kHz (20kHz and 35kHz). The frequency may change along with the change of temperature and voltage. It can keep running in stop and standby mode and provide clock for independent watchdog and automatic wake-up unit.

LSICLK can be enabled or disabled by LSIEN bit in RCM\_CSTS register. LSIRDYFLG bit in RCM\_CSTS indicates whether the low-speed internal oscillator is stable. At startup stage, the clock is not released until this bit is set to "1" by hardware. If allowed in RCM\_INT register, LSICLK ready interrupt request signal will be generated.

### 6.3.3 PLL phase locked loop

This series of products have one PLL, which usually take HSICLK or HSECLK oscillator as their clock source.

The PLL will be disabled by hardware in case of either of the following situations:

- Enter the stop or standby state
- The system clock directly or indirectly selects HSECLK as the clock source, and a fault occurs to HSECLK

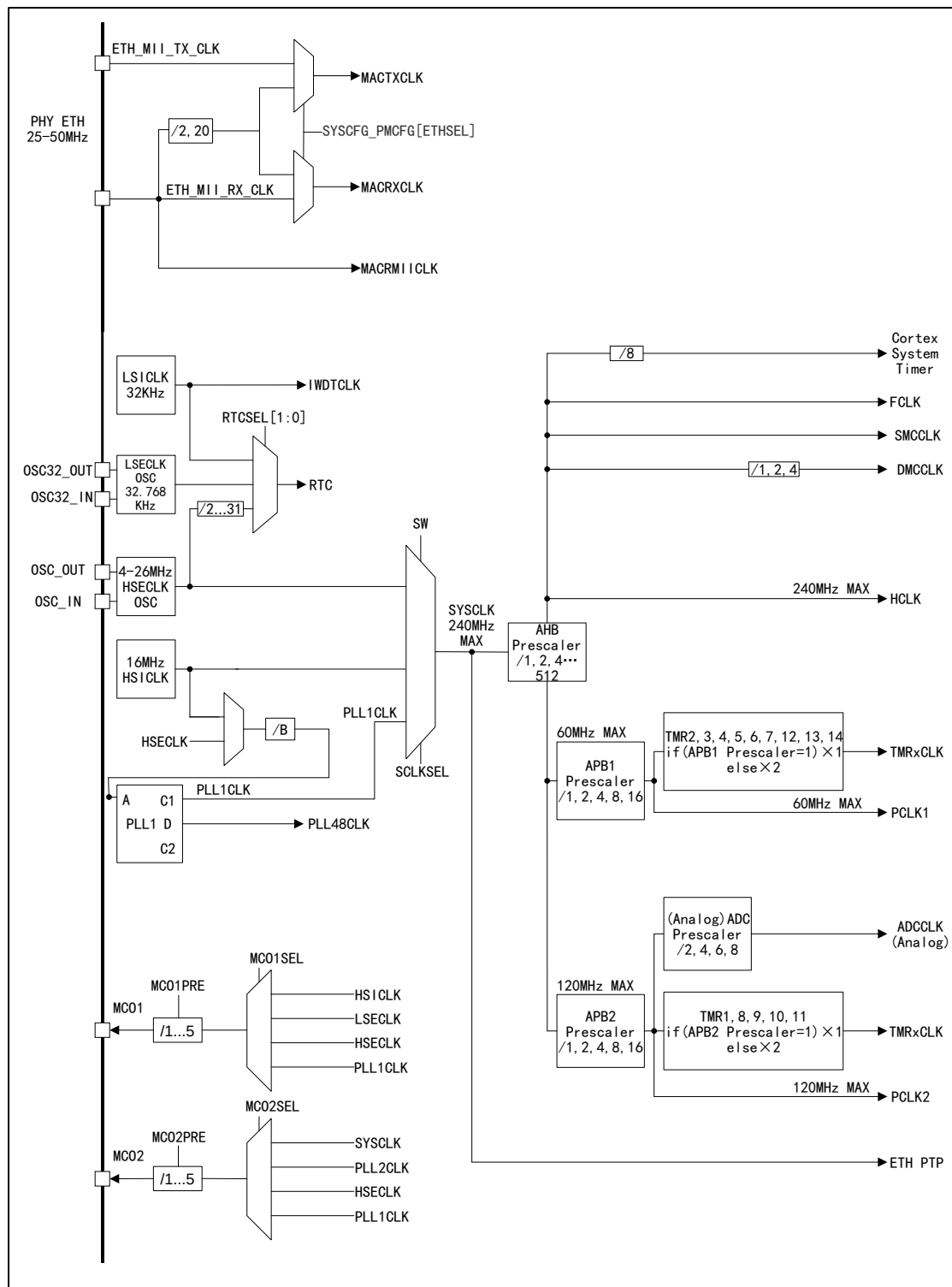
When configuring PLL related coefficient, ensure that it is not enabled.

#### 6.3.3.1 PLL1

PLL1 is the phase-locked loop, which mainly generates the clock signal with maximum frequency of 240MHz for the system clock. The clock output frequency of PLL1 is configured by RCM\_PLL1CFG register. The clock frequency is adjusted by setting the multiplication/division factor in the formula, and PLL1 shall be disabled during configuration.

### 6.3.4 Clock tree

Figure 6 APM32F425xG\_F427xG Clock Tree



Note:

- (1) HCLK means AHB clock signal.

- (2) PLCK1 and PLCK2 are clock signal connected to APB1 and APB2 respectively.
- (3) FCLK is free running clock of Arm® Cortex®-M4F with FPU.
- (4) The frequency of AHB, APB2 (high-speed APB) and APB1 (low-speed APB) domains can be configured through multiple prescalers. The maximum frequency of AHB domain is 240MHz, the maximum frequency of APB2 domain is 120MHz, and the maximum allowable frequency of APB1 is 60MHz.
- (5) The maximum frequency obtained by the system clock is 240MHz.
- (6) The clock source of OTG\_FS is PLL1CLK with frequency of 48MHz.
- (7) Only when the corresponding enable bits are set, can the peripheral obtain the clock signal.
- (8) ADC clock can be divided into analog circuit clock and digital circuit clock. The clock management unit provides a prescaler for the analog circuit clock of ADC, so that the ADC can work at the clock frequency of PCLK2 after 2/4/6/8 frequency division, and at this time the clock can be used by all ADC. The clock frequency of digital circuit of ADC is equal to PCLK2, and ADC1/2/3 clocks can be enabled respectively through the corresponding bits of RCM\_APB2CLKEN register.
- (9) SysTick (system timer) can be provided by the clock signal after frequency division of HCLK8. Different clock sources can be selected by setting SysTick control and status register.
- (10) Frequency of all TMRxCLK (timer clocks) is automatically set by the hardware according to the following two situations:
  - If the corresponding APB prescaler factor is 1, the clock frequency of the timer is the same as that of the APB bus.
  - If the corresponding APB prescaler factor is 2-16, the clock frequency of the timer will be set to twice the frequency of the APB bus connected to it.
- (11) The maximum output frequency of MCO1/2 is 100MHz.
- (12) For the structure of PLL1, refer to PLL Phase Locked Loop and PLLx configuration registers.

### 6.3.5 Clock source selection of RTC

By setting RTCSRCSEL bit in RCM\_BDCTRL (backup domain control register), you can select to divide the frequency of HSECLK into 1MHz clock signal, and use LSECLK or LSICLK as the clock source of RTC. The selection of clock source can be changed only when the backup domain is reset.

Because LSECLK is in the backup domain, and HSECLK and LSICLK are not in the backup domain, so RTC working conditions are different when selecting different clock sources as RTC clock. See the following table for details:



Table 35 Working Condition of RTC When Different Clock Sources are Selected

| Clock source                                         | Working condition                                                                                                                                                                                                                                                               |
|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LSECLK is selected as RTC clock                      | As long as $V_{BAT}$ maintains power supply, RTC will continue to work even if $V_{DD}$ is powered off.                                                                                                                                                                         |
| LSICLK is selected as automatic wake-up unit clock   | If $V_{DD}$ is powered off, the automatic wake-up unit state cannot be guaranteed.                                                                                                                                                                                              |
| HSECLK is used as RTC clock after frequency division | If the $V_{DD}$ is powered off or the internal voltage regulator is disabled (the power supply of 1.2V domain is cut off), the RTC state is uncertain, so the BPWEN bit (cancel the write protection of backup domain) of PMU_CTRL (power control register) must be set to "1". |

### 6.3.6 Clock source selection of IWDT

When IWDT (independent watchdog) is opened, LSICLK oscillator will be opened by force, and when it is stable, the clock signal will be provided to IWDT. After LSICLK is opened by force, it will always be open and cannot be closed.

### 6.3.7 Clock source selection of MCO

There are two microcontroller clock output pins, MCO1 (PA8) and MCO2 (PC9). When the corresponding GPIO ports of ports (PA8 and PC9) are configured as the corresponding multiplexing function, the clock signal can be selected to be output to MCO pin by configuring MCOxSEL bit and MCOxPSC bit in RCM\_CFG (clock configuration register). See the clock tree or register functional description for specific clock signal.

### 6.3.8 Clock source selection of SYSCLK

After system reset, HSICLK oscillator will (directly or indirectly) be selected as the system clock, and cannot be stopped. If you want to switch the SYSCLK clock source, you must wait until the destination clock source is ready (that is, the destination clock source is stable). The target clock source can be HSICLK, HSECLK and PLLCLK.

The state bit of RCM\_CTRL and RCM\_CFG registers can indicate the ready clock and selected SYSCLK clock source.

### 6.3.9 CSS clock security system

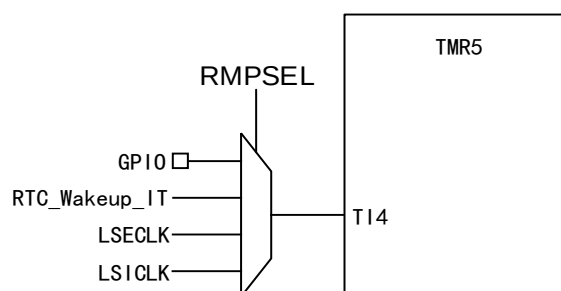
In order to prevent MCU from normal operation due to external crystal oscillator short circuit, MCU can activate CSS clock security system through software. After the security system is activated, if the HSECLK oscillator is used as the system clock directly or indirectly (used as the PLL input clock and PLL is used as the system clock), the external HSECLK oscillator will be disabled when the HSECLK fails, and the system clock will automatically switch to HSICLK. At this time, the PLLCLK which selects HSECLK as the clock input and as the system clock input source will also be disabled.

Note: When CSS is activated by software and HSECLK fails, CSS interrupt and NMI (non-maskable interrupt) will be generated. Since NMI is executed continuously before CSS interrupt is cleared, CSSCLR bit in RCM\_INT register shall be set to clear the interrupt.

### 6.3.10 TMR5-based internal/external clock measurement

Through the input capture function of TMR5 Channel 4, the frequency of certain clock source generators can be indirectly measured. The circuit diagram is as follows:

Figure 7 TMR5 Measurement Clock Frequency Circuit Diagram

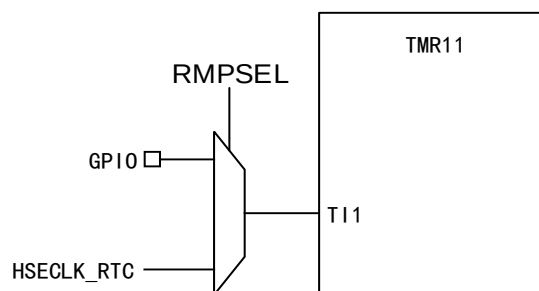


Channel 4 of TMR5 can select to connect one GPIO port or one MCU internal clock by configuring RMPSEL bit of TMR5\_OPT register.

### 6.3.11 TMR11-based internal/external clock measurement

The external oscillator frequency can be tested through TMR11 when HSECLK is used as the system clock source. As shown in the figure below, the user can select to trigger T11 by I/O port or internal clock by configuring the RMPSEL bit of TMR11\_OPT register.

Figure 8 TMR11 Measurement Clock Frequency Circuit Diagram



## 6.4 Register address mapping

Table 36 RCM Register Address Mapping

| Register name | Description                  | Offset address |
|---------------|------------------------------|----------------|
| RCM_CTRL      | Clock control register       | 0x00           |
| RCM_PLL1CFG   | PLL1 configuration register  | 0x04           |
| RCM_CFG       | Clock configuration register | 0x08           |

| Register name   | Description                                             | Offset address |
|-----------------|---------------------------------------------------------|----------------|
| RCM_INT         | Clock interrupt register                                | 0x0C           |
| RCM_AHB1RST     | AHB1 peripheral reset register                          | 0x10           |
| RCM_AHB2RST     | AHB2 peripheral reset register                          | 0x14           |
| RCM_AHB3RST     | AHB3 peripheral reset register                          | 0x18           |
| RCM_APB1RST     | APB1 peripheral reset register                          | 0x20           |
| RCM_APB2RST     | APB2 peripheral reset register                          | 0x24           |
| RCM_AHB1CLKEN   | AHB1 peripheral clock enable register                   | 0x30           |
| RCM_AHB2CLKEN   | AHB2 peripheral clock enable register                   | 0x34           |
| RCM_AHB3CLKEN   | AHB3 peripheral clock enable register                   | 0x38           |
| RCM_APB1CLKEN   | APB1 peripheral clock enable register                   | 0x40           |
| RCM_APB2CLKEN   | APB2 peripheral clock enable register                   | 0x44           |
| RCM_LPAHB1CLKEN | AHB1 peripheral clock enable register in low-power mode | 0x50           |
| RCM_LPAHB2CLKEN | AHB2 peripheral clock enable register in low-power mode | 0x54           |
| RCM_LPAHB3CLKEN | AHB3 peripheral clock enable register in low-power mode | 0x58           |
| RCM_LPAPB1CLKEN | APB1 peripheral clock enable register in low-power mode | 0x60           |
| RCM_LPAPB2CLKEN | APB2 peripheral clock enable register in low-power mode | 0x64           |
| RCM_BDCTRL      | Backup domain control register                          | 0x70           |
| RCM_CSTS        | Clock control/state register                            | 0x74           |
| RCM_SSCCFG      | Spread spectrum clock configuration register            | 0x80           |

## 6.5 Register functional description

### 6.5.1 Clock control register (RCM\_CTRL)

Offset address: 0x00

Reset value: 0x0000 XX83; X means undefined

Access: Access in the form of word, half word and byte, without wait cycle

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | HSIEN     | R/W | <p>High Speed Internal Clock Enable</p> <p>Set to 1 or cleared by software.</p> <p>HSICLK is an RC oscillator. When one of the following conditions occurs, it will be set to 1 by the hardware: power-on start, software reset, wake-up from standby mode, wake-up from stop mode, failure of external high-speed clock source (as system clock or providing system clock through PLL). When HSICLK is used as system clock or provides system clock through PLL, this bit cannot be cleared.</p> <p>0: HSICLK RC oscillator is disabled</p> <p>1: HSICLK RC oscillator is turned on</p> |
| 1     | HSIRDYFLG | R   | <p>High Speed Internal Clock Ready Flag</p> <p>0: HSICLK RC oscillator is not stable</p> <p>1: HSICLK RC oscillator is stable</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2     | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7:3   | HSITRM    | R/W | <p>High Speed Internal Clock Trim</p> <p>HSICLK has been calibrated to 16MHz±1% when the product leaves the factory. However, it changes as the temperature and voltage changes, but the frequency of HSICLK RC oscillator can be adjusted by this bit.</p>                                                                                                                                                                                                                                                                                                                               |
| 15:8  | HSICAL    | R   | <p>High Speed Internal Clock Calibrate</p> <p>HSICLK has been calibrated to 16MHz±1% when the product leaves the factory. When the system is started up, the calibration parameters will be automatically written to the register.</p>                                                                                                                                                                                                                                                                                                                                                    |
| 16    | HSEEN     | R/W | <p>High Speed External Clock Enable</p> <p>When entering the standby or stop mode, this bit is cleared by hardware and HSECLK is turned off. When HSECLK is used as system clock source or the system clock is provided through PLL, this bit cannot be cleared.</p> <p>0: Disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                   |
| 17    | HSERDYFLG | R   | <p>High Speed External Clock Ready Flag</p> <p>When HSECLK is stable, this bit will be set to 1 by hardware and set to 0 by software.</p> <p>0: HSECLK is not stable</p> <p>1: HSECLK is stable</p>                                                                                                                                                                                                                                                                                                                                                                                       |
| 18    | HSEBCFG   | R/W | <p>High Speed External Clock Bypass Configure</p> <p>Bypass mode refers to the mode in which external clock is used as the HSECLK clock source; otherwise the resonator is used as the HSECLK clock source.</p> <p>0: Non-bypass mode</p> <p>1: Bypass mode</p>                                                                                                                                                                                                                                                                                                                           |
| 19    | CSSSEN    | R/W | <p>Clock Security System Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>Note: This bit can be set to 1 only when HSECLK resonator is stable.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 23:20 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                         |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | PLL1EN     | R/W | <p>PLL1 Enable</p> <p>When entering the standby and stop mode, this bit is cleared to 0 by the hardware; when PLL1CLK has been configured as the clock source of the system clock (or in the process of configuration), this bit cannot be set to 0; in other cases, it can be set to 1 or 0 by the software.</p> <p>0: PLL1 is disabled<br/>1: PLL1 is enabled</p> |
| 25    | PLL1RDYFLG | R   | <p>PLL1 Clock Ready Flag</p> <p>PLL1 is set to 1 by hardware after it is locked.</p> <p>0: PLL1 is unlocked<br/>1: PLL1 is locked</p>                                                                                                                                                                                                                               |
| 31:26 | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                     |

### 6.5.2 PLL1 configuration register (RCM\_PLL1CFG)

Offset address: 0x04

Reset value: 0x2400 3010

Access in the form of word, half word and byte, without wait cycle.

The register is used to configure various parameters so as to output different clock signals.

$$f_{(VCO\ clock)} = f_{(PLL1\ clock\ input)} \times (PLL1A/PLL1B)$$

$$f_{(PLL1\ clock\ output)} = f_{(VCO\ clock)} / PLL1C$$

$$f_{(OTG\_FS, SDIO, RNG\ clock\ output)} = f_{(VCO\ clock)} / PLL1D$$

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0   | PLL1B | R/W | <p>Division Factor B</p> <p>It is used to calculate the clock frequency of VCO. These bits can be written only when PLL is disabled.</p> <p>000000: PLLB=0 (error)<br/>000001: PLLB=1 (error)<br/>000010: PLLB=2<br/>000011: PLLB=3<br/>.....<br/>111110: PLLB=62<br/>111111: PLLB=63</p>                                                                                                                                                         |
| 14:6  | PLL1A | R/W | <p>PLL Multiplication Factor A</p> <p>It is used to calculate VCO frequency. The calculation formula is <math>f_{(VCO\ output)} = f_{(VCO\ input)} \times PLL1A</math>, and the formula is established only when PLL1A is 50~432.</p> <p>000000000: PLLA=0 (error)<br/>000000001: PLLA=1 (error)<br/>.....<br/>000110010: PLLA=50<br/>.....<br/>110110000: PLLA=432<br/>110110001: PLLA=433 (error)<br/>.....<br/>111111111: PLLA=511 (error)</p> |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                           |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | Reserved |     |                                                                                                                                                                                                                                                       |
| 17:16 | PLL1C    | R/W | Division Factor C<br>It is used to calculate the output clock frequency of PLL1.<br>00: PLL1C=2<br>01: PLL1C=4<br>10: PLL1C=6<br>11: PLL1C=8<br>Note: This bit can be written only when PLL1 is disabled.                                             |
| 21:18 | Reserved |     |                                                                                                                                                                                                                                                       |
| 22    | PLLCLKS  | R/W | PLL Clock Source<br>This bit can be set or cleared by software and be used to select the clock source of PLL1.<br>0: HSICLK is used as clock source<br>1: HSECLK is used as clock source<br>Note: This bit can be written only when PLL1 is disabled. |
| 23    | Reserved |     |                                                                                                                                                                                                                                                       |
| 27:24 | PLLD     | R/W | Division Factor<br>It is used to calculate the clock frequency of OTG_FS, RNG and SDIO.<br>0000: PLLD=0 (error)<br>0001: PLLD=1 (error)<br>0010: PLLD=2<br>0011: PLLD=3<br>0100: PLLD=4<br>.....<br>1111: PLLD=15                                     |
| 31:28 | Reserved |     |                                                                                                                                                                                                                                                       |

### 6.5.3 Clock configuration register (RCM\_CFG)

Offset address: 0x08

Reset value: 0x0000 0000

All bits of this register are set or cleared by software.

Access: Access in the form of word, half word and byte, with 0 to 2 wait cycles.

1 or 2 wait cycles are inserted only when the access occurs during clock switching.

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                                     |
|-------|---------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | SCLKSEL | R/W | System Clock Source Select<br>When returning from stop or standby mode or the HSECLK directly or indirectly used as system clock fails, the hardware selects HSICLK as system clock by force (if the clock security system has been started)<br>00: HSICLK is used as system clock<br>01: HSECLK is used as system clock<br>10: PLL1CLK is used as system clock<br>11: Reserved |

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:2   | SCLKSELSTS | R   | <p>System Clock Selection Status</p> <p>Indicate which clock source is used as system clock. Set to 1 or cleared by the hardware.</p> <p>00: HSICLK is used as system clock</p> <p>01: HSECLK is used as system clock</p> <p>10: PLL1CLK output is used as system clock</p> <p>11: Not use</p>                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:4   | AHBPSC     | R/W | <p>AHB Clock Prescaler Factor Configure</p> <p>Control the prescaler factor of AHB clock.</p> <p>0xxx: No frequency division for SYSCLK</p> <p>1000: SYSCLK 2-divided frequency</p> <p>1001: SYSCLK 4-divided frequency</p> <p>1010: SYSCLK 8-divided frequency</p> <p>1011: SYSCLK 16-divided frequency</p> <p>1100: SYSCLK 64-divided frequency</p> <p>1101: SYSCLK 128-divided frequency</p> <p>1110: SYSCLK 256-divided frequency</p> <p>1111: SYSCLK 512-divided frequency</p> <p>Note: Only after 1 to 16 AHB clock cycles after this bit is written, can the frequency of the clock signal be divided according to the new division factor. When Ethernet is used, HCLK cannot be less than 25MHz.</p> |
| 9:8   | SDRAMPSC   | R/W | <p>SDRAM Clock Prescaler Factor Configure</p> <p>Configure the prescaler factor of SDRAM clock.</p> <p>00: No frequency division <math>f_{SDRAM}=f_{DMC}</math></p> <p>01: 2-divided frequency <math>f_{SDRAM}=f_{DMC}/2</math></p> <p>Others: 4-divided frequency <math>f_{SDRAM}=f_{DMC}/4</math></p>                                                                                                                                                                                                                                                                                                                                                                                                       |
| 12:10 | APB1PSC    | R/W | <p>APB1 Clock Prescaler Factor Configure</p> <p>Prescaler factor used to control low-speed APB1 clock (PCLK1).</p> <p>0xx: No frequency division for HCLK</p> <p>100: HCLK 2-divided frequency</p> <p>101: HCLK 4-divided frequency</p> <p>110: HCLK 8-divided frequency</p> <p>111: HCLK 16-divided frequency</p> <p>Note: PCLK1 shall not be greater than 60MHz.</p>                                                                                                                                                                                                                                                                                                                                        |
| 15:13 | APB2PSC    | R/W | <p>APB2 Clock Prescaler Factor Configure</p> <p>Prescaler factor used to control low-speed APB2 clock (PCLK2).</p> <p>0xx: No frequency division for HCLK</p> <p>100: HCLK 2-divided frequency</p> <p>101: HCLK 4-divided frequency</p> <p>110: HCLK 8-divided frequency</p> <p>111: HCLK 16-divided frequency</p> <p>Note: PCLK2 shall not be greater than 120MHz.</p>                                                                                                                                                                                                                                                                                                                                       |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20:16 | RTCPSC   | R/W | RTC Clock Prescaler Factor Configure<br>Control the prescaler factor, to make HSECLK frequency division to generate a 1MHz clock signal and provide it to RTC.<br>0000X: No clock<br>00010: HSECLK2 frequency division<br>00011: HSECLK3 frequency division<br>00100: HSECLK4 frequency division<br>.....<br>11110: HSECLK30 frequency division<br>11111: HSECLK31 frequency division<br>Note: This bit must be configured before RTC selects HSECLK as the clock source. |
| 22:21 | MCO1SEL  | R/W | Main Clock Output1 Select<br>Set or cleared by software.<br>00: HSICLK is output as a clock<br>01: LSECLK is output as a clock<br>10: HSECLK is output as a clock<br>11: PLL1CLK is output as a clock                                                                                                                                                                                                                                                                     |
| 23    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 26:24 | MCO1PSC  | R/W | MCO Clock Output1 Prescaler Factor Configure<br>0XX: No frequency division<br>100: 2 divided frequency<br>101: 3 divided frequency<br>110: 4 divided frequency<br>111: 5 divided frequency                                                                                                                                                                                                                                                                                |
| 29:27 | MCO2PSC  | R/W | MCO Clock Output2 Prescaler Factor Configure<br>0XX: No frequency division<br>100: 2 divided frequency<br>101: 3 divided frequency<br>110: 4 divided frequency<br>111: 5 divided frequency                                                                                                                                                                                                                                                                                |
| 31:30 | MCO2SEL  | R/W | Main Clock Output2 Select<br>00: SYSCLK is output as a clock<br>01: Reserved<br>10: HSECLK is output as a clock<br>11: PLL1CLK is output as a clock                                                                                                                                                                                                                                                                                                                       |

## 6.5.4 Clock interrupt register (RCM\_INT)

Offset address: 0x0C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wai cycle.



| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | LSIRDYFLG  | R   | <p>LSICLK Ready Interrupt Flag</p> <p>When LSICLK is stable and LSIRDYEN bit is set to 1, this bit will be set to 1 by hardware; when LSIRDYCLR is set to 1 by software, this bit will be cleared.</p> <p>0: No LSICLK ready interrupt<br/>1: LSICLK ready interrupt occurred</p>                                                                  |
| 1     | LSELDYFLG  | R   | <p>LSECLK Ready Interrupt Flag</p> <p>When LSECLK is stable and LSELDYEN bit is set to 1, this bit will be set to 1 by hardware; when LSELDYCLR is set to 1 by software, this bit will be cleared.</p> <p>0: No LSECLK ready interrupt<br/>1: LSECLK ready interrupt occurred</p>                                                                  |
| 2     | HSIRDYFLG  | R   | <p>HSICLK Ready Interrupt Flag</p> <p>When HSICLK is stable and HSIRDYEN bit is set to 1, this bit will be set to 1 by hardware; when HSIRDYCLR is set to 1 by software, this bit will be cleared.</p> <p>0: No HSICLK ready interrupt<br/>1: HSICLK ready interrupt occurred</p>                                                                  |
| 3     | HSELDYFLG  | R   | <p>HSECLK Ready Interrupt Flag</p> <p>When HSECLK is stable and HSELDYEN bit is set to 1, this bit will be set to 1 by hardware; when HSELDYCLR is set to 1 by software, this bit will be cleared.</p> <p>0: No HSECLK ready interrupt<br/>1: HSECLK ready interrupt occurred</p>                                                                  |
| 4     | PLL1RDYFLG | R   | <p>PLL1 Ready Interrupt Flag</p> <p>When PLL1 is stable and PLL1RDYEN bit is set to 1, this bit will be set to 1 by hardware; when PLL1RDYCLR is set to 1 by software, this bit will be cleared.</p> <p>0: PLL1 clock ready interrupt does not occur<br/>1: PLL1 clock ready interrupt occurred</p>                                                |
| 6:5   | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                    |
| 7     | CSSFLG     | R   | <p>Clock Security System Interrupt Flag</p> <p>When the external high-speed oscillator clock fails, it is set to 1 by hardware.</p> <p>When CSSCLR is set to 1 by software, this bit will be cleared.</p> <p>0: No security system interrupt caused by HSE clock failure<br/>1: Clock security system interrupt is caused by HSE clock failure</p> |
| 8     | LSIRDYEN   | R/W | <p>LSICLK Ready Interrupt Enable</p> <p>Enable or disable internal 28kHz RC oscillator ready interrupt.</p> <p>0: Disable<br/>1: Enable</p>                                                                                                                                                                                                        |
| 9     | LSELDYEN   | R/W | <p>LSECLK Ready Interrupt Enable</p> <p>Enable external 32kHz RC oscillator ready interrupt.</p> <p>0: Disable<br/>1: Enable</p>                                                                                                                                                                                                                   |

| Field | Name       | R/W | Description                                                                                                               |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------|
| 10    | HSIRDYEN   | R/W | HSICLK Ready Interrupt Enable<br>Enable the internal 8MHz RC oscillator ready interrupt.<br>0: Disable<br>1: Enable       |
| 11    | HSERDYEN   | R/W | HSCLKE Ready Interrupt Enable<br>Enable external 4-16MHz oscillator ready interrupt.<br>0: Disable<br>1: Enable           |
| 12    | PLL1RDYEN  | R/W | PLL1 Ready Interrupt Enable<br>Enable PLL1 ready interrupt.<br>0: Disable<br>1: Enable                                    |
| 15:13 | Reserved   |     |                                                                                                                           |
| 16    | LSIRDYCLR  | W   | LSICLK Ready Interrupt Clear<br>Clear LSI ready interrupt flag bit LSIRDYFLG.<br>0: No effect<br>1: Clear                 |
| 17    | LSERDYCLR  | W   | LSECLK Ready Interrupt Clear<br>Clear LSE ready interrupt flag bit LSERDYFLG.<br>0: No effect<br>1: Clear                 |
| 18    | HSIRDYCLR  | W   | HSICLK Ready Interrupt Clear<br>Clear HSI ready interrupt flag bit HSIRDYFLG.<br>0: No effect<br>1: Clear                 |
| 19    | HSERDYCLR  | W   | HSECLK Ready Interrupt Clear<br>Clear HSE ready interrupt flag bit HSERDYFLG.<br>0: No effect<br>1: Clear                 |
| 20    | PLL1RDYCLR | W   | PLL1 Ready Interrupt Clear<br>Clear PLL1 ready interrupt flag bit PLL1RDYFLG.<br>0: No effect<br>1: Clear                 |
| 22:21 | Reserved   |     |                                                                                                                           |
| 23    | CSSCLR     | W   | Clock Security System Interrupt Clear<br>Clear the security system interrupt flag bit CSSFLG.<br>0: No effect<br>1: Clear |
| 31:24 | Reserved   |     |                                                                                                                           |

### 6.5.5 AHB1 peripheral reset register (RCM\_AHB1RST)

Offset address: 0x10

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

| Field | Name      | R/W | Description                                |
|-------|-----------|-----|--------------------------------------------|
| 0     | PARST     | R/W | GPIOA Reset<br>0: No effect<br>1: Reset    |
| 1     | PBRST     | R/W | GPIOB Reset<br>0: No effect<br>1: Reset    |
| 2     | PCRST     | R/W | GPIOC Reset<br>0: No effect<br>1: Reset    |
| 3     | PDRST     | R/W | GIOD Reset<br>0: No effect<br>1: Reset     |
| 4     | PERST     | R/W | GPIOE Reset<br>0: No effect<br>1: Reset    |
| 5     | PFRST     | R/W | GPIOF Reset<br>0: No effect<br>1: Reset    |
| 6     | PGRST     | R/W | GPIOG Reset<br>0: No effect<br>1: Reset    |
| 7     | PHRST     | R/W | GPIOH Reset<br>0: No effect<br>1: Reset    |
| 11:8  | Reserved  |     |                                            |
| 12    | CRCRST    | R/W | CRC Reset<br>0: No effect<br>1: Reset      |
| 20:13 | Reserved  |     |                                            |
| 21    | DMA1RST   | R/W | DMA1 Reset<br>0: No effect<br>1: Reset     |
| 22    | DMA2RST   | R/W | DMA2 Reset<br>0: No effect<br>1: Reset ADC |
| 24:23 | Reserved  |     |                                            |
| 25    | ETHRST    | R/W | ETH Reset<br>0: No effect<br>1: Reset      |
| 28:26 | Reserved  |     |                                            |
| 29    | OTGFS2RST | R/W | OTG_FS2 Reset<br>0: No effect<br>1: Reset  |

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 31:30 | Reserved |     |             |

### 6.5.6 AHB2 peripheral reset register (RCM\_AHB2RST)

Offset address: 0x14

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

| Field | Name     | R/W | Description                              |
|-------|----------|-----|------------------------------------------|
| 5:0   | Reserved |     |                                          |
| 6     | RNGRST   | R/W | RNG Reset<br>0: No effect<br>1: Reset    |
| 7     | OTGFSRST | R/W | OTG_FS Reset<br>0: No effect<br>1: Reset |
| 31:8  | Reserved |     |                                          |

### 6.5.7 AHB3 peripheral reset register (RCM\_AHB3RST)

Offset address: 0x18

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

| Field | Name     | R/W | Description                            |
|-------|----------|-----|----------------------------------------|
| 0     | EMMCRST  | R/W | EMMC Reset<br>0: No effect<br>1: Reset |
| 1     | QSPIRST  | R/W | QSPI Reset<br>0: No effect<br>1: Reset |
| 31:2  | Reserved |     |                                        |

### 6.5.8 APB1 peripheral reset register (RCM\_APB1RST)

Offset address: 0x20

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

| Field | Name    | R/W | Description                            |
|-------|---------|-----|----------------------------------------|
| 0     | TMR2RST | R/W | TMR2 Reset<br>0: No effect<br>1: Reset |
| 1     | TMR3RST | R/W | TMR3 Reset<br>0: No effect<br>1: Reset |

| Field | Name      | R/W | Description                               |
|-------|-----------|-----|-------------------------------------------|
| 2     | TMR4RST   | R/W | TMR4 Reset<br>0: No effect<br>1: Reset    |
| 3     | TMR5RST   | R/W | TMR5 Reset<br>0: No effect<br>1: Reset    |
| 4     | TMR6RST   | R/W | TMR6 Reset<br>0: No effect<br>1: Reset    |
| 5     | TMR7RST   | R/W | TMR7 Reset<br>0: No effect<br>1: Reset    |
| 6     | TMR12RST  | R/W | TMR12 Reset<br>0: No effect<br>1: Reset   |
| 7     | TMR13RST  | R/W | TMR13 Reset<br>0: No effect<br>1: Reset   |
| 8     | TMR14RST  | R/W | TMR14 Reset<br>0: No effect<br>1: Reset   |
| 10:9  | Reserved  |     |                                           |
| 11    | WWDTRST   | R/W | WWDTRST Reset<br>0: No effect<br>1: Reset |
| 13:12 | Reserved  |     |                                           |
| 14    | SPI2RST   | R/W | SPI2 Reset<br>0: No effect<br>1: Reset    |
| 15    | SPI3RST   | R/W | SPI3 Reset<br>0: No effect<br>1: Reset    |
| 16    | Reserved  |     |                                           |
| 17    | USART2RST | R/W | USART2 Reset<br>0: No effect<br>1: Reset  |
| 18    | USART3RST | R/W | USART3 Reset<br>0: No effect<br>1: Reset  |
| 19    | UART4RST  | R/W | UART4 Reset<br>0: No effect<br>1: Reset   |

| Field | Name     | R/W | Description                                     |
|-------|----------|-----|-------------------------------------------------|
| 20    | UART5RST | R/W | UART5 Reset<br>0: No effect<br>1: Reset         |
| 21    | I2C1RST  | R/W | I2C1 Reset<br>0: No effect<br>1: Reset          |
| 22    | I2C2RST  | R/W | I2C2 Reset<br>0: No effect<br>1: Reset          |
| 23    | I2C3RST  | R/W | I2C3 Reset<br>0: No effect<br>1: Reset          |
| 24    | Reserved |     |                                                 |
| 25    | CAN1RST  | R/W | CAN1 Reset<br>0: No effect<br>1: Reset          |
| 26    | CAN2RST  | R/W | CAN2 Reset<br>0: No effect<br>1: Reset          |
| 27    | Reserved |     |                                                 |
| 28    | PMURST   | R/W | Power Clock Reset<br>0: No effect<br>1: Reset   |
| 29    | DACRST   | R/W | DAC Interface Reset<br>0: No effect<br>1: Reset |
| 31:30 | Reserved |     |                                                 |

### 6.5.9 APB2 peripheral reset register (RCM\_APB2RST)

Offset address: 0x24

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

| Field | Name     | R/W | Description                            |
|-------|----------|-----|----------------------------------------|
| 0     | TMR1RST  | R/W | TMR1 Reset<br>0: No effect<br>1: Reset |
| 1     | TMR8RST  | R/W | TMR8 Reset<br>0: No effect<br>1: Reset |
| 3:2   | Reserved |     |                                        |

| Field | Name      | R/W | Description                                                                            |
|-------|-----------|-----|----------------------------------------------------------------------------------------|
| 4     | USART1RST | R/W | USART1 Reset<br>0: No effect<br>1: Reset                                               |
| 5     | USART6RST | R/W | USART6 Reset<br>0: No effect<br>1: Reset                                               |
| 7:6   | Reserved  |     |                                                                                        |
| 8     | ADCRST    | R/W | ADC Interface Reset<br>0: No effect<br>1: Reset<br>Note: It takes effect for all ADCs. |
| 10:9  | Reserved  |     |                                                                                        |
| 11    | SDIORST   | R/W | SDIO Reset<br>0: No effect<br>1: Reset                                                 |
| 12    | SPI1RST   | R/W | SPI1 Reset<br>0: No effect<br>1: Reset                                                 |
| 13    | Reserved  |     |                                                                                        |
| 14    | SYSCFGRST | R/W | SYSCFG Module Reset<br>0: No effect<br>1: Reset                                        |
| 15    | Reserved  |     |                                                                                        |
| 16    | TMR9RST   | R/W | TMR9 Reset<br>0: No effect<br>1: Reset                                                 |
| 17    | TMR10RST  | R/W | TMR10 Reset<br>0: No effect<br>1: Reset                                                |
| 18    | TMR11RST  | R/W | TMR11 Reset<br>0: No effect<br>1: Reset                                                |
| 31:19 | Reserved  |     |                                                                                        |

#### 6.5.10 AHB1 peripheral clock enable register (RCM\_AHB1CLKEN)

Offset address: 0x30

Reset value: 0x0010 0000

Access: Access in the form of word, half word and byte, without wait cycle.

| Field | Name | R/W | Description                                   |
|-------|------|-----|-----------------------------------------------|
| 0     | PAEN | R/W | GPIOA Clock Enable<br>0: Disable<br>1: Enable |

| Field | Name       | R/W | Description                                                       |
|-------|------------|-----|-------------------------------------------------------------------|
| 1     | PBEN       | R/W | GPIOB Clock Enable<br>0: Disable<br>1: Enable                     |
| 2     | PCEN       | R/W | GPIOC Clock Enable<br>0: Disable<br>1: Enable                     |
| 3     | PDEN       | R/W | GIPIOD Clock Enable<br>0: Disable<br>1: Enable                    |
| 4     | PEEN       | R/W | GPIOE Clock Enable<br>0: Disable<br>1: Enable                     |
| 5     | PFEN       | R/W | GPIOF Clock Enable<br>0: Disable<br>1: Enable                     |
| 6     | PGEN       | R/W | GPIOG Clock Enable<br>0: Disable<br>1: Enable                     |
| 7     | PHEN       | R/W | GPIOH Clock Enable<br>0: Disable<br>1: Enable                     |
| 11:8  | Reserved   |     |                                                                   |
| 12    | CRCEN      | R/W | CRC Clock Enable<br>0: Disable<br>1: Enable                       |
| 17:13 | Reserved   |     |                                                                   |
| 18    | BAKPSRAMEN | R/W | Backup SRAM Interface Clock Enable<br>0: Disable<br>1: Enable     |
| 19    | Reserved   |     |                                                                   |
| 20    | DRAMEN     | R/W | Clock Management Data RAM Clock Enable<br>0: Disable<br>1: Enable |
| 21    | DMA1EN     | R/W | DMA1 Clock Enable<br>0: Disable<br>1: Enable                      |
| 22    | DMA2EN     | R/W | DMA2 Clock Enable<br>0: Disable<br>1: Enable                      |
| 24:23 | Reserved   |     |                                                                   |
| 25    | ETHEN      | R/W | ETH Clock Enable<br>0: Disable<br>1: Enable                       |



| Field | Name     | R/W | Description                                              |
|-------|----------|-----|----------------------------------------------------------|
| 26    | ETHTXEN  | R/W | ETH Transmission Clock Enable<br>0: Disable<br>1: Enable |
| 27    | ETHRXEN  | R/W | ETH Reception Clock Enable<br>0: Disable<br>1: Enable    |
| 28    | ETHPTPEN | R/W | ETH PTP Clock Enable<br>0: Disable<br>1: Enable          |
| 29    | OTGFS2EN | R/W | OTG_FS2 Clock Enable<br>0: Disable<br>1: Enable          |
| 31:30 | Reserved |     |                                                          |

#### 6.5.11 AHB2 peripheral clock enable register (RCM\_AHB2CLKEN)

Offset address: 0x34

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

| Field | Name     | R/W | Description                                    |
|-------|----------|-----|------------------------------------------------|
| 5:0   | Reserved |     |                                                |
| 6     | RNGEN    | R/W | RNG Clock Enable<br>0: Disable<br>1: Enable    |
| 7     | OTGFSEN  | R/W | OTG_FS Clock Enable<br>0: Disable<br>1: Enable |
| 31:8  | Reserved |     |                                                |

#### 6.5.12 AHB3 peripheral clock enable register (RCM\_AHB3CLKEN)

Offset address: 0x38

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

| Field | Name     | R/W | Description                                  |
|-------|----------|-----|----------------------------------------------|
| 0     | EMMCEN   | R/W | EMMC Clock Enable<br>0: Disable<br>1: Enable |
| 1     | QSPIEN   | R/W | QSPI Clock Enable<br>0: Disable<br>1: Enable |
| 31:2  | Reserved |     |                                              |

#### 6.5.13 APB1 peripheral clock enable register (RCM\_APB1CLKEN)

Offset address: 0x40

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

| Field | Name     | R/W | Description                                   |
|-------|----------|-----|-----------------------------------------------|
| 0     | TMR2EN   | R/W | TMR2 Clock Enable<br>0: Disable<br>1: Enable  |
| 1     | TMR3EN   | R/W | TMR3 Clock Enable<br>0: Disable<br>1: Enable  |
| 2     | TMR4EN   | R/W | TMR4 Clock Enable<br>0: Disable<br>1: Enable  |
| 3     | TMR5EN   | R/W | TMR5 Clock Enable<br>0: Disable<br>1: Enable  |
| 4     | TMR6EN   | R/W | TMR6 Clock Enable<br>0: Disable<br>1: Enable  |
| 5     | TMR7EN   | R/W | TMR7 Clock Enable<br>0: Disable<br>1: Enable  |
| 6     | TMR12EN  | R/W | TMR12 Clock Enable<br>0: Disable<br>1: Enable |
| 7     | TMR13EN  | R/W | TMR13 Clock Enable<br>0: Disable<br>1: Enable |
| 8     | TMR14EN  | R/W | TMR14 Clock Enable<br>0: Disable<br>1: Enable |
| 10:9  | Reserved |     |                                               |
| 11    | WWDTEN   | R/W | WWDT Clock Enable<br>0: Disable<br>1: Enable  |
| 13:12 | Reserved |     |                                               |
| 14    | SPI2EN   | R/W | SPI2 Clock Enable<br>0: Disable<br>1: Enable  |
| 15    | SPI3EN   | R/W | SPI3 Clock Enable<br>0: Disable<br>1: Enable  |
| 16    | Reserved |     |                                               |

| Field | Name     | R/W | Description                                           |
|-------|----------|-----|-------------------------------------------------------|
| 17    | USART2EN | R/W | USART2 Clock Enable<br>0: Disable<br>1: Enable        |
| 18    | USART3EN | R/W | USART3 Clock Enable<br>0: Disable<br>1: Enable        |
| 19    | UART4EN  | R/W | UART4 Clock Enable<br>0: Disable<br>1: Enable         |
| 20    | UART5EN  | R/W | UART5 Clock Enable<br>0: Disable<br>1: Enable         |
| 21    | I2C1EN   | R/W | I2C1 Clock Enable<br>0: Disable<br>1: Enable          |
| 22    | I2C2EN   | R/W | I2C2 Clock Enable<br>0: Disable<br>1: Enable          |
| 23    | I2C3EN   | R/W | I2C3 Clock Enable<br>0: Disable<br>1: Enable          |
| 24    | Reserved |     |                                                       |
| 25    | CAN1EN   | R/W | CAN1 Clock Enable<br>0: Disable<br>1: Enable          |
| 26    | CAN2EN   | R/W | CAN2 Clock Enable<br>0: Disable<br>1: Enable          |
| 27    | Reserved |     |                                                       |
| 28    | PMUEN    | R/W | PMU Clock Enable<br>0: Disable<br>1: Enable           |
| 29    | DACEN    | R/W | DAC Interface Clock Enable<br>0: Disable<br>1: Enable |
| 31:30 | Reserved |     |                                                       |

#### 6.5.14 APB2 peripheral clock enable register (RCM\_APB2CLKEN)

Offset address: 0x44

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

| Field | Name     | R/W | Description                                            |
|-------|----------|-----|--------------------------------------------------------|
| 0     | TMR1EN   | R/W | TMR1 Clock Enable<br>0: Disable<br>1: Enable           |
| 1     | TMR8EN   | R/W | TMR8 Clock Enable<br>0: Disable<br>1: Enable           |
| 3:2   | Reserved |     |                                                        |
| 4     | USART1EN | R/W | USART1 Clock Enable<br>0: Disable<br>1: Enable         |
| 5     | USART6EN | R/W | USART6 Clock Enable<br>0: Disable<br>1: Enable         |
| 7:6   | Reserved |     |                                                        |
| 8     | ADC1EN   | R/W | ADC1 Interface Clock Enable<br>0: Disable<br>1: Enable |
| 9     | ADC2EN   | R/W | ADC2 Interface Clock Enable<br>0: Disable<br>1: Enable |
| 10    | ADC3EN   | R/W | ADC3 Interface Clock Enable<br>0: Disable<br>1: Enable |
| 11    | SDIOEN   | R/W | SDIO Clock Enable<br>0: Disable<br>1: Enable           |
| 12    | SPI1EN   | R/W | SPI1 Clock Enable<br>0: Disable<br>1: Enable           |
| 13    | Reserved |     |                                                        |
| 14    | SYSCFGEN | R/W | SYSCFG Module Clock Enable<br>0: Disable<br>1: Enable  |
| 15    | Reserved |     |                                                        |
| 16    | TMR9EN   | R/W | TMR9 Clock Enable<br>0: Disable<br>1: Enable           |
| 17    | TMR10EN  | R/W | TMR10 Clock Enable<br>0: Disable<br>1: Enable          |
| 18    | TMR11EN  | R/W | TMR11 Clock Enable<br>0: Disable<br>1: Enable          |

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 31:19 | Reserved |     |             |

### 6.5.15 AHB1 peripheral clock enable register in low-power mode (RCM\_LPAHB1CLKEN)

Offset address: 0x50

Reset value: 0x3E6F 90FF

Access: Access in the form of word, half word and byte, without wait cycle.

The function of this register is to enable the peripheral clock of AHB1 in low-power (sleep) mode.

| Field | Name     | R/W | Description                                   |
|-------|----------|-----|-----------------------------------------------|
| 0     | PAEN     | R/W | GPIOA Clock Enable<br>0: Disable<br>1: Enable |
| 1     | PBEN     | R/W | GPIOB Clock Enable<br>0: Disable<br>1: Enable |
| 2     | PCEN     | R/W | GPIOC Clock Enable<br>0: Disable<br>1: Enable |
| 3     | PDEN     | R/W | GIOD Clock Enable<br>0: Disable<br>1: Enable  |
| 4     | PEEN     | R/W | GPIOE Clock Enable<br>0: Disable<br>1: Enable |
| 5     | PFEN     | R/W | GPIOF Clock Enable<br>0: Disable<br>1: Enable |
| 6     | PGEN     | R/W | GPIOG Clock Enable<br>0: Disable<br>1: Enable |
| 7     | PHEN     | R/W | GPIOH Clock Enable<br>0: Disable<br>1: Enable |
| 11:8  | Reserved |     |                                               |
| 12    | CRCEN    | R/W | CRC Clock Enable<br>0: Disable<br>1: Enable   |
| 14:13 | Reserved |     |                                               |
| 15    | FMEN     | R/W | FMC Clock Enable<br>0: Disable<br>1: Enable   |

| Field | Name       | R/W | Description                                                   |
|-------|------------|-----|---------------------------------------------------------------|
| 16    | SRAM1EN    | R/W | SRAM1 Clock Enable<br>0: Disable<br>1: Enable                 |
| 17    | SRAM2EN    | R/W | SRAM2 Clock Enable<br>0: Disable<br>1: Enable                 |
| 18    | BAKPSRAMEN | R/W | Backup SRAM Interface Clock Enable<br>0: Disable<br>1: Enable |
| 19    | SRAM3EN    | R/W | SRAM3 Clock Enable<br>0: Disable<br>1: Enable                 |
| 20    | Reserved   |     |                                                               |
| 21    | DMA1EN     | R/W | DMA1 Clock Enable<br>0: Disable<br>1: Enable                  |
| 22    | DMA2EN     | R/W | DMA2 Clock Enable<br>0: Disable<br>1: Enable                  |
| 24:23 | Reserved   |     |                                                               |
| 25    | ETHEN      | R/W | ETH Clock Enable<br>0: Disable<br>1: Enable                   |
| 26    | ETHTXEN    | R/W | ETH Transmission Clock Enable<br>0: Disable<br>1: Enable      |
| 27    | ETHRXEN    | R/W | ETH Reception Clock Enable<br>0: Disable<br>1: Enable         |
| 28    | ETHPTPEN   | R/W | ETH PTP Clock Enable<br>0: Disable<br>1: Enable               |
| 29    | OTGFS2EN   | R/W | OTG_FS2 Clock Enable<br>0: Disable<br>1: Enable               |
| 31:30 | Reserved   |     |                                                               |

#### 6.5.16 AHB2 peripheral clock enable register in low-power mode (RCM\_LPAHB2CLKEN)

Offset address: 0x54

Reset value: 0x0000 00C0

Access: Access in the form of word, half word and byte, without wait cycle.

The function of this register is to enable the peripheral clock of AHB2 in low-power (sleep) mode.

| Field | Name     | R/W | Description                                    |
|-------|----------|-----|------------------------------------------------|
| 5:0   | Reserved |     |                                                |
| 6     | RNGEN    | R/W | RNG Clock Enable<br>0: Disable<br>1: Enable    |
| 7     | OTGFSEN  | R/W | OTG_FS Clock Enable<br>0: Disable<br>1: Enable |
| 31:8  | Reserved |     |                                                |

### 6.5.17 AHB3 peripheral clock enable register in low-power mode (RCM\_LPAHB3CLKEN)

Offset address: 0x58

Reset value: 0x0000 0003

Access: Access in the form of word, half word and byte, without wait cycle.

The function of this register is to enable the peripheral clock of AHB3 in low-power (sleep) mode.

| Field | Name     | R/W | Description                                  |
|-------|----------|-----|----------------------------------------------|
| 0     | EMMCEN   | R/W | EMMC Clock Enable<br>0: Disable<br>1: Enable |
| 1     | QSPIEN   | R/W | QSPI Clock Enable<br>0: Disable<br>1: Enable |
| 31:2  | Reserved |     |                                              |

### 6.5.18 APB1 peripheral clock enable register in low-power mode (RCM\_LPAPB1CLKEN)

Offset address: 0x60

Reset value: 0x36FE C9FF

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

The function of this register is to enable the peripheral clock of APB1 in low-power (sleep) mode.

| Field | Name   | R/W | Description                                  |
|-------|--------|-----|----------------------------------------------|
| 0     | TMR2EN | R/W | TMR2 Clock Enable<br>0: Disable<br>1: Enable |
| 1     | TMR3EN | R/W | TMR3 Clock Enable<br>0: Disable<br>1: Enable |

| Field | Name     | R/W | Description                                    |
|-------|----------|-----|------------------------------------------------|
| 2     | TMR4EN   | R/W | TMR4 Clock Enable<br>0: Disable<br>1: Enable   |
| 3     | TMR5EN   | R/W | TMR5 Clock Enable<br>0: Disable<br>1: Enable   |
| 4     | TMR6EN   | R/W | TMR6 Clock Enable<br>0: Disable<br>1: Enable   |
| 5     | TMR7EN   | R/W | TMR7 Clock Enable<br>0: Disable<br>1: Enable   |
| 6     | TMR12EN  | R/W | TMR12 Clock Enable<br>0: Disable<br>1: Enable  |
| 7     | TMR13EN  | R/W | TMR13 Clock Enable<br>0: Disable<br>1: Enable  |
| 8     | TMR14EN  | R/W | TMR14 Clock Enable<br>0: Disable<br>1: Enable  |
| 10:9  | Reserved |     |                                                |
| 11    | WWDTEN   | R/W | WWDT Clock Enable<br>0: Disable<br>1: Enable   |
| 13:12 | Reserved |     |                                                |
| 14    | SPI2EN   | R/W | SPI2 Clock Enable<br>0: Disable<br>1: Enable   |
| 15    | SPI3EN   | R/W | SPI3 Clock Enable<br>0: Disable<br>1: Enable   |
| 16    | Reserved |     |                                                |
| 17    | USART2EN | R/W | USART2 Clock Enable<br>0: Disable<br>1: Enable |
| 18    | USART3EN | R/W | USART3 Clock Enable<br>0: Disable<br>1: Enable |
| 19    | UART4EN  | R/W | UART4 Clock Enable<br>0: Disable<br>1: Enable  |



| Field | Name     | R/W | Description                                           |
|-------|----------|-----|-------------------------------------------------------|
| 20    | UART5EN  | R/W | UART5 Clock Enable<br>0: Disable<br>1: Enable         |
| 21    | I2C1EN   | R/W | I2C1 Clock Enable<br>0: Disable<br>1: Enable          |
| 22    | I2C2EN   | R/W | I2C2 Clock Enable<br>0: Disable<br>1: Enable          |
| 23    | I2C3EN   | R/W | I2C3 Clock Enable<br>0: Disable<br>1: Enable          |
| 24    | Reserved |     |                                                       |
| 25    | CAN1EN   | R/W | CAN1 Clock Enable<br>0: Disable<br>1: Enable          |
| 26    | CAN2EN   | R/W | CAN2 Clock Enable<br>0: Disable<br>1: Enable          |
| 27    | Reserved |     |                                                       |
| 28    | PMUEN    | R/W | PMU Clock Enable<br>0: Disable<br>1: Enable           |
| 29    | DACEN    | R/W | DAC Interface Clock Enable<br>0: Disable<br>1: Enable |
| 31:30 | Reserved |     |                                                       |

#### 6.5.19 APB2 peripheral clock enable register in low-power mode (RCM\_LPAPB2CLKEN)

Offset address: 0x64

Reset value: 0x0007 5F33

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

The function of this register is to enable the peripheral clock of AHB2 in low-power (sleep) mode.

| Field | Name   | R/W | Description                                  |
|-------|--------|-----|----------------------------------------------|
| 0     | TMR1EN | R/W | TMR1 Clock Enable<br>0: Disable<br>1: Enable |
| 1     | TMR8EN | R/W | TMR8 Clock Enable<br>0: Disable<br>1: Enable |

| Field | Name     | R/W | Description                                            |
|-------|----------|-----|--------------------------------------------------------|
| 3:2   | Reserved |     |                                                        |
| 4     | USART1EN | R/W | USART1 Clock Enable<br>0: Disable<br>1: Enable         |
| 5     | USART6EN | R/W | USART6 Clock Enable<br>0: Disable<br>1: Enable         |
| 7:6   | Reserved |     |                                                        |
| 8     | ADC1EN   | R/W | ADC1 Interface Clock Enable<br>0: Disable<br>1: Enable |
| 9     | ADC2EN   | R/W | ADC2 Interface Clock Enable<br>0: Disable<br>1: Enable |
| 10    | ADC3EN   | R/W | ADC3 Interface Clock Enable<br>0: Disable<br>1: Enable |
| 11    | SDIOEN   | R/W | SDIO Clock Enable<br>0: Disable<br>1: Enable           |
| 12    | SPI1EN   | R/W | SPI1 Clock Enable<br>0: Disable<br>1: Enable           |
| 13    | Reserved |     |                                                        |
| 14    | SYSCFGEN | R/W | SYSCFG Module Clock Enable<br>0: Disable<br>1: Enable  |
| 15    | Reserved |     |                                                        |
| 16    | TMR9EN   | R/W | TMR9 Clock Enable<br>0: Disable<br>1: Enable           |
| 17    | TMR10EN  | R/W | TMR10 Clock Enable<br>0: Disable<br>1: Enable          |
| 18    | TMR11EN  | R/W | TMR11 Clock Enable<br>0: Disable<br>1: Enable          |
| 31:19 | Reserved |     |                                                        |

#### 6.5.20 Backup domain control register (RCM\_BDCTRL)

Offset address: 0x70

Reset value: 0x0000 0000, which can be reset effectively only by RTC domain

Access: Access in the form of word, half word and byte, with 0 to 3 wait cycles

When the register is accessed continuously, the waiting state will be inserted.

Note: Only when BPWEN bit in PMU\_CTRL is set to 1, can LSEEN, LSEBCFG, RTCSRCSEL and RTCCLKEN be changed.

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | LSEEN     | R/W | Low-Speed External Oscillator Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                     |
| 1     | LSERDYFLG | R   | Low-Speed External Clock Ready Flag<br>When LSECLK is stable, this bit is set to 1 by hardware, and when it is unstable, it is cleared by hardware.<br>0: Not ready<br>1: Ready                                                                                                                                                                                                                                     |
| 2     | LSEBCFG   | R/W | Low-Speed External Clock Bypass Mode Configure<br>Bypass mode refers to the mode in which external clock is used as the LSECLK clock source; otherwise the resonator is used as the LSECLK clock source.<br>0: Non-bypass mode<br>1: Bypass mode                                                                                                                                                                    |
| 7:3   | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9:8   | RTCSRCSEL | R/W | RTC Clock Source Select<br>First set the RTCRST bit to reset the RTC domain, and then select the RTC clock source. It is impossible to directly configure the register to modify.<br>00: No clock<br>01: LSECLK is used as RTC clock<br>10: LSICLK is used as RTC clock<br>11: HSECLK is used as RTC clock after frequency division (the frequency division factor is determined by RTCPSC bit of RCM_CFG register) |
| 14:10 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 15    | RTCCLKEN  | R/W | RTC Clock Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                         |
| 16    | BDRST     | R/W | Reset the backup domain software (Backup Domain Software Reset)<br>Set to 1 or cleared by software.<br>0: Reset is not activated<br>1: Reset the backup domain (only affect LSECLK oscillator, RTC real-time clock and register RCM_BDCTRL)                                                                                                                                                                         |
| 31:17 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                     |

### 6.5.21 Clock control/State register (RCM\_CSTS)

Offset address: 0x74

Reset value: 0x0E00 0000, except reset flag, all are cleared by system reset, and reset flag can only be cleared by power reset.

Access: Access in the form of word, half word and byte, with 0 to 3 wait cycles.

When the register is accessed continuously, the waiting state will be inserted.

| Field | Name       | R/W  | Description                                                                                                                                                                                                            |
|-------|------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | LSIEN      | R/W  | Low-Speed Internal Oscillator Enable<br>Set to 1 or cleared by software.<br>0: Disable<br>1: Enable                                                                                                                    |
| 1     | LSIRDYFLG  | R    | Low-Speed Internal Oscillator Ready Flag<br>When LSICLK is stable, this bit is set to 1 by hardware, and when it is unstable, it is cleared by hardware.<br>0: Not ready<br>1: Ready                                   |
| 23:2  | Reserved   |      |                                                                                                                                                                                                                        |
| 24    | RSTFLGCLR  | RT_W | Reset Flag Clear<br>The reset flag is set or cleared by software, including RSTFLGCLR.<br>0: Disable<br>1: Clear the reset flag                                                                                        |
| 25    | BORRSTFLG  | R    | BOR flag<br>It is set by hardware when brownout reset occurs; otherwise it is cleared by setting RSTFLGCLR bit.<br>0: Reset does not occur<br>1: Reset occurs                                                          |
| 26    | PINRSTFLG  | R    | PIN Reset Flag<br>It is set by hardware when pin reset occurs; otherwise it is cleared by setting RSTFLGCLR.<br>0: Reset does not occur<br>1: Reset occurs                                                             |
| 27    | PODRSTFLG  | R    | POR/PDR Reset Flag<br>Set to 1 by hardware; cleared by software by writing RSTFLGCLR bit.<br>0: No power-on/power-down reset occurs<br>1: Power-on/power-down reset occurs                                             |
| 28    | SWRSTFLG   | R    | Software Reset Flag<br>Set to 1 by hardware; cleared by software by writing RSTFLGCLR bit.<br>0: Reset does not occur<br>1: Reset occurs                                                                               |
| 29    | IWDTRSTFLG | R    | Independent Watchdog Reset Flag<br>When independent watchdog reset occurs in $V_{DD}$ area, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit.<br>0: Reset does not occur<br>1: Reset occurs |
| 30    | WWDTRSTFLG | R    | Window Watchdog Reset Flag<br>When window watchdog is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit.<br>0: Reset does not occur<br>1: Reset occurs                                |

| Field | Name       | R/W | Description                                                                                                                                                                            |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | LPWRRSTFLG | R   | Low Power Reset Flag<br>When low-power management is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit.<br>0: Reset does not occur<br>1: Reset occurs |

#### 6.5.22 Spread spectrum clock configuration register (RCM\_SSCCFG)

Offset address: 0x80

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, with 0 to 3 wait cycles.

Because the spread spectrum clock only acts on PLL1, this register can be written only when PLL1 is not enabled to configure the spread spectrum clock.

| Field | Name     | R/W | Description                                                                                                  |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------|
| 12:0  | MODPCFG  | R/W | Modulation Period Configure<br>Set to 1 or cleared by software.<br>Configure the input of modulation period. |
| 27:13 | STEP     | R/W | Incrementation Step<br>Set to 1 or cleared by software.<br>Configure the input of modulation amplitude.      |
| 29:28 | Reserved |     |                                                                                                              |
| 30    | SSSEL    | R/W | Spread Spectrum Select<br>It is set or cleared by software.<br>0: Center spread<br>1: Downward spread        |
| 31    | SSEN     | R/W | Spread Spectrum Enable<br>Set to 1 or cleared by software.<br>0: Disable<br>1: Enable                        |

## 7 Power Management Unit (PMU)

### 7.1 Full name and abbreviation description of terms

Table 37 Full name and abbreviation description of terms

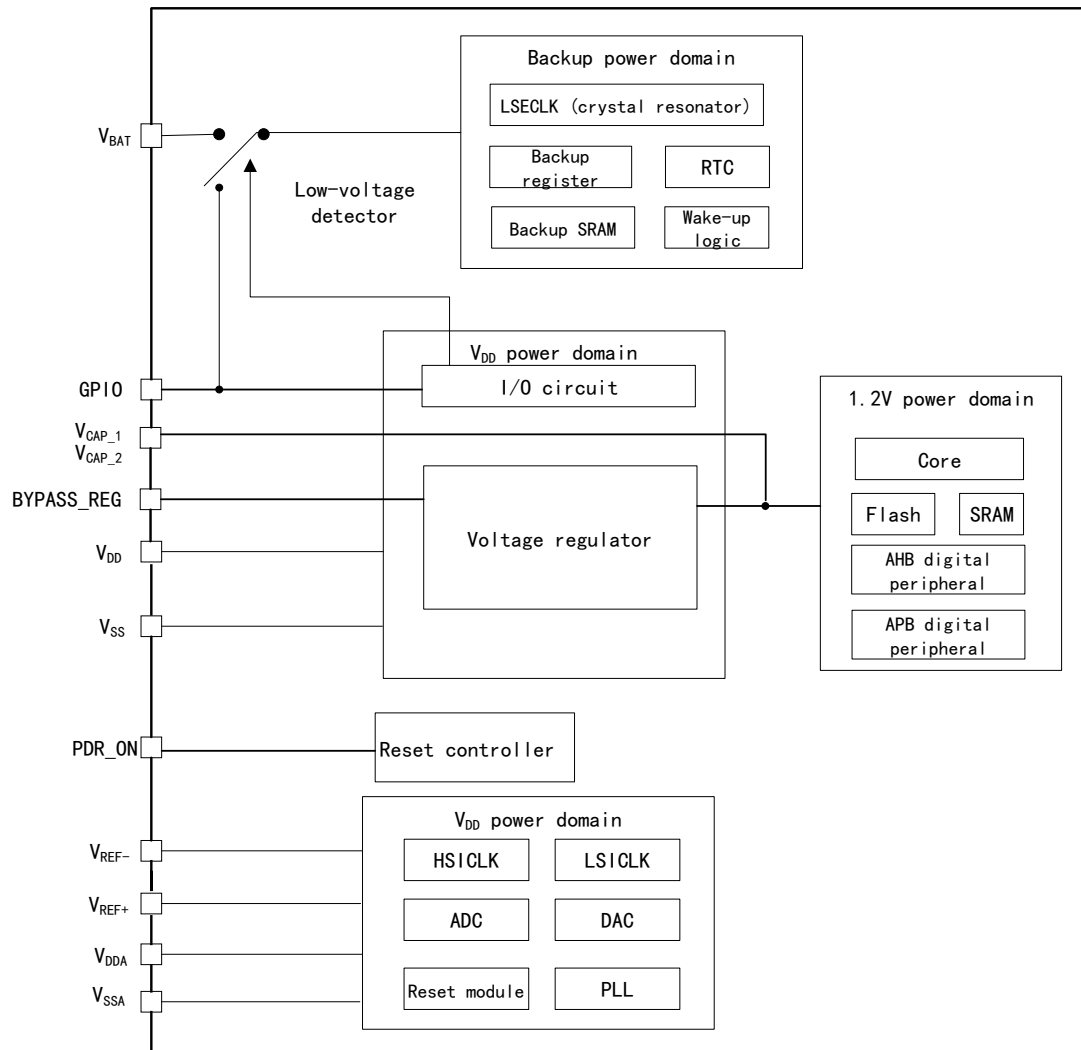
| Full name in English   | English abbreviation |
|------------------------|----------------------|
| Power Management Unit  | PMU                  |
| Power On Reset         | POR                  |
| Power Down Reset       | PDR                  |
| Brown-out Reset        | BOR                  |
| Power Voltage Detector | PVD                  |

### 7.2 Introduction

The power supply is the basis for stable operation of a system. The working voltage is 1.8~3.6V. It can provide 1.2V power supply through the built-in voltage regulator. If the main power  $V_{DD}$  is powered down, it can supply power to the backup power supply area through  $V_{BAT}$ .

## 7.3 Structure block diagram

Figure 38 Power Supply Structure Block Diagram



## 7.4 Functional description

### 7.4.1 Power domain

The power domain of the product includes:  $V_{DD}$  power domain,  $V_{DDA}$  power domain, 1.2V power domain, and backup power domain.

#### 7.4.1.1 $V_{DD}$ power domain

Supply power through  $V_{DD}/V_{SS}$  pin to the voltage regulator and I/O.

#### Voltage regulator

Power can be supplied to 1.2V power domain in the following operating modes:

- Normal mode: In this mode, 1.2V power supply area operates at full power, and the level of the output voltage can be selected through VOSSEL bit of the register PMU\_CTRL.
- Stop mode: In this mode, 1.2V power supply area works in low-power state. All clocks are off. Peripherals stop working and the set voltage output level remains unchanged.
- Standby mode: In this mode, the 1.2V power supply area stops power supply, and except for the standby circuit, the content of register and SRAM will be lost.

#### 7.4.1.2 $V_{DDA}$ power domain

Power the ADC, DAC, HSICLK, LSICLK, PLL and reset module through  $V_{DDA}/V_{SSA}$  and  $V_{REF+}/V_{REF-}$  pins.

#### Independent ADC power supply and reference voltage

Independent ADC power supply can improve conversion accuracy, and the specific power pins are as follows:

- $V_{DDA}$ : Power pin of ADC
- $V_{SSA}$ : Independent power ground pin
- $V_{REF+}/V_{REF-}$ : ADC reference voltage pin

#### 7.4.1.3 1.2V power domain

The core, Flash, SRAM and digital peripherals are powered by voltage regulator.

#### 7.4.1.4 Backup power domain

When  $V_{DD}$  exists, the backup power supply area is powered by  $V_{DD}$ . When  $V_{DD}$  is powered down, the backup power supply area is powered by  $V_{BAT}$ , which is used to save the content of backup register and maintain RTC function. Power the LSECLK crystal oscillator, RTC, backup register, backup SRAM, PC13, PC14, PC15, and wake-up logics.

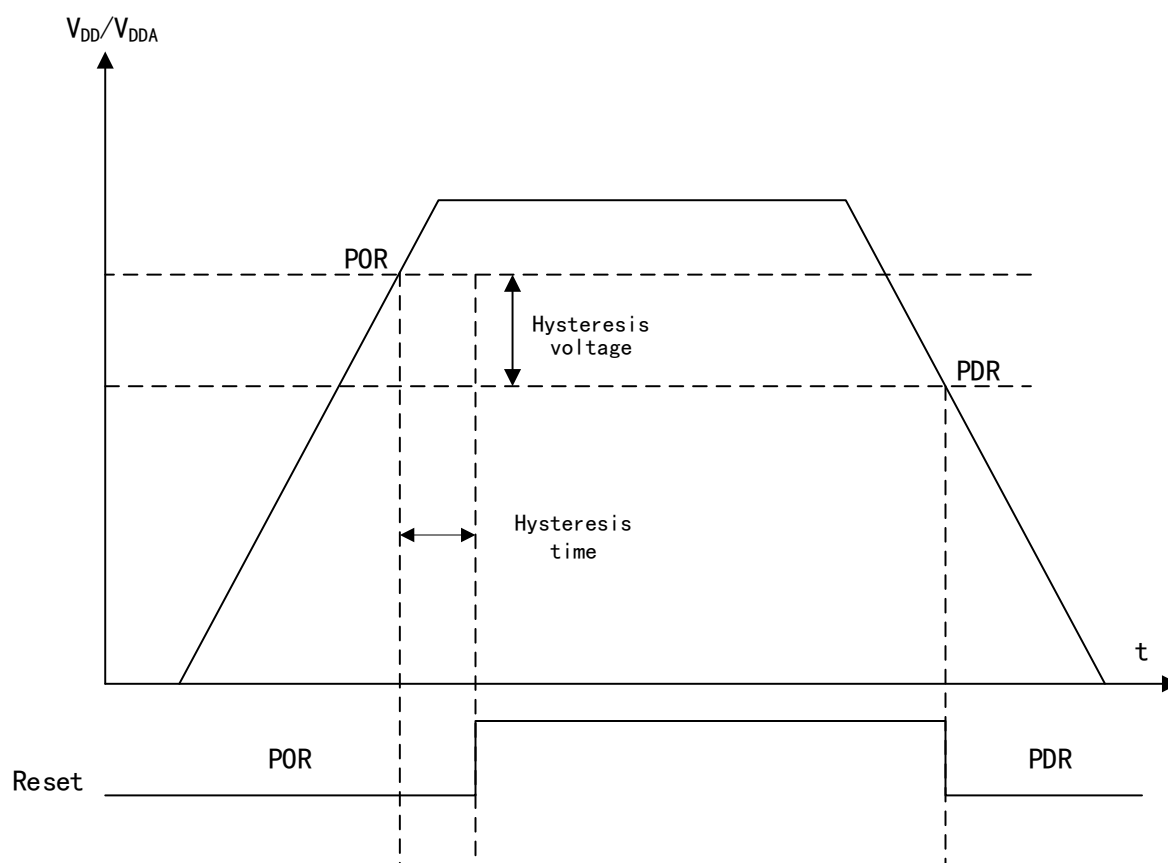
### 7.4.2 Power Management

#### 7.4.2.1 Power-on/power-down reset (POR and PDR)

When the  $V_{DD}/V_{DDA}$  is detected to be lower than the threshold voltage  $V_{POR}$  and  $V_{PDR}$ , the chip will automatically maintain the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, refer to the corresponding datasheet.



Figure 9 Power-on Reset and Power-down Reset Waveform

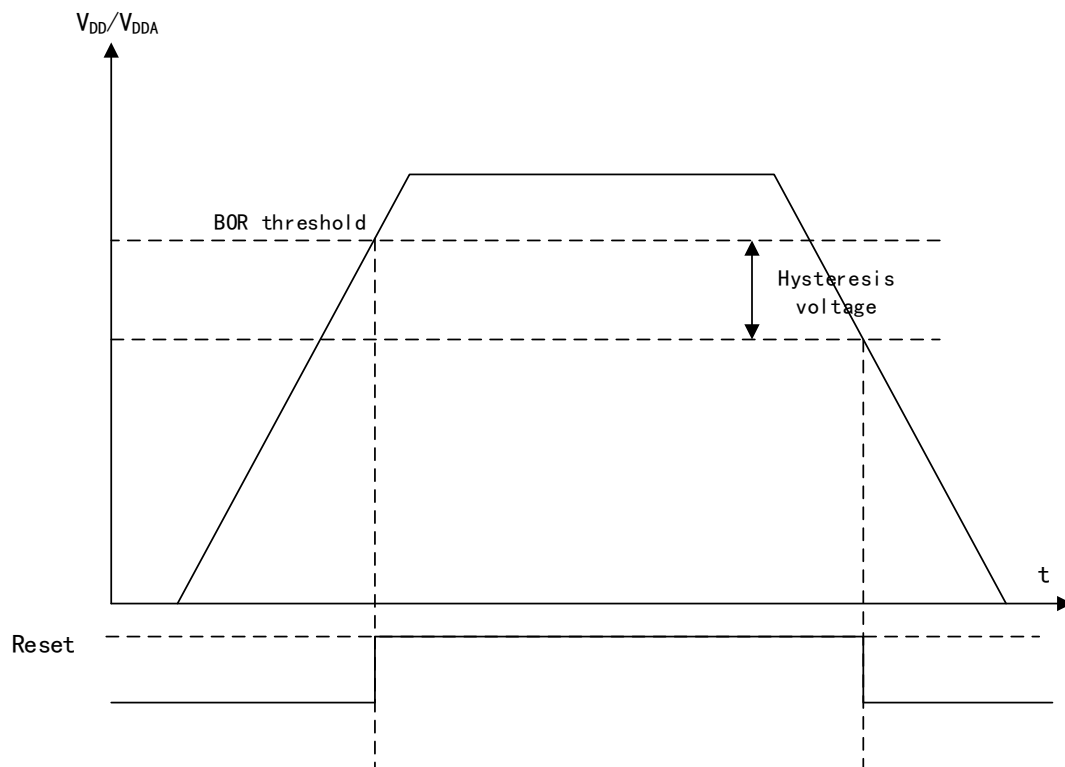


#### 7.4.2.2 Brownout reset (BOR)

When it is detected that  $V_{DD}/V_{DDA}$  is lower than the threshold voltage  $V_{BOR}$ , the chip will automatically remain in reset state, and  $V_{BOR}$  can be configured through option bytes. The followings are 4 thresholds of  $V_{BOR}$ :

- $V_{BOR0}$ : BOR is turned off, and the voltage range is 1.80~2.10V
- $V_{BOR1}$ : BOR level is 1, and the voltage range is 2.10~2.40V
- $V_{BOR2}$ : BOR level is 2, and the voltage range is 2.40~2.70V
- $V_{BOR3}$ : BOR level is 3, and the voltage range is 2.70~3.60V

Figure 10 BOR Threshold Waveform



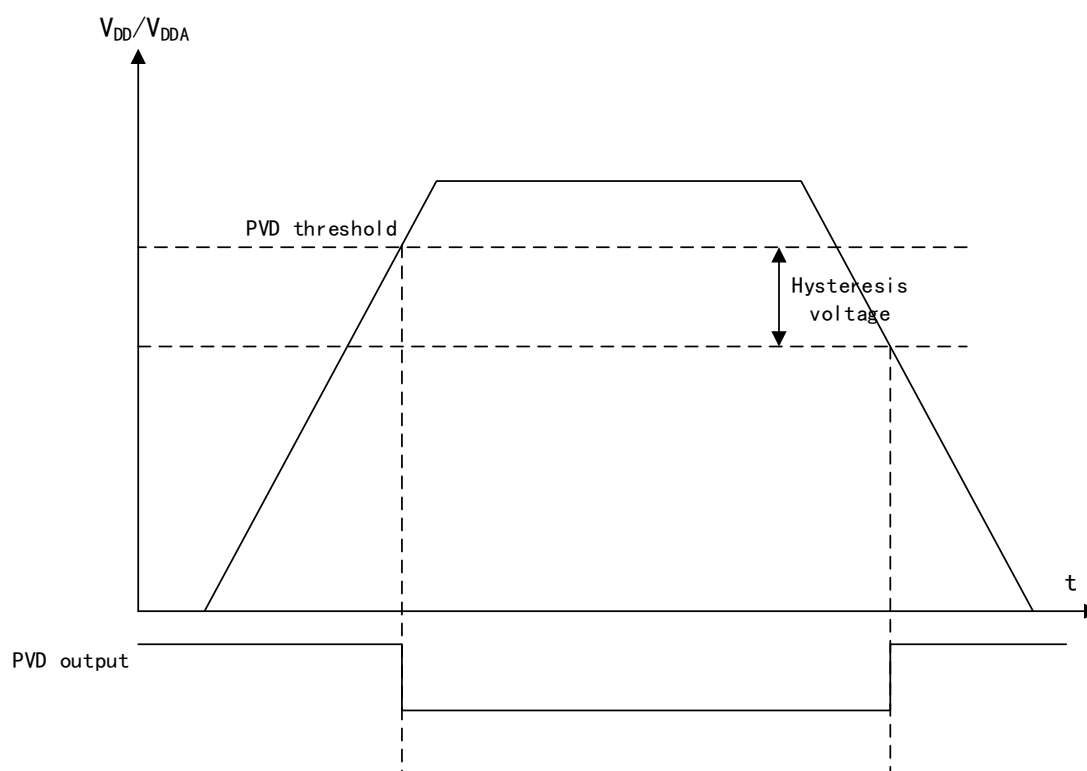
#### 7.4.2.3 Power voltage detector (PVD)

A threshold can be set for PVD to monitor whether  $V_{DD}/V_{DDA}$  is higher or lower than the threshold. If interrupt is enabled, the interrupt can be triggered to process  $V_{DD}/V_{DDA}$  exceeding the threshold in advance. The usage of PVD is as follows:

- (1) Set the PVDEN bit of the configuration register PMU\_CTRL to 1 to enable PVD.
- (2) Select the voltage threshold of PVD for the PLSEL[2:0] bits of the configuration register PMU\_CTRL.
- (3) The PVDOFLG bit of the configuration register PMU\_CSTS indicates the value of  $V_{DD}$  is higher or lower than the threshold of PVD.
- (4) When it is detected that  $V_{DD}/V_{DDA}$  is lower or higher than the threshold of PVD, PVD interrupt will be generated.

The threshold waveform of PVD is shown below. See the corresponding datasheet for PVD threshold and hysteresis voltage.

Figure 11 PVD Threshold Waveform



### 7.4.3 Power consumption control

#### 7.4.3.1 Reduce the power consumption in low-power mode

There are three low-power modes: sleep mode, stop mode and standby mode. The power consumption is reduced by closing the core and clock source and setting the voltage regulator.

The power consumption, wake-up start time, wake-up mode and data storage of each low-power mode are different. The lower the power consumption is, the longer the wake-up time is. The less the wake-up mode is, the less the data saved are after wake-up. Users can choose the most appropriate low-power mode according to their needs. The following table shows the difference among three low-power modes.

Table 39 Difference among "Sleep Mode, Stop Mode and Standby Mode"

| Mode  | Description           | Entry mode           | Wake-up mode  | Voltage regulator | Effect on 1.2V area clock | Effect on $V_{DD}$ area clock |
|-------|-----------------------|----------------------|---------------|-------------------|---------------------------|-------------------------------|
| Sleep | Arm® Cortex®-M4F core | Call WFI instruction | Any interrupt | Open              | Only the core clock       | None                          |

| Mode    | Description                                                                | Entry mode                                          | Wake-up mode                                                                                                                                   | Voltage regulator               | Effect on 1.2V area clock                                         | Effect on V <sub>DD</sub> area clock              |
|---------|----------------------------------------------------------------------------|-----------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|-------------------------------------------------------------------|---------------------------------------------------|
|         | stops, and all peripherals including the core peripheral are still working | Call WFE instruction                                | Wake-up event                                                                                                                                  | Open                            | is turned off and it has no effect on other clocks and ADC clocks | None                                              |
| Stop    | All clocks have stopped                                                    | PDDSCFG and LPDSCFG bits +SLEEPDEEP bit +WFI or WFE | Any external interrupt                                                                                                                         | Turn on or be in low-power mode | Close clocks of all 1.2V areas                                    | The oscillator of HSICLK and HSECLK is turned off |
| Standby | 1.2V power off                                                             | PDDSCFG bit +SLEEPDEEP bit +WFI or WFE              | Rising edge of WKUP pin, RTC alarm event, RTC wake-up event, RTC timestamp event, RTC tamper event, external reset on NRST pin, and IWDG reset | Off                             |                                                                   |                                                   |

## Sleep mode

The characteristics of sleep mode are shown in the table below:

Table 40 Characteristics of Sleep Mode

| Characteristics | Description                                                                                                                                                                                                                                                                                                       |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Enter           | Enter the sleep mode immediately by executing WFI or WFE instructions. When SLEEPONEINT is set to 0 and WFI or WFE instruction is executed, the system will enter the sleep mode immediately. When SLEEPONEINT is set to 1, the system will exit the interrupt program and then enter the sleep mode immediately. |
| Wake-up         | If WFI instruction is executed to enter the stop mode, wake up by any interrupt. If WFE instruction is executed to enter the stop mode, wake up through an event.                                                                                                                                                 |
| Sleep           | The core stops working, all peripherals are still running, and the data in the core registers and memory before sleep are saved.                                                                                                                                                                                  |
| Wake-up delay   | None                                                                                                                                                                                                                                                                                                              |

| Characteristics | Description                                                                                                                                                                                                                                             |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| After wake-up   | If the system is woken up by interrupt, it will first enter the interrupt, then exit the interrupt, and then execute the program after WFI instruction. If the system is woken up by event, it will directly execute the program after WFE instruction. |

## Stop mode

The characteristics of stop mode are shown in the table below:

Table 41 Characteristics of Stop Mode

| Characteristics | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Enter           | SLEEPDEEP bit of the core register is set to 1, PDDSCFG bit of the register PMU_CTRL is set to 0, and when executing WFI or WFE instruction, the system will enter the stop mode immediately.<br>When LPDSCFG bit of the register PMU_CTRL is set to 0, the voltage regulator is working in normal mode. When LPDSCFG bit of the register PMU_CTRL is set to 1, the voltage regulator is working in low-power mode. |
| Wake-up         | If WFI instruction is executed to enter the sleep mode, wake up by any interrupt. If WFE instruction is executed to enter the sleep mode, wake up through an event.                                                                                                                                                                                                                                                 |
| Stop            | The core will stop working, the peripheral will stop working, and the data in the core register and memory before stop will be saved.                                                                                                                                                                                                                                                                               |
| Wake-up delay   | HSICLK oscillator wake-up time + voltage regulator wake-up time from low-power mode.                                                                                                                                                                                                                                                                                                                                |
| After wake-up   | If the system is woken up by interrupt, it will first enter the interrupt, then exit the interrupt, and then execute the program after WFI instruction. If the system is woken up by event, it will directly execute the program after WFE instruction.                                                                                                                                                             |

## Standby mode

The characteristics of standby mode are shown in the table below:

Table 42 Standby Mode

| Characteristics | Description                                                                                                                                                                                                             |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Enter           | SLEEPDEEP bit of the core register is set to 1, PDDSCFG bit of the register PMU_CTRL is set to 1, WUEFLG bit is set to 0 and when executing WFI or WFE instruction, the system will enter the standby mode immediately. |
| Wake-up         | Wake up by rising edge of WKUP pin, RTC alarm, wake-up, tamper event or NRST pin external reset and IWDG reset.                                                                                                         |
| Standby         | The core will stop working, the peripheral will stop working, and the data in the core register and memory will be lost.                                                                                                |
| Wake-up delay   | Chip reset time.                                                                                                                                                                                                        |
| After wake-up   | The program starts executing from the beginning.                                                                                                                                                                        |

### 7.4.3.2 Reduce the power consumption in run mode

In the run mode, the power consumption can be reduced by reducing the system clock, closing or reducing the peripheral clock on the APB/AHB bus.

### 7.4.3.3 RTC multiplexing function is waken up from low-power mode

RTC multiplexing functions include RTC alarm, RTC wake-up event, RTC tamper event and RTC timestamp event. These functions can wake up MCU from stop mode or standby mode, and RTC provides programmable time base to wake up the devices regularly from stop or standby mode.

## 7.5 Register address mapping

Table 43 PMU Register Address Mapping

| Register name | Description                  | Offset address |
|---------------|------------------------------|----------------|
| PMU_CTRL      | Power control register       | 0x00           |
| PMU_CSTS      | Power control/state register | 0x04           |

## 7.6 Register functional description

### 7.6.1 Power control register (PMU\_CTRL)

Offset address: 0x00

Reset value: 0x0000 C000 (cleared when waking up from standby mode)

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                       |
|-------|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | LPDSCFG  | R/W   | Low Power Deepsleep Configure<br>Configure the working state of the voltage regulator in stop mode.<br>0: Enable<br>1: Low-power mode                                                                                                             |
| 1     | PDDSCFG  | R/W   | Power Down Deep Sleep Configure<br>When the CPU enters deep sleep, configure the voltage regulator state in standby and stop modes.<br>0: The voltage regulator is controlled by LPDSCFG bit when entering the stop mode<br>1: Enter standby mode |
| 2     | WUFLGCLR | RC_W1 | Wakeup Flag Clear<br>0: Invalid<br>1: Clear the wake-up flag after 2 system clock cycles by writing 1                                                                                                                                             |
| 3     | SBFLGCLR | RC_W1 | Standby Flag Clear<br>0: Invalid<br>1: Write 1 to clear the standby flag                                                                                                                                                                          |
| 4     | PVDEN    | R/W   | Power Voltage Detector Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                          |
| 7:5   | PLSEL    | R/W   | PVD Level Select<br>000: 2.0V<br>001: 2.1V<br>010: 2.3V<br>011: 2.5V<br>100: 2.6V                                                                                                                                                                 |

| Field | Name     | R/W | Description                                                                                                                                                                                              |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 101: 2.7V<br>110: 2.8V<br>111: 2.9V<br>Note: For detailed instructions, see the corresponding datasheet.                                                                                                 |
| 8     | BPWEN    | R/W | Backup Domain Write Access Enable<br>Backup area refers to RTC and backup register. Write access is disabled after reset, and is allowed after writing 1.<br>0: Write is disabled<br>1: Write is enabled |
| 9     | FPDSM    | R/W | Flash power-down in Stop mode<br>0: Flash does not power down when entering the stop mode<br>1: Flash powers down when entering the stop mode                                                            |
| 13:10 | Reserved |     |                                                                                                                                                                                                          |
| 14    | VOSSEL   | R/W | Regulator Voltage Scaling Output Selection<br>0: Level 2 mode<br>1: Level 1 mode                                                                                                                         |
| 31:15 | Reserved |     |                                                                                                                                                                                                          |

### 7.6.2 Power supply control/state register (PMU\_CSTS)

Offset address: 0x04

Reset value: 0x0000 0000 (not cleared when waking up from standby mode)

Compared with the standard APB read, it requires extra APB cycle to read this register.

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | WUEFLG  | R   | Wakeup Event Flag<br>This bit is set by hardware, indicating whether wake-up event or RTC alarm wake-up event, RTC tamper event, RTC timestamp or RTC wake-up event occurs on WKUP pin.<br>0: Not occur<br>1: Occurred<br>Note: Enable the WKUP pin, and an event will be detected when the WKUP pin is at high level.                                           |
| 1     | SBFLG   | R   | Standby Flag<br>This bit is set to 1 by hardware, and can only be cleared by POR/PDR (power-on/power-down reset) or by setting the SBFLGCLR bit of the power supply control register (PMU_CTRL).<br>0: Not enter the standby mode<br>1: Have entered the standby mode                                                                                            |
| 2     | PVDOFLG | R   | PVD Output Flag<br>Indicate whether $V_{DD}/V_{DDA}$ is higher than the PVD threshold selected by PLSEL[2:0]<br>This bit is valid only when PVD is enabled by PVDEN BIT.<br>0: $V_{DD}/V_{DDA}$ higher than PVD threshold<br>1: $V_{DD}/V_{DDA}$ lower than PVD threshold<br>Note: This bit is 0 after reset or when entering the standby mode (PVD stops work). |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3     | BKPRFLG  | R   | Backup Regulator Ready Flag<br>This bit is set to 1 by hardware, indicating whether the backup regulator is ready.<br>0: Not ready<br>1: Ready                                                                                                                             |
| 7:4   | Reserved |     |                                                                                                                                                                                                                                                                            |
| 8     | WKUPCFG  | R/W | WKUP Pin Configure<br>When WKUP is used as a normal I/O, the event on WKUP pin cannot wake up the CPU in standby mode. It can wake up CPU only when it is not used as a normal I/O.<br>0: Configure normal I/O<br>1: Can wake MCU<br>Note: Clear this bit in system reset. |
| 9     | BKPREN   | R/W | Backup Regulator Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                         |
| 13:10 | Reserved |     |                                                                                                                                                                                                                                                                            |
| 14    | VOSRFLG  | R   | Regulator Voltage Scaling Output Selection Ready Flag<br>0: Not ready<br>1: Ready                                                                                                                                                                                          |
| 31:15 | Reserved |     |                                                                                                                                                                                                                                                                            |



## 8 Nested Vector Interrupt Controller (NVIC)

### 8.1 Full name and abbreviation description of terms

Table 44 Full name and abbreviation description of terms

| Full name in English   | English abbreviation |
|------------------------|----------------------|
| Non Maskable Interrupt | NMI                  |

### 8.2 Introduction

The Cortex-M4F core in the product integrates nested vectored interrupt controller (NVIC), which is closely coupled with the core, and can handle exceptions and interrupts and power management control efficiently and with low delay. For more instructions about NVIC, see *Cortex-M4F Technical Reference Manual*.

### 8.3 Main characteristics

- (1) 88 maskable interrupt channels (excluding 16 Arm® Cortex®-M4F interrupt lines)
- (2) Low-delay exception and interrupt processing
- (3) Power management control
- (4) Implementation of system control register

### 8.4 Interrupt and exception vector table

Table 45 APM32F425xG\_F427xG Interrupt and Exception Vector Table

| Exception type | Vector No. | Priority   | Vector address | Description             |
|----------------|------------|------------|----------------|-------------------------|
| -              | -          | -          | 0x0000_0000    | Reserved                |
| Reset          | -          | -3         | 0x0000_0004    | Reset                   |
| NMI            | -          | -2         | 0x0000_0008    | Non-maskable interrupt  |
| HardFault      | -          | -1         | 0x0000_000C    | Various hardware faults |
| MemManage      | -          | Can be set | 0x0000_0010    | Memory management       |
| BusFault       | -          | Can be set | 0x0000_0014    | -                       |
| UsageFault     | -          | Can be set | 0x0000_0018    | -                       |

| Exception type | Vector No. | Priority   | Vector address                | Description                                         |
|----------------|------------|------------|-------------------------------|-----------------------------------------------------|
| -              | -          | -          | 0x0000_001C to<br>0x0000_002B | Reserved                                            |
| SVCall         | -          | Can be set | 0x0000_002C                   | System service called by SWI instruction            |
| Debug Monitor  | -          | Can be set | 0x0000_0030                   | Debug monitor                                       |
| -              | -          | -          | 0x0000_0034                   | Reserved                                            |
| PendSV         | -          | Can be set | 0x0000_0038                   | Pending system service request                      |
| SysTick        | -          | Can be set | 0x0000_003C                   | System tick timer                                   |
| WWDT           | 0          | Can be set | 0x0000_0040                   | Window watchdog interrupt                           |
| PVD            | 1          | Can be set | 0x0000_0044                   | Power voltage detection interrupt through EINT line |
| TAMP_STAMP     | 2          | Can be set | 0x0000_0048                   | Tamper and timestamp interrupt through EINT line    |
| RTC_WKUP       | 3          | Can be set | 0x0000_004C                   | RTC wake-up interrupt through EINT line             |
| FLASH          | 4          | Can be set | 0x0000_0050                   | Flash memory global interrupt                       |
| RCM            | 5          | Can be set | 0x0000_0054                   | RCM interrupt                                       |
| EINT0          | 6          | Can be set | 0x0000_0058                   | EINT Line 0 interrupt                               |
| EINT1          | 7          | Can be set | 0x0000_005C                   | EINT Line 1 interrupt                               |
| EINT2          | 8          | Can be set | 0x0000_0060                   | EINT Line 2 interrupt                               |
| EINT3          | 9          | Can be set | 0x0000_0064                   | EINT Line 3 interrupt                               |
| EINT4          | 10         | Can be set | 0x0000_0068                   | EINT Line 4 interrupt                               |
| DMA1_STR0      | 11         | Can be set | 0x0000_006C                   | DMA1 data stream 0 global interrupt                 |
| DMA1_STR1      | 12         | Can be set | 0x0000_0070                   | DMA1 data stream 1 global interrupt                 |

| Exception type     | Vector No. | Priority   | Vector address | Description                                                     |
|--------------------|------------|------------|----------------|-----------------------------------------------------------------|
| DMA1_STR2          | 13         | Can be set | 0x0000_0074    | DMA1 data stream 2 global interrupt                             |
| DMA1_STR3          | 14         | Can be set | 0x0000_0078    | DMA1 data stream 3 global interrupt                             |
| DMA1_STR4          | 15         | Can be set | 0x0000_007C    | DMA1 data stream 4 global interrupt                             |
| DMA1_STR5          | 16         | Can be set | 0x0000_0080    | DMA1 data stream 5 global interrupt                             |
| DMA1_STR6          | 17         | Can be set | 0x0000_0084    | DMA1 data stream 6 global interrupt                             |
| ADC                | 18         | Can be set | 0x0000_0088    | ADC1 and ADC2 global interrupt                                  |
| CAN1_TX            | 19         | Can be set | 0x0000_008C    | CAN1 transmitting interrupt                                     |
| CAN1_RX0           | 20         | Can be set | 0x0000_0090    | CAN1 receiving 0 interrupt                                      |
| CAN1_RX1           | 21         | Can be set | 0x0000_0094    | CAN1 receiving 1 interrupt                                      |
| CAN1_SCE           | 22         | Can be set | 0x0000_0098    | CAN1 SCE interrupt                                              |
| EINT9_5            | 23         | Can be set | 0x0000_009C    | EINT line [9:5] interrupt                                       |
| TMR1_BRK_TMR9      | 24         | Can be set | 0x0000_00A0    | TMR1 braking interrupt/TMR9 global interrupt                    |
| TMR1_UP_TMR10      | 25         | Can be set | 0x0000_00A4    | TMR1 update interrupt/TMR10 global interrupt                    |
| TMR1_TRG_COM_TMR11 | 26         | Can be set | 0x0000_00A8    | TMR1 trigger and communication interrupt/TMR11 global interrupt |
| TMR1_CC            | 27         | Can be set | 0x0000_00AC    | TMR1 capture/compare interrupt                                  |
| TMR2               | 28         | Can be set | 0x0000_00B0    | TMR2 interrupt                                                  |

| Exception type         | Vector No. | Priority   | Vector address | Description                                                     |
|------------------------|------------|------------|----------------|-----------------------------------------------------------------|
| TMR3                   | 29         | Can be set | 0x0000_00B4    | TMR3 interrupt                                                  |
| TMR4                   | 30         | Can be set | 0x0000_00B8    | TMR4 interrupt                                                  |
| I2C1_EV                | 31         | Can be set | 0x0000_00BC    | I2C1 event interrupt                                            |
| I2C1_ER                | 32         | Can be set | 0x0000_00C0    | I2C1 error interrupt                                            |
| I2C2_EV                | 33         | Can be set | 0x0000_00C4    | I2C2 event interrupt                                            |
| I2C2_ER                | 34         | Can be set | 0x0000_00C8    | I2C2 error interrupt                                            |
| SPI1                   | 35         | Can be set | 0x0000_00CC    | SPI1 interrupt                                                  |
| SPI2                   | 36         | Can be set | 0x0000_00D0    | SPI2 interrupt                                                  |
| USART1                 | 37         | Can be set | 0x0000_00D4    | USART1 interrupt                                                |
| USART2                 | 38         | Can be set | 0x0000_00D8    | USART2 interrupt                                                |
| USART3                 | 39         | Can be set | 0x0000_00DC    | USART3 interrupt                                                |
| EINT15_10              | 40         | Can be set | 0x0000_00E0    | EINT line [15:10] interrupt                                     |
| RTC_Alarm              | 41         | Can be set | 0x0000_00E4    | RTC alarm interrupt                                             |
| OTG_FS1 WKUP           | 42         | Can be set | 0x0000_00E8    | OTG_FS1 wake-up interrupt through EINT line                     |
| TMR8_BRK_TMR1<br>2     | 43         | Can be set | 0x0000_00EC    | TMR8 braking interrupt/TMR12 global interrupt                   |
| TMR8_UP_TMR13          | 44         | Can be set | 0x0000_00F0    | TMR8 update interrupt/TMR13 global interrupt                    |
| TMR8_TRG_COM_<br>TMR14 | 45         | Can be set | 0x0000_00F4    | TMR8 trigger and communication interrupt/TMR14 global interrupt |
| TMR8_CC                | 46         | Can be set | 0x0000_00F8    | TMR8 capture/compare interrupt                                  |
| DMA1_STR7              | 47         | Can be set | 0x0000_00FC    | DMA1 data stream 7 global interrupt                             |

| Exception type | Vector No. | Priority   | Vector address | Description                                           |
|----------------|------------|------------|----------------|-------------------------------------------------------|
| EMMC           | 48         | Can be set | 0x0000_0100    | EMMC interrupt                                        |
| SDIO           | 49         | Can be set | 0x0000_0104    | SDIO interrupt                                        |
| TMR5           | 50         | Can be set | 0x0000_0108    | TMR5 interrupt                                        |
| SPI3           | 51         | Can be set | 0x0000_010C    | SPI3 interrupt                                        |
| UART4          | 52         | Can be set | 0x0000_0110    | UART4 interrupt                                       |
| UART5          | 53         | Can be set | 0x0000_0114    | UART5 interrupt                                       |
| TMR6_DAC       | 54         | Can be set | 0x0000_0118    | TMR6 interrupt/DAC1 and DAC2 underrun error interrupt |
| TMR7           | 55         | Can be set | 0x0000_011C    | TMR7 interrupt                                        |
| DMA2_STR0      | 56         | Can be set | 0x0000_0120    | DMA2 data stream 0 interrupt                          |
| DMA2_STR1      | 57         | Can be set | 0x0000_0124    | DMA2 data stream 1 interrupt                          |
| DMA2_STR2      | 58         | Can be set | 0x0000_0128    | DMA2 data stream 2 interrupt                          |
| DMA2_STR3      | 59         | Can be set | 0x0000_012C    | DMA2 data stream 3 interrupt                          |
| DMA2_STR4      | 60         | Can be set | 0x0000_0130    | DMA2 data stream 4 interrupt                          |
| ETH            | 61         | Can be set | 0x0000_0134    | Ethernet global interrupt                             |
| ETH_WKUP       | 62         | Can be set | 0x0000_0138    | Ethernet wake-up interrupt through EINT line          |
| CAN2_TX        | 63         | Can be set | 0x0000_013C    | CAN2 transmitting interrupt                           |
| CAN2_RX0       | 64         | Can be set | 0x0000_0140    | CAN2 receiving 0 interrupt                            |
| CAN2_RX1       | 65         | Can be set | 0x0000_0144    | CAN2 receiving 1 interrupt                            |
| CAN2_SCE       | 66         | Can be set | 0x0000_0148    | CAN2 SCE interrupt                                    |

| Exception type | Vector No. | Priority   | Vector address             | Description                                           |
|----------------|------------|------------|----------------------------|-------------------------------------------------------|
| OTG_FS1        | 67         | Can be set | 0x0000_014C                | OTG_FS1 global interrupt                              |
| DMA2_STR5      | 68         | Can be set | 0x0000_0150                | DMA2 data stream 5 interrupt                          |
| DMA2_STR6      | 69         | Can be set | 0x0000_0154                | DMA2 data stream 6 interrupt                          |
| DMA2_STR7      | 70         | Can be set | 0x0000_0158                | DMA2 data stream 7 interrupt                          |
| USART6         | 71         | Can be set | 0x0000_015C                | USART6 global interrupt                               |
| I2C3_EV        | 72         | Can be set | 0x0000_0160                | I2C3 event interrupt                                  |
| I2C3_ER        | 73         | Can be set | 0x0000_0164                | I2C3 error interrupt                                  |
| -              | 74-79      | -          | 0x0000_0168 to 0x0000_017C | Reserved                                              |
| RNG            | 80         | Can be set | 0x0000_0180                | RNG global interrupt                                  |
| FPU            | 81         | Can be set | 0x0000_0184                | FPU global interrupt                                  |
| -              | 82-84      | Can be set | 0x0000_0188 to 0x0000_0190 | Reserved                                              |
| OTG_FS2 WKUP   | 85         | Can be set | 0x0000_0194                | OTG_FS2 triggers wake-up interrupt via the EINT line. |
| OTG_FS2        | 86         | Can be set | 0x0000_0198                | OTG_FS2 global interrupt                              |
| QSPI           | 87         | Can be set | 0x0000_019C                | QSPI global interrupt                                 |

## 9 External Interrupt/Event Controller (EINT)

### 9.1 Introduction

The interrupts/events contain internal interrupt/event and external interrupt/event. In this manual, external interrupt refers to the interrupt/event caused by I/O pin input signal, which is EINTx in interrupt vector table; other interrupts are internal interrupts/events.

The events can be divided into hardware events and software events. Hardware events are generated by external/core hardware signals, while software events are generated by instructions.

Interrupts need to go through the interrupt handler function to handle the work to be processed, while events do not need to go through interrupt handler function, and the preset work can be triggered by hardware. The external events output pulse through events such as GPIO, while the internal events trigger another TMR to work, for example, through update event of one TMR.

### 9.2 Main Characteristics

- (1) Support 23 event/interrupt requests
- (2) Each event/interrupt line can be masked independently
- (3) Each external event/interrupt line can be triggered independently
- (4) Each external interrupt line has dedicated state bit
- (5) Detect external signals whose pulse width is lower than the APB2 clock width

### 9.3 Functional description

#### 9.3.1 "External interrupt and event" classification and difference points

"External interrupt and event" can be classified into external hardware interrupt, external hardware event, external software event, and external software interrupt according to trigger source, configuration and execution process. The differences are shown in the table below:

Table 46 "External Interrupt and Event" Classifications and Differences

| Name                        | Trigger source                                                   | Configuration and execution process                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------------------------|------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| External hardware interrupt | External signal                                                  | <p>(1) Set the trigger mode, allow the interrupt request, and enable corresponding peripheral interrupt line (enable in NVIC).</p> <p>(2) When an edge consistent with the configuration is generated on the external interrupt line, an interrupt request will be generated, and the corresponding suspend bit will be set to 1. Write 1 to the corresponding bit of the pending register and the interrupt request will be cleared.</p> |
| External hardware event     | External signal                                                  | <p>(1) Set the trigger mode and enable the event line.</p> <p>(2) When an edge consistent with the configuration is generated on the external event line, one event request pulse will be generated, and the corresponding pending bit will not be set to 1.</p>                                                                                                                                                                          |
| External software request   | Software interrupt register/transmission event (SEV) instruction | <p>(1) Enable the event line.</p> <p>(2) Write 1 to the software interrupt event register of the corresponding event line to generate an event request pulse, and the corresponding pending bit will not be set to 1.</p>                                                                                                                                                                                                                 |
| External software interrupt | Software interrupt register                                      | <p>(1) Allow interrupt request, and enable the corresponding peripheral interrupt line (enable in NVIC).</p> <p>(2) Write 1 to the software interrupt event register of the corresponding interrupt line to generate an interrupt request, the corresponding pending bit will be set to 1; write 1 to the corresponding bit of the pending register and the interrupt request will be cleared.</p>                                        |

### 9.3.2 Core wake-up

Using WFI and WFE instructions can make the core stop working. When WFI instruction is used, any interrupt can wake up the core; when WFE instruction is used, the core can be awakened up by event.

When interrupt is used for wake-up, the interrupt handler function will be triggered, and normal interrupt configuration can wake up the core. When an event is used to wake up the core, the interrupt handler function will not be triggered, which will reduce the wake-up time.

#### 9.3.2.1 Event wake-up

**Trigger an internal interrupt (internal hardware event) but not trigger the interrupt handler function for wake-up**



- (1) Enable an internal interrupt in the peripheral, but do not enable the corresponding interrupt in NVIC to avoid triggering the interrupt handler function;
- (2) Enable SEVONPEND bit in the system controller of the core, and execute WFE instruction to make the core enter sleep mode;
- (3) Generate an interrupt to wake up the core; when the core recovers from WFE, it is required to clear the pending bit of corresponding peripheral interrupt and the pending bit of peripheral NVIC interrupt channel (clear the pending register in the NVIC interrupt).

#### Wake up through EINT line events (external hardware event)

- (1) Configure EINT line as the event mode;
- (2) Execute WFE instruction to make the core enter the sleep mode;
- (3) Generate an interrupt to wake up the core. When the CPU recovers from WFE, since the pending bit of corresponding event line is not set, it is unnecessary to clear the interrupt pending bit of corresponding peripheral or the NVIC interrupt channel pending bit.

### 9.3.3 External Interrupt and Event Line Mapping

Table 47 External Interrupt and Event Line Mapping

| External Interrupt and Event Channel Name | External Interrupt and Event Line No. |
|-------------------------------------------|---------------------------------------|
| PA0/PB0/PC0/PE0/PF0/PG0/PH0               | EINT 0                                |
| PA1/PB1/PC1/PE1/PF1/PG1/PH1               | EINT 1                                |
| ...                                       | ...                                   |
| PA15/PB15/PC15/PE15/PF15/PG15             | EINT 15                               |
| PVD output                                | EINT 16                               |
| RTC alarm event                           | EINT 17                               |
| OTG_FS1 wake-up event                     | EINT 18                               |
| Ethernet wake-up event                    | EINT 19                               |
| OTG_FS2 wake-up event                     | EINT 20                               |
| RTC tamper and timestamp event            | EINT 21                               |
| RTC wake-up event                         | EINT 22                               |
| Reserved                                  | EINT 23                               |
| Reserved                                  | EINT 24                               |
| Reserved                                  | EINT 25                               |
| Reserved                                  | EINT 26                               |

| External Interrupt and Event Channel Name | External Interrupt and Event Line No. |
|-------------------------------------------|---------------------------------------|
| Reserved                                  | EINT 27                               |
| Reserved                                  | EINT 28                               |
| Reserved                                  | EINT 29                               |
| Reserved                                  | EINT 30                               |
| Reserved                                  | EINT 31                               |

## 9.4 Register address mapping

Table 48 EINT Register Address Mapping

| Register name | Description                                     | Offset address |
|---------------|-------------------------------------------------|----------------|
| EINT_IMASK    | Interrupt mask register                         | 0x00           |
| EINT_EMASK    | Event mask register                             | 0x04           |
| EINT_RTEN     | Enable the rising edge to trigger the register  | 0x08           |
| EINT_FTEN     | Enable the falling edge to trigger the register | 0x0C           |
| EINT_SWINTE   | Software interrupt event register               | 0x10           |
| EINT_IPEND    | Interrupt pending register                      | 0x14           |

## 9.5 Register functional description

### 9.5.1 Interrupt mask register (EINT\_IMASK)

Offset address: 0x00

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                     |
|-------|----------|-----|-----------------------------------------------------------------|
| 22:0  | IMASKx   | R/W | Interrupt Request Mask on Line x (x=0~22)<br>0: Mask<br>1: Open |
| 31:23 | Reserved |     |                                                                 |

### 9.5.2 Event mask register (EINT\_EMASK)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                 |
|-------|----------|-----|-------------------------------------------------------------|
| 22:0  | EMASKx   | R/W | Event Request Mask on Line x (x=0~22)<br>0: Mask<br>1: Open |
| 31:23 | Reserved |     |                                                             |

### 9.5.3 Enable the rising edge trigger register (EINT\_RTEN)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                             |
|-------|----------|-----|-----------------------------------------------------------------------------------------|
| 22:0  | RTENx    | R/W | Rising Trigger Event and Interrupt Enable of Line x (x=0~22)<br>0: Disable<br>1: Enable |
| 31:23 | Reserved |     |                                                                                         |

Note: Since the external wake-up lines are edge triggered, there should be no burr signal on these lines. When writing EINT\_RTEN register, if the rising edge signal is on the external interrupt line, it will not be recognized and the set pending bit will not be set. In the same interrupt line, the rising edge trigger and falling edge trigger can be set at the same time.

### 9.5.4 Enable the falling edge trigger register (EINT\_FTEN)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                              |
|-------|----------|-----|------------------------------------------------------------------------------------------|
| 22:0  | FTENx    | R/W | Falling Trigger Event and Interrupt Enable of Line x (x=0~22)<br>0: Disable<br>1: Enable |
| 31:23 | Reserved |     |                                                                                          |

Note: Since the external wake-up lines are edge triggered, there should be no burr signal on these lines. When writing EINT\_FTEN register, if the rising edge signal is on the external interrupt line, it will not be recognized and the set pending bit will not be set. In the same interrupt line, the rising edge trigger and falling edge trigger can be set at the same time.

### 9.5.5 Software interrupt event register (EINT\_SWINTE)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name                | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|---------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22:0  | SWINTE <sub>x</sub> | R/W | Software Interrupt Event on Line x (x=0~22)<br>This bit can be set to 1 by software, and be cleared by writing 1 to the corresponding bit of EINT_IPEND.<br>When this bit is 0, the pending bit of EINT_IPEND can be set by writing 1. If EINT_IMASK (EINT_EMASK) is set to open the interrupt (event) request, an interrupt (event) will be generated.<br>0: No effect<br>1: Software generates an interrupt (event) |
| 31:23 | Reserved            |     |                                                                                                                                                                                                                                                                                                                                                                                                                       |

### 9.5.6 Interrupt pending register (EINT\_IPEND)

Offset address: 0x14

Reset value: 0xFFFF XXXX

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                          |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22:0  | IPENDx   | RC_W1 | Interrupt Pending Occur of Line x Flag (x=0~22)<br>When an edge-triggered request corresponding to EINT_RTEN/EINT_FTEN occurs on the external interrupt line, it is set to 1 by hardware. It can be cleared to 0 by changing the edge detection polarity or by writing 1 to the bit. |
| 31:23 | Reserved |       |                                                                                                                                                                                                                                                                                      |

## 10 Direct Memory Access (DMA)

### 10.1 Introduction

DMA (Direct Memory Access) can handle high-speed data transmission between peripheral devices and memory or between memory and memory without CPU intervention, thus saving CPU resources for other operations.

The product has two DMA controllers, with 16 data streams. Each data stream corresponds to 8 channels, but each data stream can only use 1 channel at the same time. Each data stream can set priority, and the arbiter can coordinate the priority of corresponding DMA requests of each data stream according to the priority of the data stream.

### 10.2 Main characteristics

- (1) Two DMA; each DMA has 8 data streams, and each data stream has 8 channels
- (2) Dual AHB main interfaces; one is memory interface, and the other is peripheral interface
- (3) There are three data transmission modes: peripheral to memory, memory to peripheral, memory to memory
- (4) Each data stream has a special hardware DMA request for connection
- (5) Support software priority and hardware priority when multiple requests occur at the same time
- (6) Each data stream has 5 event flags and independent interrupts
- (7) Support circular transmission mode
- (8) The number of data transmission is programmable, up to 65535
- (9) The configurable source and target transmission width is byte, half word or word
- (10) Support source and target incremental modes
- (11) The configurable burst increment size can be single, 4, 8 or 16 ticks

### 10.3 Functional description

#### 10.3.1 DMA request

If the peripheral or memory needs to use DMA to transmit data, it is required to first transmit DMA request and wait for DMA approval before data transmission.

Two DMA have 16 data streams in total. Each data stream is connected with different peripheral channels, and each data stream has five event flags (DMA half transmission, DMA transmission completion, DMA transmission error, DMA FIFO error, and direct mode error). The logic of the five event flags may become a separate interrupt request, and they all support software trigger.

When multiple peripherals request the same data stream, it is required to configure the corresponding register to turn on or off the request of each peripheral, so as to ensure that one data stream can only turn on one peripheral request.

Table 49 DMA1 Request Mapping Table

| Peripheral request | Data stream 0       | Data stream 1         | Data stream 2       | Data stream 3         | Data stream 4         | Data stream 5 | Data stream 6        | Data stream 7       |
|--------------------|---------------------|-----------------------|---------------------|-----------------------|-----------------------|---------------|----------------------|---------------------|
| Channel 0          | SPI3_RX             | -                     | SPI3_RX             | SPI2_RX               | SPI2_TX               | SPI3_TX       | -                    | SPI3_TX             |
| Channel 1          | I2C1_RX             | -                     | TMR7_UP             | -                     | TMR7_UP               | I2C1_RX       | I2C1_TX              | I2C1_TX             |
| Channel 2          | TMR4_CH1            | -                     | -                   | TMR4_CH2              | -                     | -             | TMR4_UP              | TMR4_CH3            |
| Channel 3          | -                   | TMR2_UP<br>TMR2_CH3   | I2C3_RX             | -                     | I2C3_TX               | TMR2_CH1      | TMR2_CH2<br>TMR2_CH4 | TMR2_UP<br>TMR2_CH4 |
| Channel 4          | UART5_RX            | USART3_RX             | UART4_RX            | USART3_TX             | UART4_TX              | USART2_RX     | USART2_TX            | UART5_TX            |
| Channel 5          | -                   | -                     | TMR3_CH4<br>TMR3_UP | -                     | TMR3_CH1<br>TMR3_TRIG | TMR3_CH2      | -                    | TMR3_CH3            |
| Channel 6          | TMR5_CH3<br>TMR5_UP | TMR5_CH4<br>TMR5_TRIG | TMR5_CH1            | TMR5_CH4<br>TMR5_TRIG | TMR5_CH2              | -             | TMR5_UP              | -                   |
| Channel 7          | -                   | TMR6_UP               | I2C2_RX             | I2C2_RX               | USART3_TX             | DAC1          | DAC2                 | I2C2_TX             |

Table 50 DMA2 Request Mapping Table

| Peripheral request | Data stream 0 | Data stream 1 | Data stream 2                    | Data stream 3 | Data stream 4                     | Data stream 5 | Data stream 6                    | Data stream 7                     |
|--------------------|---------------|---------------|----------------------------------|---------------|-----------------------------------|---------------|----------------------------------|-----------------------------------|
| Channel 0          | ADC1          | -             | TMR8_CH1<br>TMR8_CH2<br>TMR8_CH3 | -             | ADC1                              | -             | TMR1_CH1<br>TMR1_CH2<br>TMR1_CH3 | -                                 |
| Channel 1          | -             | -             | ADC2                             | ADC2          | -                                 | -             | -                                | -                                 |
| Channel 2          | ADC3          | ADC3          | -                                | -             | -                                 | -             | -                                | -                                 |
| Channel 3          | SPI1_RX       | -             | SPI1_RX                          | SPI1_TX       | QSPI_RX                           | SPI1_TX       | -                                | QSPI_TX                           |
| Channel 4          | -             | -             | USART1_RX                        | SDIO          | -                                 | USART1_RX     | SDIO                             | USART1_TX                         |
| Channel 5          | -             | USART6_RX     | USART6_RX                        | -             | -                                 | -             | USART6_TX                        | USART6_TX                         |
| Channel 6          | TMR1_TRIG     | TMR1_CH1      | TMR1_CH2                         | TMR1_CH1      | TMR1_CH4<br>TMR1_TRIG<br>TMR1_COM | TMR1_UP       | TMR1_CH3                         | -                                 |
| Channel 7          | -             | TMR8_UP       | TMR8_CH1                         | TMR8_CH2      | TMR8_CH3                          | -             | -                                | TMR8_CH4<br>TMR8_TRIG<br>TMR8_COM |



### 10.3.2 Arbitrator

When multiple DMA channel requests occur, an arbiter is needed to manage the response sequence. Management is divided into two stages: the first stage is software stage, which is divided into the highest, high, medium and low priority; the second stage is hardware stage, and under the condition of the same software priority, the lower the data stream number is, the higher the priority is.

### 10.3.3 FIFO

FIFO is used to temporarily store data before the source data is transmitted to the destination address. Each data stream has an independent 4-word FIFO, and the FIFO threshold can be controlled by software to be 1/4, 1/2, 3/4 or full.

There are two DMA transmission modes.

- The first is direct mode, in which a single transmission will be started to the memory immediately after each peripheral requests. If DMA is configured to transmit data from the memory to the peripheral, DMA will store a data in FIFO, and once the peripheral triggers the DMA request, it will transmit the data. The direct mode requires the same data width configuration for the source and destination addresses, and does not support burst mode and memory-to-memory transmission mode.
- The second is FIFO mode, in which, FIFO threshold is configured first, and when the data storage reaches the threshold, FIFO content will be transmitted to the destination address; FIFO mode is applicable when the data width of source address and destination address is different, and it supports burst mode; FIFO can store the data first and output them as required.

### 10.3.4 Port

DMA controller transmits data between the memory and the peripherals through the memory port and the peripheral port. The memory port and peripheral port of DMA2 are connected to AHB matrix bus, and the memory and peripheral of DMA2 can access the internal Flash, internal SRAM, AHB1 peripheral, APB1 peripheral, APB2 peripheral, AHB2 peripheral and external memory; the memory port of DMA1 does not have the access right for AHB2 peripheral compared with DMA2. The peripheral port of DMA1 is only connected to APB1 peripheral, so DMA1 cannot achieve memory-to-memory transmission.

### 10.3.5 DMA initialization parameter configuration

#### 10.3.5.1 Transmission mode

DMA2 supports three transmission modes: peripheral-to-memory mode, memory-to-peripheral mode and memory-to-memory mode. DMA1 supports two transmission modes: peripheral-to-memory and memory-to-peripheral.

The transmission mode can be controlled through DIRCFG bit of DMA\_SCFG register.

### 10.3.5.2 Increment mode

The increment mode of peripheral and memory is controlled through PERIM and MEMIM bits of DMA\_SCFG register. When both bits are set to 1, it is configured as the increment mode and the increment is the value of PERSIZECFG and MENSIZECFG bits of DMA\_SCFG register. The PERSIZECFG and MENSIZECFG bits are used to set the data size of peripheral and memory to byte, half word or word.

### 10.3.5.3 Single transmission and burst mode

Burst transmission refers to the high-speed transmission that increases the data volume transmitted each time at the transmission stage so as to improve the transmission speed. In the process of burst transmission, AHB bus will be occupied.

Single and burst transmissions can be controlled through the PBCFG and MBCFG bits of DMA\_SCFG register, and it can be configured as single transmission, incremental burst transmission of 4 ticks, incremental burst transmission of 8 ticks and incremental burst transmission of 16 ticks. This increment is determined by the value of PERSIZECFG and MENSIZECFG bits. The burst mode can be enabled only when the increment mode is supported.

The burst mode shall be used in combination with FIFO, and the selected FIFO threshold shall be suitable for the burst size of memory, as shown in the table below.

Table 51 FIFO Threshold Configuration

| MENSIZECFG | FIFO threshold | MBCFG=01                    | MBCFG=10                  | MBCFG=11                   |
|------------|----------------|-----------------------------|---------------------------|----------------------------|
| Byte       | 1/4            | One-time burst of 4 ticks   | Disable                   | Disable                    |
|            | 1/2            | Two-time burst of 4 ticks   | One-time burst of 8 ticks |                            |
|            | 3/4            | Three-time burst of 4 ticks | Disable                   |                            |
|            | Full           | Four-time burst of 4 ticks  | Two-time burst of 8 ticks | One-time burst of 16 ticks |
| Half word  | 1/4            | Disable                     | Disable                   | Disable                    |
|            | 1/2            | One-time burst of 4 ticks   |                           |                            |
|            | 3/4            | Disable                     |                           |                            |
|            | Full           | Two-time burst of 4 ticks   | One-time burst of 8 ticks |                            |
| Word       | 1/4            | Disable                     | Disable                   |                            |
|            | 1/2            |                             |                           |                            |

| MENSIZECFG | FIFO threshold | MBCFG=01                  | MBCFG=10 | MBCFG=11 |
|------------|----------------|---------------------------|----------|----------|
|            | 3/4            |                           |          |          |
|            | Full           | One-time burst of 4 ticks |          |          |

#### 10.3.5.4 Circular mode

The circular mode is used to process the circular buffer area and continuous data stream. The circular mode will automatically configure the number of data items as the initial value after the transmission ends, and continue the data transmission.

The circular mode can be controlled through CIRC MEN bit of DMA\_SCFG register.

#### 10.3.5.5 Double-buffer mode

Set DBM of DMA\_SCFG register to 1 to turn on the double- buffer mode and automatically activate the circular mode. In the double-buffer mode, the DMA\_M1ADDR register is activated, and when the corresponding memory area of the address pointer of DMA\_M0ADDR register finishes transmission, the corresponding memory area of the address pointer of DMA\_M1ADDR register will continue to transmit and be called circularly. When DMA accesses DMA\_M1ADDR, CTARG bit of DMA\_SCFG register will be set to 1 and can write or read data to DMA\_M0ADDR register at the same time.

This mode does not support memory-to-memory transmission.

#### 10.3.5.6 Stream controller

The stream controller can be configured as DMA or peripheral through PERFC bit of DMA\_SCFG register.

When DMA is used as the stream controller, configure DMA\_NDATA register before enabling data stream, and set the number of data items to be transmitted.

When the peripheral is used as the stream controller, the number of transmitted data items is unknown, and the hardware will force the value of DMA\_NDATA register to 0xFFFF for execution. After the transmission is completed, the peripheral will transmit instructions to DMA through hardware, and then read the value of the register. The number of transmitted data=0xFFFF-DMA\_NDATA.

When the peripheral is used as the stream controller, the circular mode is disabled. When the memory-to-memory mode is selected, the PERFC bit will be forced to be cleared to zero by the hardware, and only DMA can be selected as the stream controller.

### 10.3.6 Interrupt

Each data stream has five types of interrupt events: half transmission, transmission completion, transmission error, FIFO error and direct mode error.

Table 52 DMA Interrupt Request

| Interrupt event        | Event flag bit | Enable interrupt bit |
|------------------------|----------------|----------------------|
| Half transmission      | HTXIFLGx       | HTXIEN               |
| Transmission completed | TXCIFLGx       | TXCIEN               |
| Transmission error     | TXEIFLGx       | TXEIEN               |
| FIFO error             | FEIFLGx        | FEIEN                |
| Direct mode error      | DMEIFLGx       | DMEIEN               |

## 10.4 DMA register address mapping

Table 53 DMA Register Address Mapping

| Register name | Description                                   | Offset address                  |
|---------------|-----------------------------------------------|---------------------------------|
| DMA_LINTSTS   | DMA low interrupt state register              | 0x00                            |
| DMA_HINTSTS   | DMA high interrupt state register             | 0x04                            |
| DMA_LIFCLR    | DMA low interrupt flag clear register         | 0x08                            |
| DMA_HIFCLR    | DMA high interrupt flag clear register        | 0x0C                            |
| DMA_SCFG      | DMA data stream x configuration register      | 0x10+0x18× (data stream number) |
| DMA_NDATA     | DMA data stream x data item number register   | 0x14+0x18× (data stream number) |
| DMA_PADDR     | DMA data stream x peripheral address register | 0x18+0x18× (data stream number) |
| DMA_M0ADDR    | DMA data stream x memory 0 address register   | 0x1C+0x18× (data stream number) |
| DMA_M1ADDR    | DMA data stream x memory 1 address register   | 0x20+0x18× (data stream number) |
| DMA_FCTRL     | DMA data stream x FIFO control register       | 0x24+0x18× (data stream number) |

## 10.5 Register functional description

### 10.5.1 DMA low interrupt state register (DMA\_LINTSTS)

Offset address: 0x00

Reset value: 0x0000 0000

| Field       | Name     | R/W | Description                                                                                                                                                                                                                                                            |
|-------------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22、16、6、0   | FEIFLGx  | R   | Stream x FIFO Error Interrupt Flag (x=0...3)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_LIFCLR register.<br>0: No FIFO error event<br>1: FIFO error event occurs                                         |
| 23、17、7、1   | Reserved |     |                                                                                                                                                                                                                                                                        |
| 24、18、8、2   | DMEIFLGx | R   | Stream x Direct Mode Error Interrupt Flag (x=0...3)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_LIFCLR register.<br>0: No direct mode error<br>1: Direct mode error is generated                          |
| 25、19、9、3   | TXEIFLGx | R   | Stream x Transfer Error Interrupt Flag (x=0...3)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_LIFCLR register.<br>0: No transmission error<br>1: Transmission error is generated                           |
| 26、20、10、4  | HTXIFLGx | R   | Stream x Half Transfer Interrupt Flag (x=0...3)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_LIFCLR register.<br>0: No half-transmission event<br>1: Half-transmission event is generated                  |
| 27、21、11、5  | TXCIFLGx | R   | Stream x Transfer Complete Interrupt Flag (x=0...3)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_LIFCLR register.<br>0: No transmission completion event<br>1: Transmission completion event is generated. |
| 31:28、15:12 | Reserved |     |                                                                                                                                                                                                                                                                        |

### 10.5.2 DMA high interrupt state register (DMA\_HINTSTS)

Offset address: 0x04

Reset value: 0x0000 0000

| Field     | Name     | R/W | Description                                                                                                                                                                                                                                   |
|-----------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22、16、6、0 | FEIFLGx  | R   | Stream x FIFO Error Interrupt Flag (x=4...7)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_HIFCLR register.<br>0: No FIFO error event<br>1: FIFO error event occurs                |
| 23、17、7、1 | Reserved |     |                                                                                                                                                                                                                                               |
| 24、18、8、2 | DMEIFLGx | R   | Stream x Direct Mode Error Interrupt Flag (x=4...7)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_HIFCLR register.<br>0: No direct mode error<br>1: Direct mode error is generated |

| Field       | Name     | R/W | Description                                                                                                                                                                                                                                                            |
|-------------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25、19、9、3   | TXEIFLGx | R   | Stream x Transfer Error Interrupt Flag (x=4...7)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_HIFCLR register.<br>0: No transmission error<br>1: Transmission error is generated                           |
| 26、20、10、4  | HTXIFLGx | R   | Stream x Half Transfer Interrupt Flag (x=4...7)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_HIFCLR register.<br>0: No half-transmission event<br>1: Half-transmission event is generated                  |
| 27、21、11、5  | TXCIFLGx | R   | Stream x Transfer Complete Interrupt Flag (x=4...7)<br>These bits are set to 1 by hardware; write 1 and set to 0 by software on the corresponding bit of DMA_HIFCLR register.<br>0: No transmission completion event<br>1: Transmission completion event is generated. |
| 31:28、15:12 | Reserved |     |                                                                                                                                                                                                                                                                        |

### 10.5.3 DMA low interrupt flag clear register (DMA\_LIFCLR)

Offset address: 0x08

Reset value: 0x0000 0000

| Field       | Name      | R/W | Description                                                                                                                                           |
|-------------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22、16、6、0   | CFEIFLGx  | W   | Stream x Clear FIFO Error Interrupt Flag (x=0...3)<br>0: Invalid<br>1: The corresponding FEIFLGx flag in DMA_LINTSTS register is set to 0             |
| 23、17、7、1   | Reserved  |     |                                                                                                                                                       |
| 24、18、8、2   | CDMEIFLGx | W   | Stream x Clear Direct Mode Error Interrupt Flag (x=0...3)<br>0: Invalid<br>1: The corresponding DMEIFLGx flag in DMA_LINTSTS register is cleared to 0 |
| 25、19、9、3   | CTXEIFLGx | W   | Stream x Clear Transfer Error Interrupt Flag (x=0...3)<br>0: Invalid<br>1: The corresponding TXEIFLGx flag in DMA_LINTSTS register is cleared to 0    |
| 26、20、10、4  | CHTXIFLGx | W   | Stream x Clear Half Transfer Interrupt Flag (x=0...3)<br>0: Invalid<br>1: The corresponding HTXIFLGx flag in DMA_LINTSTS register is cleared to 0     |
| 27、21、11、5  | CTXCIFLGx | W   | Stream x Clear Transfer Complete Interrupt Flag (x=0...3)<br>0: Invalid<br>1: The corresponding TXCIFLGx flag in DMA_LINTSTS register is cleared to 0 |
| 31:28、15:12 | Reserved  |     |                                                                                                                                                       |

### 10.5.4 DMA high interrupt flag clear register (DMA\_HIFCLR)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field       | Name      | R/W | Description                                                                                                                                           |
|-------------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22、16、6、0   | CFEIFLGx  | W   | Stream x Clear FIFO Error Interrupt Flag (x=4...7)<br>0: Invalid<br>1: The corresponding FEIFLGx flag in DMA_HINTSTS register is cleared to 0         |
| 23、17、7、1   | Reserved  |     |                                                                                                                                                       |
| 24、18、8、2   | CDMEIFLGx | W   | Stream x Clear Direct Mode Error Interrupt Flag (x=4...7)<br>0: Invalid<br>1: The corresponding DMEIFLGx flag in DMA_HINTSTS register is cleared to 0 |
| 25、19、9、3   | CTXEIFLGx | W   | Stream x Clear Transfer Error Interrupt Flag (x=4...7)<br>0: Invalid<br>1: The corresponding TXEIFLGx flag in DMA_HINTSTS register is cleared to 0    |
| 26、20、10、4  | CHTXIFLGx | W   | Stream x Clear Half Transfer Interrupt Flag (x=4...7)<br>0: Invalid<br>1: The corresponding HTXIFLGx flag in DMA_HINTSTS register is cleared to 0     |
| 27、21、11、5  | CTXCIFLGx | W   | Stream x Clear Transfer Complete Interrupt Flag (x=4...7)<br>0: Invalid<br>1: The corresponding TXCIFLGx flag in DMA_HINTSTS register is cleared to 0 |
| 31:28、15:12 | Reserved  |     |                                                                                                                                                       |

#### 10.5.5 DMA data stream x configuration register (DMA\_SCFG) (x=0...7)

Offset address: 0x10+0x18× (data stream number)

Reset value: 0x0000 0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                           |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | EN     | R/W | Stream Enable<br>0: Disable<br>1: Enable<br>This bit shall be set to 0 by hardware in any of the following situations:<br>1. When DMA transmission ends<br>2. When transmission error occurs to AHB main bus<br>3. When the FIFO threshold on the memory AHB port is incompatible with the burst size |
| 1     | DMEIEN | R/W | Direct Mode Error Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                         |
| 2     | TXEIEN | R/W | Transfer Error Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                            |
| 3     | HTXIEN | R/W | Half Transfer Interrupt Enable<br>0: Disable                                                                                                                                                                                                                                                          |

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |            |     | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 4     | TXCIEN     | R/W | Transfer Complete Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                  |
| 5     | PERFC      | R/W | Peripheral Flow Controller<br>0: DMA is stream controller<br>1: The peripheral is stream controller<br>This bit can be written only when the EN bit is 0; when the memory-to-memory mode is selected, this bit will be automatically forced to zero by the hardware.                                                                                                                                                           |
| 7:6   | DIRCFG     | R/W | Configure data transfer direction (Data Transfer Direction Configure)<br>00: From peripheral to memory<br>01: From memory to peripheral<br>10: From memory to memory<br>11: Reserved<br>These bits can be written only when EN bit is 0.                                                                                                                                                                                       |
| 8     | CIRCMEN    | R/W | Circular Mode Enable<br>This bit can be set to 1 or 0 by software, or be set to 0 by hardware.<br>0: Disable<br>1: Enable<br>If the peripheral is set as the stream controller and the data stream is enabled, this bit will be automatically forced to 0 by hardware.<br>If DMA transmission is ended, switch the target memory area, enable the data stream, and this bit will be automatically forced to 1 by the hardware. |
| 9     | PERIM      | R/W | Peripheral Increment Mode<br>0: The peripheral address pointer is fixed<br>1: After each data transmission, the peripheral address pointer will increase<br>This bit can be written only when EN bit is 0.                                                                                                                                                                                                                     |
| 10    | MEMIM      | R/W | Memory Increment Mode<br>0: The memory address pointer is fixed<br>1: After each data transmission, the memory address pointer will increase<br>This bit can be written only when EN bit is 0.                                                                                                                                                                                                                                 |
| 12:11 | PERSIZECFG | R/W | Peripheral Data Size Configure<br>00: Byte (8 bits)<br>01: Half word (16 bits)<br>10: Word (32 bits)<br>11: Reserved<br>These bits can be written only when EN bit is 0.                                                                                                                                                                                                                                                       |
| 14:13 | MEMSIZECFG | R/W | Memory Data Size Configure<br>00: Byte (8 bits)<br>01: Half word (16 bits)                                                                                                                                                                                                                                                                                                                                                     |



| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |           |     | 10: Word (32 bits)<br>11: Reserved<br>These bits can be written only when EN bit is 0.<br>In direct mode, when EN bit is 1, MEMSIZECFG bit will be forced to be of the same value as that of PERSIZECFG bit.                                                                                                                                                                                                                                          |
| 15    | PERIOSIZE | R/W | Peripheral increment offset size<br>0: The offset used to calculate the peripheral address is related to PERSIZECFG<br>1: The offset used to calculate the peripheral address is fixed to 4<br>If PERIM bit is 0, this bit is meaningless, and it can be written only when EN bit is 0.<br>If the direct mode is selected or the PBCFG bit is not configured to 00, and the data stream is enabled, this bit will be forced to low level by hardware. |
| 17:16 | PRILCFG   | R/W | Priority Level Configure<br>00: Low<br>01: Medium<br>10: High<br>11: Very high<br>These bits can be written only when EN bit is 0.                                                                                                                                                                                                                                                                                                                    |
| 18    | DBM       | R/W | Double Buffer Mode<br>0: Do not switch the buffer when the transmission ends<br>1: Switch the target memory when DMA transmission ends<br>This bit can be written only when EN bit is 0.                                                                                                                                                                                                                                                              |
| 19    | CTARG     | R/W | Current Target (only in double buffer mode)<br>This bit can be set to 1 or 0 by hardware, or be written by software.<br>0: The current target memory is Memory 0<br>1: The current target memory is Memory 1                                                                                                                                                                                                                                          |
| 20    | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 22:21 | PBCFG     | R/W | Peripheral Burst Transfer Configure<br>00: Single transmission<br>01: INCR4 (4-tick increment burst transmission)<br>10: INCR8 (8-tick increment burst transmission)<br>11: INCR16 (16-tick increment burst transmission)<br>This bit can be written only when EN bit is 0.<br>In direct mode, these bits will be forced to 0.                                                                                                                        |
| 24:23 | MBCFG     | R/W | Memory Burst Transfer Configure<br>00: Single transmission<br>01: INCR4 (4-tick increment burst transmission)<br>10: INCR8 (8-tick increment burst transmission)<br>11: INCR16 (16-tick increment burst transmission)<br>This bit can be written only when EN bit is 0.<br>In direct mode, these bits will be forced to 0.                                                                                                                            |
| 27:25 | CHSEL     | R/W | Channel Selection<br>000: Select Channel 0                                                                                                                                                                                                                                                                                                                                                                                                            |

| Field | Name     | R/W | Description                                                                                                                                                                 |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 001: Select Channel 1<br>010: Select Channel 2<br>011: Select Channel 3<br>100: Select Channel 4<br>101: Select Channel 5<br>110: Select Channel 6<br>111: Select Channel 7 |
| 31:28 | Reserved |     |                                                                                                                                                                             |

### 10.5.6 DMA data stream x data item number register (DMA\_NDATA) (x=0...7)

Offset address: 0x14+0x18× (data stream number)

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | NDATA    | R/W | Number of Data Items to Transfer<br>The number of data items to be transmitted is 0-65535. This register can be operated only when the data stream is disabled. After the data stream is enabled, this register is read-only to indicate the number of remaining data items to be transmitted. After each DMA transmission, this register will decrease.<br>This register is 0 after completion of transmission, and the initial value will be automatically reloaded in any of the following circumstances:<br>1. Configure the data stream in circular mode<br>2. Re-enable the data stream |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

### 10.5.7 DMA data stream x peripheral address register (DMA\_PADDR) (x=0...7)

Offset address: 0x18+0x18× (data stream number)

Reset value: 0x0000 0000

| Field | Name  | R/W | Description                                                                                                                          |
|-------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | PADDR | R/W | Peripheral Address<br>Base address of peripheral data register of read/write data.<br>This bit can be written only when EN bit is 0. |

### 10.5.8 DMA data stream x memory 0 address register (DMA\_M0ADDR) (x=0...7)

Offset address: 0x1C+0x18× (data stream number)

Reset value: 0x0000 0000

| Field | Name   | R/W | Description                                                                                                                                                                                 |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | M0ADDR | R/W | Memory 0 Address<br>Base address of memory 0 of read/write data.<br>These bits are write-protected, and can be written only in any of the following circumstances:<br>● Disable data stream |

| Field | Name | R/W | Description                                                                                                          |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------|
|       |      |     | <ul style="list-style-type: none"> <li>Enable the data stream and set CTARG bit of DMA_SCFG register to 1</li> </ul> |

### 10.5.9 DMA data stream x memory 1 address register (DMA\_M1ADDR) (x=0...7)

Offset address: 0x20+0x18× (data stream number)

Reset value: 0x0000 0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | M1ADDR | R/W | <p>Memory 1 Address</p> <p>Base address of memory 1 of read/write data.</p> <p>This register is only applicable to double-buffer mode.</p> <p>These bits are write-protected, and can be written only in any of the following circumstances:</p> <ul style="list-style-type: none"> <li>Disable data stream</li> <li>Enable the data stream and set CTARG bit of DMA_SCFG register to 0</li> </ul> |

### 10.5.10 DMA data stream x xFIFO control register (DMA\_FCTRL) (x=0...7)

Offset address: 0x24+0x18× (data stream number)

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | FTHSEL   | R/W | <p>FIFO Threshold Select</p> <p>00: 1/4 of FIFO capacity</p> <p>01: 1/2 of FIFO capacity</p> <p>10: 3/4 of FIFO capacity</p> <p>11: Full FIFO capacity</p> <p>In direct mode, these bits are invalid, and they can be written only when EN bit is 1.</p>                                          |
| 2     | DMDEN    | R/W | <p>Direct Mode Disable</p> <p>0: Enable direct mode</p> <p>1: Disable direct mode</p> <p>This bit can be written only when the EN bit is 0. When the memory-to-memory mode is selected and EN bit is 1, this bit will be set to 1 by hardware.</p>                                                |
| 5:3   | FSTS     | R   | <p>FIFO Status</p> <p>000: 0&lt;fifo_level&lt;1/4</p> <p>001: 1/4&lt;fifo_level&lt;1/2</p> <p>010: 1/2&lt;fifo_level&lt;3/4</p> <p>011: 3/4&lt;fifo_level&lt;full</p> <p>100: FIFO is empty</p> <p>101: FIFO is full</p> <p>Others: Meaningless</p> <p>These bits are invalid in direct mode.</p> |
| 6     | Reserved |     |                                                                                                                                                                                                                                                                                                   |

| Field | Name     | R/W | Description                                            |
|-------|----------|-----|--------------------------------------------------------|
| 7     | FEIEN    | R/W | FIFO Error Interrupt Enable<br>0: Disable<br>1: Enable |
| 31:8  | Reserved |     |                                                        |

# 11 Debug MCU (DBGMCU)

## 11.1 Full name and abbreviation description of terms

Table 54 Full name and abbreviation description of terms

| Full name in English        | English abbreviation |
|-----------------------------|----------------------|
| Frame Clock                 | FCLK                 |
| Serial Wire/JTAG Debug Port | SWJ-DP               |

## 11.2 Introduction

APM32F425xG\_F427xG MCU series uses Arm® Cortex® -M4F core, and Arm® Cortex® -M4F core includes hardware debug module and supports complex debug operation. During debugging, the module can make the running core stop at breakpoint, and achieve the effect of querying the internal state of the core and the external state of the system. After the query is completed, the core and peripheral operation can be restored to continue to execute the program.

Two debug interfaces are supported:

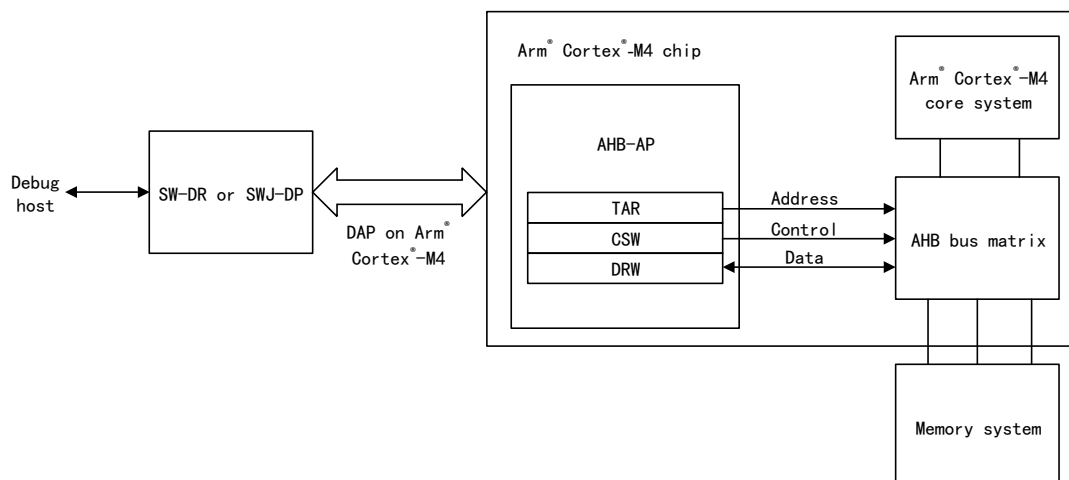
- Serial interface
- JTAG debug interface

Note: The hardware debug interface included in Arm® Cortex® -M4F core is subset of Arm CoreSight development tool set. Please refer to *Cortex®-M4F (Version r1p1) Technical Reference Manual* (TRM) and CoreSight development tool set (Version r1p0) TRM for more information about debug function of Arm® Cortex®-M4F core.

## 11.3 Main characteristics

- (1) Replace the core to access AHB bus matrix
- (2) Flexible debug pin assignment
- (3) MCU debug box (support low-power mode, control peripheral clock, etc.)

Figure 12 APM32F425xG\_F427xG Level and Arm® Cortex® -M4F Level Debugging Block Diagram



## 11.4 Functional description

### 11.4.1 Debug pin function configuration

- (1) Achieve the on-line programming and debugging of the chip.
- (2) Use KEIL/IAR software to achieve on-line debugging, downloading and programming.
- (3) Flexible implementation of the off-line programmer.

Table 55 Pin Function Configuration

| Pin name | JTAG debug port |      |                          | SW debug port |      |                               |
|----------|-----------------|------|--------------------------|---------------|------|-------------------------------|
|          | Name            | Type | Description              | Name          | Type | Description                   |
| PA13     | JTMS            | I    | JTAG test mode selection | SWDIO         | I/O  | Serial wire data input/output |
| PA14     | JTCK            | I    | JTAG test clock          | SWCLK         | I    | Serial wire clock input       |
| PA15     | JTDI            | I    | JTAG test data input     | -             | -    | -                             |
| PB3      | JTDO            | O    | JTAG test data output    | TRACES WO     | O    | Serial wire data output       |
| PB4      | NJTRST          | I    | JTAG test nReset         | -             | -    | -                             |

### 11.4.2 ID code

#### 11.4.2.1 MCU device ID code

APM32F MCU series includes a MCU ID code. It can be accessed with JTAG or SW debug interface or user code.

### 11.4.2.2 Boundary scan TAP

#### JTAG ID code

The boundary scan TAP of APM32F MCU series integrates JTAG ID code. For APM32F425xG\_F427xG series products, its JTAG ID code is 0x04190B47, which is 4 bits revision count + 12 bits Device ID + 4 bits 0 + 12 bits company code.

### 11.4.2.3 Arm® Cortex®-M4F TAP

Arm® Cortex® -M4F TAP has a JTAG ID code, which is 0x4BA00477.

### 11.4.2.4 Arm® Cortex® -M4F JEDEC-106 ID code

Arm® Cortex® -M4F has a JEDEC-106 ID code. It is located in 4KB ROM table in which the internal PPB bus address is 0xE0042000.

## 11.5 Register address mapping

Table 56 Register Address Mapping

| Register name | Description                      | Address     |
|---------------|----------------------------------|-------------|
| DBGMCU_IDCODE | Device ID register               | 0xE004 2000 |
| DBGMCU_CFG    | Debug MCU configuration register | 0xE004 2004 |
| DBGMCU_APB1F  | Debug MCU APB1 freeze register   | 0xE004 2008 |
| DBGMCU_APB2F  | Debug MCU APB2 freeze register   | 0xE004 200C |

## 11.6 Register functional description

### 11.6.1 Device ID register (DBGMCU\_IDCODE)

Address: 0xE004 2000

Reset value: 0XXXXX XXXX, X=undefined bit

Only support 32-bit access

| Field | Name     | R/W | Description                                                                                                                         |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------|
| 11:0  | EQR      | R   | Equipment Recognition<br>APM32F425xG_F427xG series products: 0x419<br>The debugger/programming tool identifies chips by EQR (11:0). |
| 15:12 | Reserved |     |                                                                                                                                     |
| 31:16 | WVR      | R   | Wafer Version Recognition<br>This domain identifies wafer information<br>APM32F425xG_F427xG series products<br>Version A: 0x1000    |

### 11.6.2 Debug MCU configuration register (DBGMCU\_CFG)

Address: 0xE004 2004

Reset value: 0x0000 0000 (not affected by system reset, only power-on reset)

This register can configure MCU in debug mode. It includes the counters supporting timer and watchdog, low-power mode, CAN communication and allocation of tracking pins.

Only support 32-bit access.

| Field | Name            | R/W | Description                                                                                                                                                                                                                                                            |
|-------|-----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | SLEEP_CLK_STS   | R/W | Configure Clock Status When MCU is Debugged in Sleep Mode<br>0: FCLK ON, HCLK OFF<br>1: FCLK ON, HCLK ON, provided by system clock                                                                                                                                     |
| 1     | STOP_CLK_STS    | R/W | Configure Clock Status When MCU is Debugged in Stop Mode<br>0: FCLK OFF, HCLK OFF<br>1: FCLK ON, HCLK ON, provided by HSICLK                                                                                                                                           |
| 2     | STANDBY_CLK_STS | R/W | Configure Clock Status When MCU is Debugged in Standby Mode<br>0: FCLK OFF, HCLK OFF<br>1: FCLK ON, HCLK ON, provided by HSICLK                                                                                                                                        |
| 4:3   | Reserved        |     |                                                                                                                                                                                                                                                                        |
| 5     | TRACE_IOEN      | R/W | Trace Debug Pin Enable<br>0: Tracking debug pin disabled<br>1: Tracking debug pin enabled                                                                                                                                                                              |
| 7:6   | TRACE_MODE      | R/W | Trace Debug Pin Mode Configure<br>Tracking debug pin mode can be configured only when TRACE_IOEN=1:<br>00: Asynchronous mode<br>01: Synchronous mode, the data length is 1<br>10: Synchronous mode, the data length is 2<br>11: Synchronous mode, the data length is 4 |
| 31:8  | Reserved        |     |                                                                                                                                                                                                                                                                        |

### 11.6.3 Debug MCU APB1 freeze register (DBGMCU\_APB1F)

Address: 0xE004 2008

Reset value: 0x0000 (unaffected by system reset)

This register is used to configure MCU during debugging.

Involve some APB peripherals:

- Freeze the timer counter
- Freeze I2C SMBus timeout
- Freeze supporting system window regulators and independent watchdog counters

This register is reset asynchronously by POR (instead of system reset) and can be written by the debugger through system reset.

Only support 32-bit access.



| Field | Name      | R/W | Description                                                                                                                                                            |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TMR2_STS  | R/W | Configure TMR2 Work Status When Core is in Halted<br>Whether TMR2 timer continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working       |
| 1     | TMR3_STS  | R/W | Configure Timer3 Work Status When Core is in Halted<br>Whether TMR3 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working   |
| 2     | TMR4_STS  | R/W | ConfigureTimer4 Work Status When Core is in Halted<br>Whether TMR4 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working    |
| 3     | TMR5_STS  | R/W | ConfigureTimer5 Work Status When Core is in Halted<br>Whether TMR5 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working    |
| 4     | TMR6_STS  | R/W | Configure Timer6 Work Status When Core is in Halted<br>Whether TMR6 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working   |
| 5     | TMR7_STS  | R/W | Configure Timer7 Work Status When Core is in Halted<br>Whether TMR7 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working   |
| 6     | TMR12_STS | R/W | ConfigureTimer12 Work Status When Core is in Halted<br>Whether TMR12 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working  |
| 7     | TMR13_STS | R/W | ConfigureTimer13 Work Status When Core is in Halted<br>Whether TMR13 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working  |
| 8     | TMR14_STS | R/W | Configure Timer14 Work Status When Core is in Halted<br>Whether TMR14 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working |
| 9     | Reserved  |     |                                                                                                                                                                        |

| Field | Name                   | R/W | Description                                                                                                                                                                                             |
|-------|------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10    | RTC_STS                | R/W | Configure RTC Work Status When Core is in Halted<br>Whether RTC counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working                                        |
| 11    | WWDT_STS               | R/W | Configure Window Watchdog Work Status When Core is in Halted<br>Whether WWDT counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working                           |
| 12    | IWDT_STS               | R/W | Configure Independent Watchdog Work Status When Core is in Halted<br>Whether IWDT counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working                      |
| 20:13 | Reserved               |     |                                                                                                                                                                                                         |
| 21    | I2C1_SMBUS_TIMEOUT_STS | R/W | Configure I2C1_SMBUS_TIMEOUT Work Status When Core is in Halted<br>Whether I2C1_SMBUS_TIMEOUT continues to work when the core stops working.<br>0: Work normally<br>1: Freeze the timeout mode of SMBUS |
| 22    | I2C2_SMBUS_TIMEOUT_STS | R/W | Configure I2C2_SMBUS_TIMEOUT Work Status When Core is in Halted<br>Whether I2C2_SMBUS_TIMEOUT continues to work when the core stops working.<br>0: Work normally<br>1: Freeze the timeout mode of SMBUS |
| 23    | I2C3_SMBUS_TIMEOUT_STS | R/W | Configure I2C3_SMBUS_TIMEOUT Work Status When Core is in Halted<br>Whether I2C3_SMBUS_TIMEOUT continues to work when the core stops working.<br>0: Work normally<br>1: Freeze the timeout mode of SMBUS |
| 24    | Reserved               |     |                                                                                                                                                                                                         |
| 25    | CAN1_STS               | R/W | Configure Controller Area Network 1 Work Status When Core is in Halted<br>Whether CAN1 continues to work when the core stops working.<br>0: Work normally<br>1: Freeze CAN1 receiving register          |
| 26    | CAN2_STS               | R/W | Configure Controller Area Network 2 Work Status When Core is in Halted<br>Whether CAN2 continues to work when the core stops working.<br>0: Work normally<br>1: Freeze CAN2 receiving register          |

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 31:27 | Reserved |     |             |

#### 11.6.4 Debug MCU APB2 freeze register (DBGMCU\_APB2F)

Address: 0xE004 200C

Reset value: 0x0000 (unaffected by system reset)

This register is used to configure MCU during debugging.

Involve some APB peripherals:

- Freeze the timer counter

This register is reset asynchronously by POR (instead of system reset) and can be written by the debugger through system reset.

Only support 32-bit access.

| Field | Name      | R/W | Description                                                                                                                                                          |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TMR1_STS  | R/W | Configure Timer1 Work Status When Core is in Halted<br>Whether TMR1 counter continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working |
| 1     | TMR8_STS  | R/W | Configure Timer8 Work Status When Core is in Halted<br>Whether TMR8 continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working         |
| 15:2  | Reserved  |     |                                                                                                                                                                      |
| 16    | TMR9_STS  | R/W | Configure Timer9 Work Status When Core is in Halted<br>Whether TMR9 continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working         |
| 17    | TMR10_STS | R/W | Configure Timer10 Work Status When Core is in Halted<br>Whether TMR10 continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working       |
| 18    | TMR11_STS | R/W | Configure Timer11 Work Status When Core is in Halted<br>Whether TMR11 continues to work when the core stops working.<br>0: Continue to work<br>1: Stop working       |
| 31:19 | Reserved  |     |                                                                                                                                                                      |

## 12 General-purpose Input/Output Pin (GPIO)

### 12.1 Full name and abbreviation description of terms

Table 57 Full name and abbreviation description of terms

| Full name in English                | English abbreviation |
|-------------------------------------|----------------------|
| P-channel Metal Oxide Semiconductor | P-MOS                |
| N-channel Metal Oxide Semiconductor | N-MOS                |

### 12.2 Main characteristics

GPIO port can configure the following functions through 32-bit configuration register (GPIOx\_CFGLOW/GPIOx\_CFGHIG) and two 32-bit data registers (GPIOx\_IDATA/GPIOx\_ODATA):

- (1) Input mode
  - Analog input
  - Floating input
  - Pull-up input
  - Pull-down input
- (2) Output mode
  - Push-pull output
  - Open-drain output
  - Configurable maximum output rate
- (3) Multiplexing mode
  - Push-pull multiplexing function
  - Open-drain multiplexing function
- (4) Analog function
- (5) GPIO can be used as external interrupt/wake-up line
- (6) Support locking I/O configuration function



- Disable output buffer
- Connect weak pull-up and pull-down resistors according to different input configurations
- The input data register GPIOx\_IDATA captures the data on I/O pin in each AHB1 clock cycle
- Read I/O state through the input data register GPIOx\_IDATA

The initial level state of the floating input mode is uncertain and is easy to be disturbed by the outside; when connecting the equipment, it is determined by the external input level (except for the very high impedance).

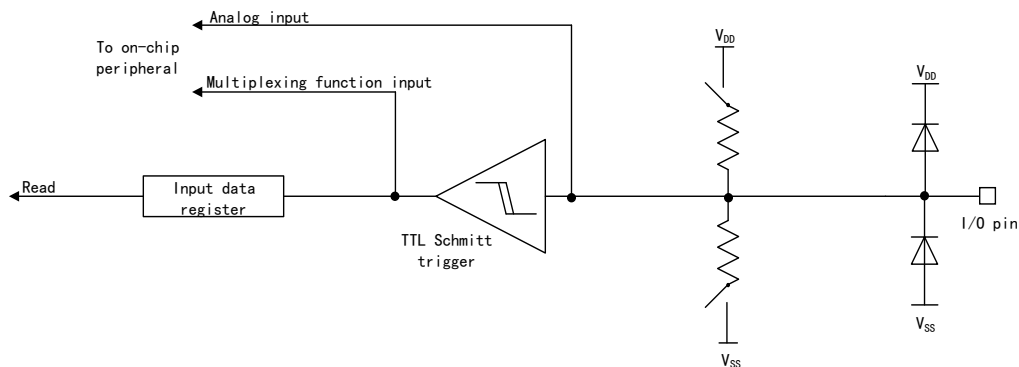
The initial level state of pull-up/pull-down input mode is high level if pull-up, and low level if pull-down; when connecting the equipment, it is determined by the external input level and load impedance.

### Analog input mode

In analog input mode

- Disable output buffer
- The input of Schmitt trigger is disabled, and the output value of Schmitt trigger is forced to be 0
- Weak pull-up and pull-down resistors are disabled
- The value of port input state register is 0

Figure 14 Input Mode Structure



### 12.4.3 Output mode

In the output mode, it can be set as push-pull output and open-drain output.

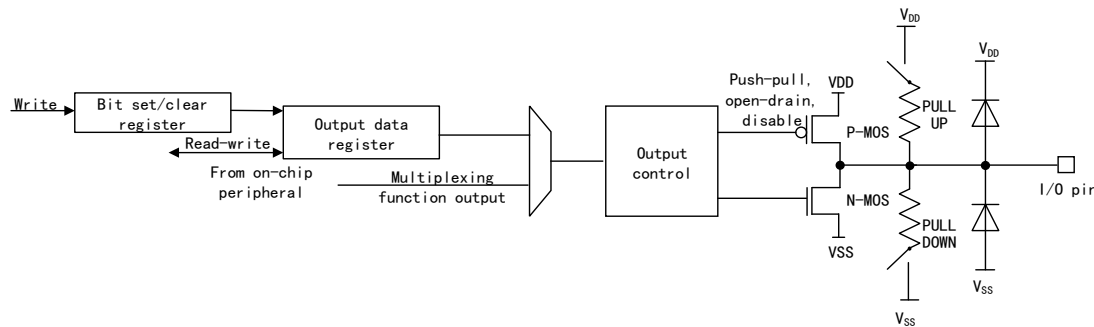
When GPIO is configured as the output pin, the output speed of the port can be configured and the output drive mode (push-pull / open-drain) can be selected.

In output mode:

- Schmitt trigger is opened
- Activate output buffer
- Weak pull-up and pull-down resistors are disabled
- Push-pull mode:

- Double MOS transistor works by turns and the output data register can control the high and low level of I/O output
- Read the finally written value through the output data register GPIOx\_ODATA
- Open-drain mode:
  - Only N-MOS works, and the output data register can control I/O output high resistance state or low level
  - Read the actual I/O state through the input data register GPIOx\_IDATA

Figure 15 I/O Structure in Output Mode



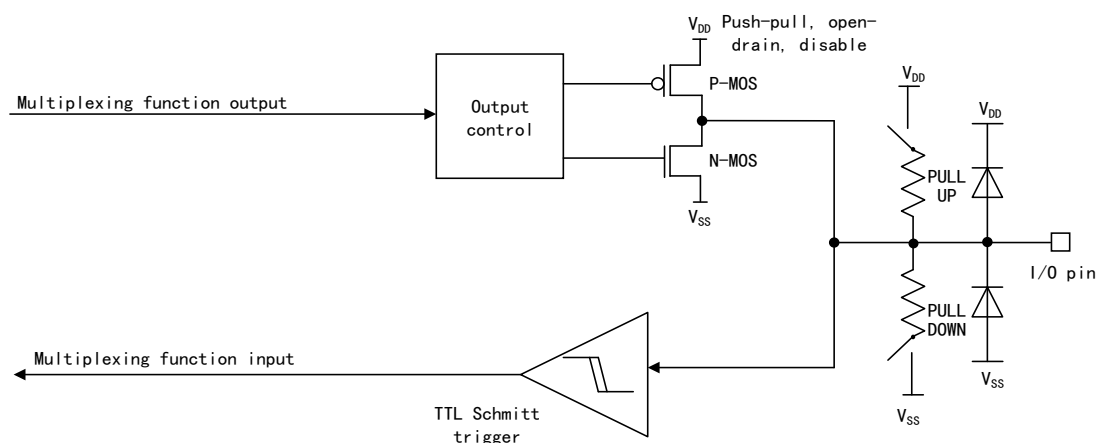
#### 12.4.4 Multiplexing mode

In multiplexing mode, it can be set as push-pull multiplexing and open-drain multiplexing.

In push-pull/open-drain multiplexed mode:

- Open the output buffer
- Output buffer is driven by peripheral
- Activate schmitt trigger input
- Weak pull-up and pull-down resistors are disabled
- The data on the I/O pin is sampled in each AHB1 clock cycle and stored in the port input state register
- In open-drain mode, the actual state of I/O can be read through input data register GPIOx\_IDATA
- In push-pull mode, the last written value is read through output data register GPIOx\_ODATA

Figure 16 I/O Structure in Multiplexing Mode



#### 12.4.5 External interrupt/wake-up line

All GPIO ports have external interrupt function. If you need to use external interrupt line, the port must be configured as input mode.

#### 12.4.6 Bit set and bit clear

Software does not need to disable interrupt when programming some bits of GPIOx\_IDATA. By setting the bit to be changed in GPIOx\_BSC and BSC registers to 1, the function of changing one or more bits in AHB1 write operation can be achieved.

#### 12.4.7 GPIO locking function

Locking function can be used in power driver module. The locking mechanism of GPIO can protect the configuration of I/O port. I/O configuration can be locked by configuring the lock register (GPIOx\_LOCK). When a port bit executes the locking program, the configuration of port bit cannot be modified before the next reset.

#### 12.4.8 OSC32\_IN/OSC32\_OUT pin

Only when LSECLK oscillator is turned off, can OSC32\_IN and OSC32\_OUT pins be used as general-purpose PC14 I/O and PC15 I/O. It is controlled by RCC\_BDCTRL[LSEEN] bit. The priority of LSECLK is higher than GPIO function.

#### 12.4.9 OSC\_IN/OSC\_OUT pin

Only when HSECLK oscillator is turned off, can OSC\_IN and OSC\_OUT pins be used as general-purpose PH0 I/O and PH1 I/O. It is controlled by RCC\_BDCTRL[HSEEN] bit. The priority of HSECLK is higher than GPIO function.



## 12.5 Register address mapping

Table 58 GPIO Register Address Mapping

| Register name | Description                                    | Offset address |
|---------------|------------------------------------------------|----------------|
| GPIOx_MODE    | Port mode register                             | 0x00           |
| GPIOx_OMODE   | Port output mode register                      | 0x04           |
| GPIOx_OSSEL   | Port output speed register                     | 0x08           |
| GPIOx_PUPD    | Port pull-up/pull-down register                | 0x0C           |
| GPIOx_IDATA   | Port bit input data register                   | 0x10           |
| GPIOx_ODATA   | Port bit output clear register                 | 0x14           |
| GPIOx_BSC     | Port set/reset register                        | 0x18           |
| GPIOx_LOCK    | Port lock register                             | 0x1C           |
| GPIOx_ALFL    | Port multiplexing function low 8-bit register  | 0x20           |
| GPIOx_ALFH    | Port multiplexing function high 8-bit register | 0x24           |

## 12.6 Register functional description

These peripheral registers must be operated by word (32 bits).

It should be noted that since the value of x in Plx is 0...11, the bit of the corresponding register depends on specific situation.

### 12.6.1 Port mode register (GPIOx\_MODE) (x=A...H)

Offset address: 0x00

Reset value: 0xA800 0000 (Port A)

0x0000 0280 (Port B)

0x0000 000 (other ports)

| Field   | Name       | R/W | Description                                                                                                                                                  |
|---------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2y+1:2y | MODEy[1:0] | R/W | Port x Pin y Mode Configure (y=0...15)<br>00: Input mode (state after reset)<br>01: General output mode<br>10: Multiplexing function mode<br>11: Analog mode |

### 12.6.2 Port output mode register (GPIOx\_OMODE) (x=A...H)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------|
| 15:0  | OMODEy   | R/W | Port x Pin y Output Mode Configure (y=0...15)<br>0: Push-pull output (reset state)<br>1: Open-drain output |
| 31:16 | Reserved |     |                                                                                                            |

### 12.6.3 Port output speed register (GPIOx\_OSSEL) (x=A...H)

Offset address: 0x08

Reset value: 0x0C00 0000 (Port A)

0x0000 00C0 (Port B)

0x0000 000 (other ports)

| Field   | Name        | R/W | Description                                                                                                                                                                              |
|---------|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2y+1:2y | OSSELy[1:0] | R/W | Port x Pin y Output Speed Select (y=0...15)<br>00: Low speed<br>01: Medium speed<br>10: High speed<br>11: Very high speed<br>The speed of configuration I/O port is written by software. |

### 12.6.4 GPIO port pull-up/pull-down register (GPIOx\_PUPD) (x=A...H)

Offset address: 0x0C

Reset value: 0x6400 0000 (Port A)

0x0000 0100 (Port B)

0x0000 000 (other ports)

| Field   | Name       | R/W | Description                                                                                                                                                                                                                   |
|---------|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2y+1:2y | PUPDy[1:0] | R/W | Port x Pin y Pull-up/Pull-down Configure (y=0...15)<br>These bits are written by software to configure pull-up/pull-down of the port bit<br>00: Pull-up/Pull-down is disabled<br>01: Pull up<br>10: Pull down<br>11: Reserved |

### 12.6.5 GPIO port input data register (GPIOx\_IDATA) (x=A...H)

Offset address: 0x10

Reset value: 0x0000 XXXX

| Field | Name     | R/W | Description                                                                                                                |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------|
| 15:0  | IDATAy   | R   | Port x Pin y Input Data (y=0...15)<br>These bits can only be read to store the input values of the corresponding I/O ports |
| 31:16 | Reserved |     |                                                                                                                            |

### 12.6.6 GPIO port output data register (GPIOx\_ODATA) (x=A...H)

Offset address: 0x14

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                      |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | ODATAy   | R/W | Port x Pin y Output Data (y=0...15)<br>Read and write operation can be performed by software<br>For bit set/clear, the ODATAy bit can be set separately by writing to GPIOx_BSC. |
| 31:16 | Reserved |     |                                                                                                                                                                                  |

### 12.6.7 GPIO port set/reset register (GPIOx\_BSC) (x=A...H)

Offset address: 0x18

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | BSy  | W   | Port x Pin y Set bit (y=0...15)<br>These bits can only perform write operation, and the value of 0x0000 is returned when reading these bits.<br>These bits are used to affect the corresponding ODATAy bits.<br>0: No effect<br>1: Set the corresponding ODATAy bit                                                                                |
| 31:16 | BCy  | W   | Port x Pin y Reset Bit (y=0...15)<br>These bits can only perform write operation, and the value of 0x0000 is returned when reading these bits.<br>These bits are used to affect the corresponding ODATAy bits.<br>0: No effect<br>1: Corresponding ODATAy bit is cleared<br>If Bsy bit and Bcy bit are set at the same time, Bsy has the priority. |

### 12.6.8 GPIO port lock register (GPIOx\_LOCK) (x=A..G)

Offset address: 0x1C

Reset value: 0x0000 0000

This register protects the configuration of GPIO from being modified by mistake during the running of the program. If the GPIO configuration is modified again, it can be modified only after the system is reset. When configuring GPIO locking function, it is necessary to execute the specified sequence to the register to start the GPIO locking function.

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | LOCKy   | R/W | Port x Pin y Lock Configure (y=0...15)<br>0: The configuration of Port x Pin y is not locked<br>1: The configuration of Port x Pin y is locked<br>These bits can be read and written, but can only be written when LOCKKEY=0.                                                                                                                                                                                                                           |
| 16    | LOCKKEY | R/W | Lock Key<br>This bit determines whether the port configuration lock key bit is activated.<br>0: Not activated<br>1: Activated; GPIOx_LOCK register is locked until the next MUC reset is generated.<br>Lock key write sequence:<br>Write LOCK[16]=1+LOCK[15:0]<br>Write LOCK[16]=0+LOCK[15:0]<br>Write LOCK[16]=1+LOCK[15:0]<br>Read LOCK<br>Read LOCK[16]=1 (this read operation can be selected to confirm whether to activate the lock key)<br>Note: |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | <p>The value of LOCKy cannot be changed during the write sequence of the operation lock key.</p> <p>Any error in the write sequence of operation lock key will abort the lock.</p> <p>After the first lock sequence on any bit of the port, any read access on the LOCKKEY bit will return "1" until the next MCU is reset or the peripheral is reset.</p> |
| 31:17 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                            |

### 12.6.9 GPIO multiplexing function low 8-bit register (GPIOx\_ALFL) (x=A...H)

Offset address: 0x20

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | ALFSELY | R/W | <p>Port x Pin y Alternate Function Select (y=0....7)</p> <p>These bits can be read by software to configure the multiplexing function of the port.</p> <p>ALFSELY selection:</p> <p>0000: AF0</p> <p>0001: AF1</p> <p>0010: AF2</p> <p>0011: AF3</p> <p>0100: AF4</p> <p>0101: AF5</p> <p>0110: AF6</p> <p>0111: AF7</p> <p>1000: AF8</p> <p>1001: AF9</p> <p>1010: AF10</p> <p>1011: AF11</p> <p>1100: AF12</p> <p>1101: AF13</p> <p>1111: AF14</p> <p>1110: AF15</p> |

### 12.6.10 GPIO multiplexing function high 8-bit register (GPIOx\_ALFH) (x=A...H)

Offset address: 0x24

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                                                                                                                                                          |
|-------|---------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | ALFSELY | R/W | <p>Port x Pin y Alternate Function Select (y=8....15)</p> <p>These bits can be read by software to configure the multiplexing function of the port.</p> <p>ALFSELY selection:</p> <p>0000: AF0</p> <p>0001: AF1</p> <p>0010: AF2</p> |

| Field | Name | R/W | Description                                                                                                                                                                 |
|-------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |      |     | 0011: AF3<br>0100: AF4<br>0101: AF5<br>0110: AF6<br>0111: AF7<br>1000: AF8<br>1001: AF9<br>1010: AF10<br>1011: AF11<br>1100: AF12<br>1101: AF13<br>1111: AF14<br>1110: AF15 |

## 13 Timer Overview

### 13.1 Full name and abbreviation description of terms

Table 59 Full name and abbreviation description of terms

| Full name in English | English abbreviation |
|----------------------|----------------------|
| Timer                | TMR                  |
| Update               | U                    |
| Request              | R                    |
| Event                | EV                   |
| Capture              | C                    |
| Compare              | C                    |
| Length               | LEN                  |

### 13.2 Timer category and main difference

In this series of products, there are three types of timers: advanced timer, general-purpose timer and basic timer (watchdog timer is described in other chapters).

The advanced timer includes the functions of general-purpose timer and basic timer. The advanced timer has four capture/compare channels, supports timing function, input capture and output compare function, braking and complementary output function. It is a 16-bit timer that can count up/down.

The function of general-purpose timer is simpler than that of advanced timer. The main differences are the total number of channels, the number of complementary output channel groups and the braking function.

The basic timer is a timer that can only provide timing function and has no external interface.

The main differences of timers included in the products are shown in the table below:

Table 60 Main Differences among Timers Included in the Products

| Item          | Specific content/Category | Advanced timer | General-purpose timer | General-purpose timer |         | Basic timer |
|---------------|---------------------------|----------------|-----------------------|-----------------------|---------|-------------|
| Name          | —                         | TMR1/8         | TMR2/3/4/5            | TMR10/11/13/14        | TMR9/12 | TMR6/7      |
| Timebase unit | Counter                   | 16 bits        | 32 bits               | 16 bits               | 16 bits | 16 bits     |
|               | Prescaler                 | 16 bits        | 16 bits               | 16 bits               | 16 bits | 16 bits     |

| Item     | Specific content/Category    | Advanced timer                 | General-purpose timer          | General-purpose timer |      | Basic timer |
|----------|------------------------------|--------------------------------|--------------------------------|-----------------------|------|-------------|
|          | Count mode                   | Up<br>Down<br>Center alignment | Up<br>Down<br>Center alignment | Up                    | Up   | Up          |
| Channel  | Input channel                | 4                              | 4                              | 1                     | 2    | 0           |
|          | Capture/Compare channel      | 4                              | 4                              | 1                     | 2    | 0           |
|          | Output channel               | 7                              | 4                              | 1                     | 2    | 0           |
|          | Complementary output channel | 3                              | 0                              | 0                     | 0    | 0           |
| Function | Generate DMA request         | Yes                            | Yes                            | No                    | No   | Yes         |
|          | PWM mode                     | Yes                            | Yes                            | Yes                   | Yes  | None        |
|          | Single-pulse mode            | Yes                            | Yes                            | Yes                   | Yes  | None        |
|          | Forced output mode           | Yes                            | Yes                            | Yes                   | Yes  | None        |
|          | Deadband insertion           | Yes                            | None                           | None                  | None | None        |

## Timer term

Table 61 Definitions and Terms of Pins

| Name                                | Description                               |
|-------------------------------------|-------------------------------------------|
| TMRx_ETR                            | External trigger signal of Timer x        |
| TMRx_CH1、TMRx_CH2、TMRx_CH3、TMRx_CH4 | Channel 1/2/3/4 of Timer x                |
| TMRx_ChN                            | Complementary output channel y of Timer x |
| TMRx_BKIN                           | Braking signal of Timer x                 |

Table 62 Definitions and Terms of Internal Signals

| Name            | Description                                       |
|-----------------|---------------------------------------------------|
| ETR             | TMRx_ETR external trigger signal                  |
| ETRF            | External trigger filter                           |
| ETRP            | External trigger prescaler                        |
| -               |                                                   |
| ITR, ITR0, ITR1 | Internal trigger                                  |
| TRGI            | Clock/Trigger/Slave mode controller trigger input |
| TIF_ED          | Timer input filter edge detection                 |

| Name           | Description                     |
|----------------|---------------------------------|
| -              |                                 |
| CK_PSC         | Prescaler clock                 |
| CK_CNT         | Counter clock                   |
| PSC            | Prescaler                       |
| CNT            | Counter                         |
| AUTORLD        | Autoload register               |
| -              |                                 |
| TIx, TI1       | Timer input                     |
| TIxF, TI1F,    | Timer input filter              |
| TI1_ED         | Timer input edge detection      |
| TIxFPx, TI1FP1 | Timer input filter polarity     |
| ICx, IC1       | Input capture                   |
| ICxPS, IC1PS   | Input capture prescaler         |
| TRC            | Trigger capture                 |
| BRK            | Braking signal                  |
| -              |                                 |
| OCx, OC1       | Timer output coparison channel  |
| OCxREF, OC1REF | Output compare reference signal |
| -              |                                 |
| TGI            | Trigger interrupt               |
| BI             | Braking interrupt               |
| CCxI, CC1I     | Capture/Compare interrupt       |
| UEV            | Update event                    |
| UIFLG          | Update interrupt flag           |



## 14 Advanced Timers (TMR1/8)

### 14.1 Introduction

The advanced timer takes the time base unit as the core, and has the functions of input capture, output compare and braking input, including a 16-bit automatic loading counter. Compared with other timers, the advanced timer supports complementary output, repeat count and programmable dead-time insertion function, and is more suitable for motor control.

### 14.2 Main characteristics

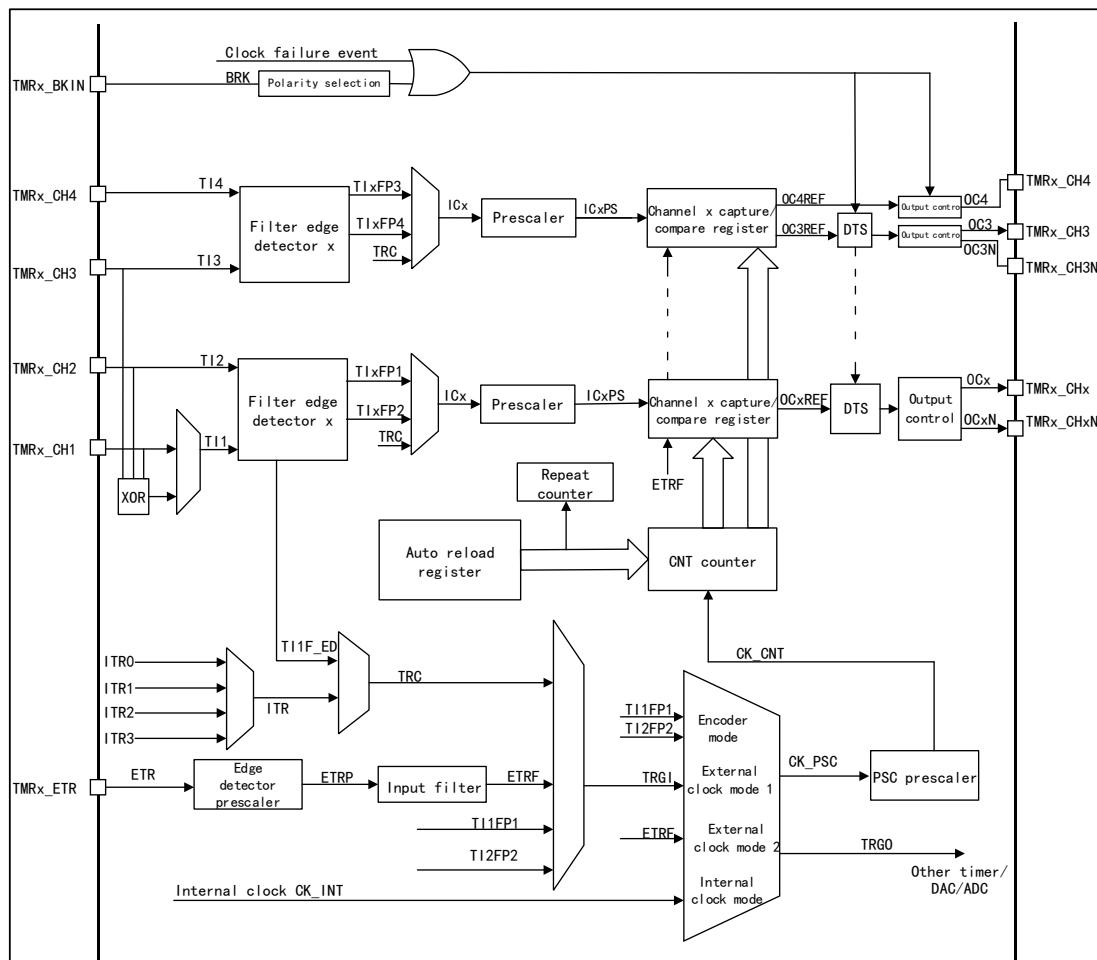
- (1) Timebase unit
  - Counter: 16-bit counter, count-up, count-down and center-aligned count
  - Prescaler: 16-bit programmable prescaler
  - Repeat counter: 16-bit repeat counter
  - Auto reloading function
- (2) Clock source selection
  - Internal clock
  - External input
  - External trigger
  - Internal trigger
- (3) Input capture function
  - Counting function
  - PWM input mode (measurement of pulse width, frequency and duty cycle)
  - Encoder interface mode
- (4) Output compare function
  - PWM output mode
  - Forced output mode
  - Single-pulse mode
  - Complementary output and dead-time insertion
- (5) Timing function
- (6) Braking function
- (7) Master/Slave mode controller of timer
  - Timers can be synchronized and cascaded
  - Support multiple slave modes and synchronization signals
- (8) Interrupt output and DMA request event
  - Update event (counter overrun/underrun, counter initialization)

- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Braking signal input event

- (9) Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes

## 14.3 Structure block diagram

Figure 17 Advanced Timer Structure Block Diagram



## 14.4 Functional description

### 14.4.1 Clock source selection

The advanced timer has four clock sources.

#### Internal clock

It is TMRx\_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK\_PSC of the prescaler is driven by the internal clock CK\_INT.

### External clock mode 1

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F\_ED signal, namely double-edge signal of TIF\_ED. Specially the PWM input can only be input by TI1/2.

### External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to slave mode controller through trigger input selector to control the work of counter.

### Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

## 14.4.2 Timebase unit

The time base unit in the advanced timer contains four registers

- 16-bit counter register (CNT)
- 16-bit auto reload register (AUTORLD)
- 16-bit prescaler register (PSC)
- 8-bit repetition count register (REPCNT)

Repetition register is unique to advanced timer.

### Counter CNT

There are three counting modes for the counter in the advanced timer

- Count-up mode
- Count-down mode
- Center-aligned mode

### Count-up mode

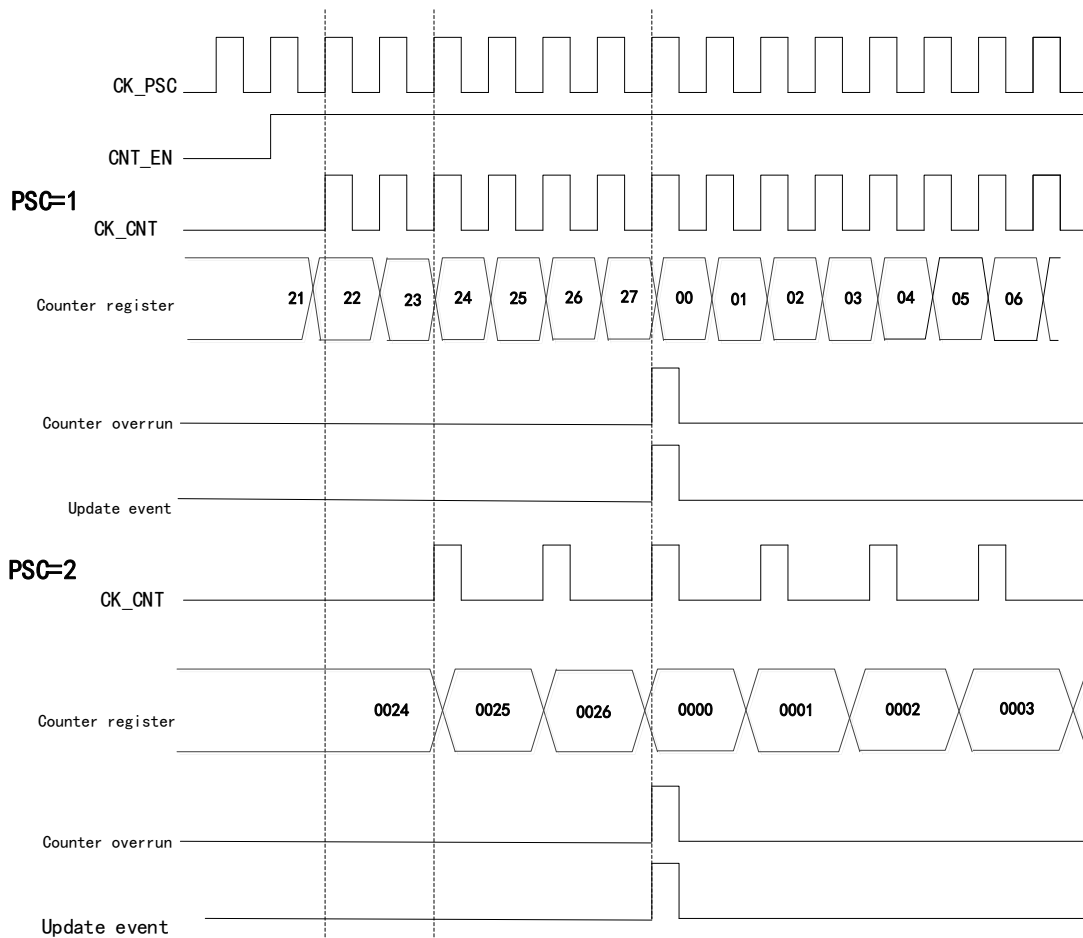
Set to the count-up mode by CNTDIR bit of configuration control register (TMRx\_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx\_CNT) is equal to the value of the auto reload (TMRx\_AUTORLD), the counter will start to count again from 0. A count-up overrun event will be generated, and the value of the auto reload

(TMRx\_AUTORLD) is written in advance. If a repeat counter is used, an update event will be generated when the number of count-up repetitions reaches the number in the repeat counter register plus one time (TMRx\_REPCNT+1). Otherwise, an update event will be generated every time the counter overruns. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMRx\_CTRL1.

The figure below is timing diagram when division factor is 1 or 2 in the count-up mode.

Figure 18 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



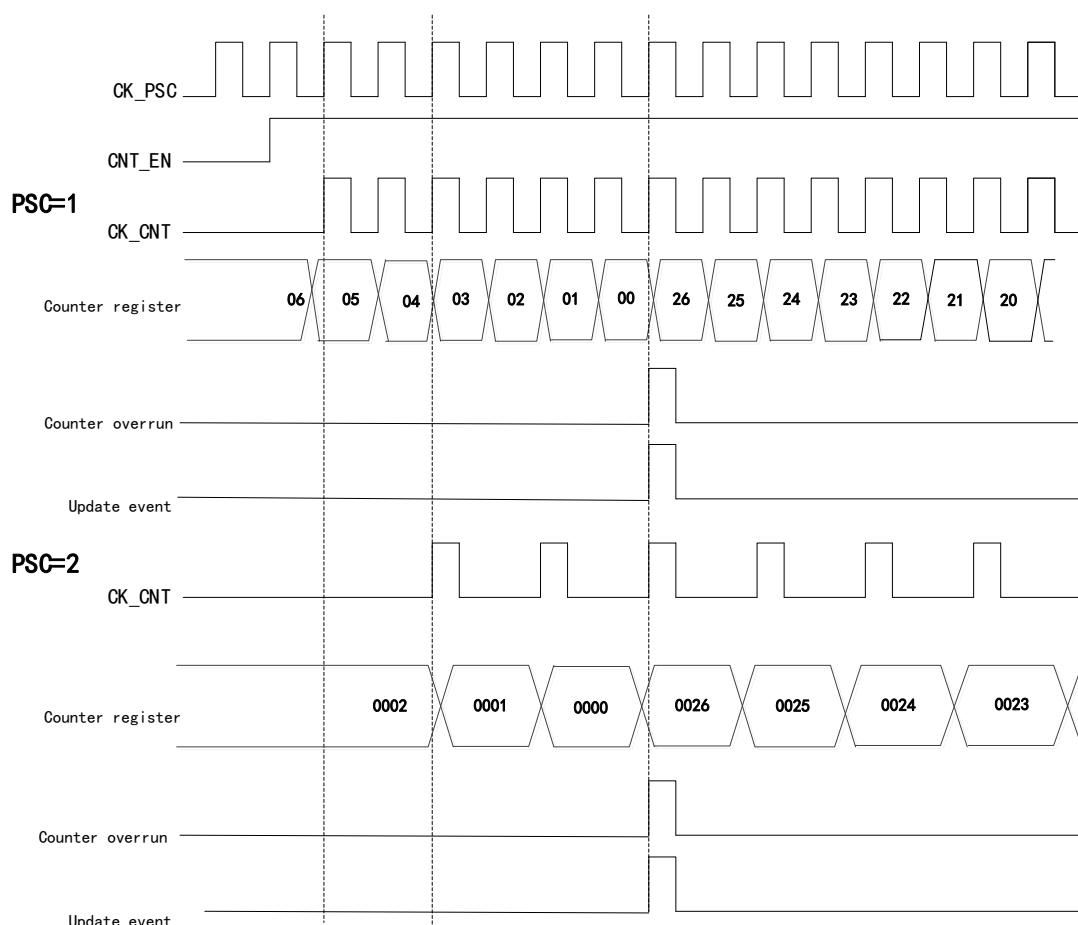
### Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMRx\_CTRL1).

When the counter is in count-down mode, the counter will start to count down from the value of the auto reload (TMRx\_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMRx\_AUTORLD). Meanwhile, a count-down overrun event will be generated, and the value of the auto reload

(TMRx\_AUTORLD) is written in advance. If a repeat counter is used, an update event will be generated when the number of count-down repetitions reaches the number in the repeat counter register plus one time (TMRx\_REPCNT+1). Otherwise, an update event will be generated every time the counter underruns. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the UD bit of the TMRx\_CTRL1 register.

Figure 19 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

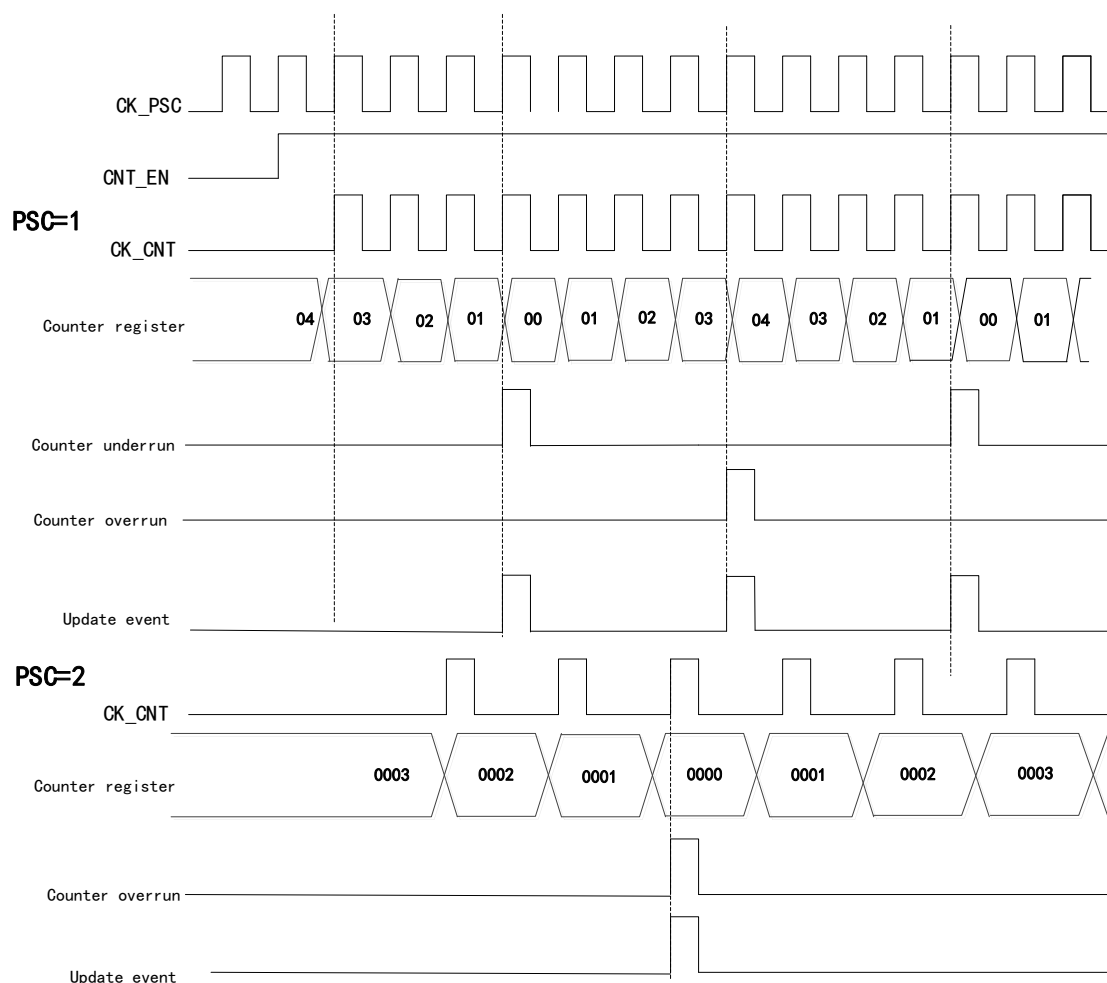


### Center-aligned mode

Set to the center-aligned mode by CAMSEL bit of configuration control register (TMRx\_CTRL1).

When the counter is in center-aligned mode, the counter counts up from 0 to the value of auto reload (TMRx\_AUTORLD), then counts down to 0 from the value of the auto reload (TMRx\_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 20 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



### Repeat counter REPCNT

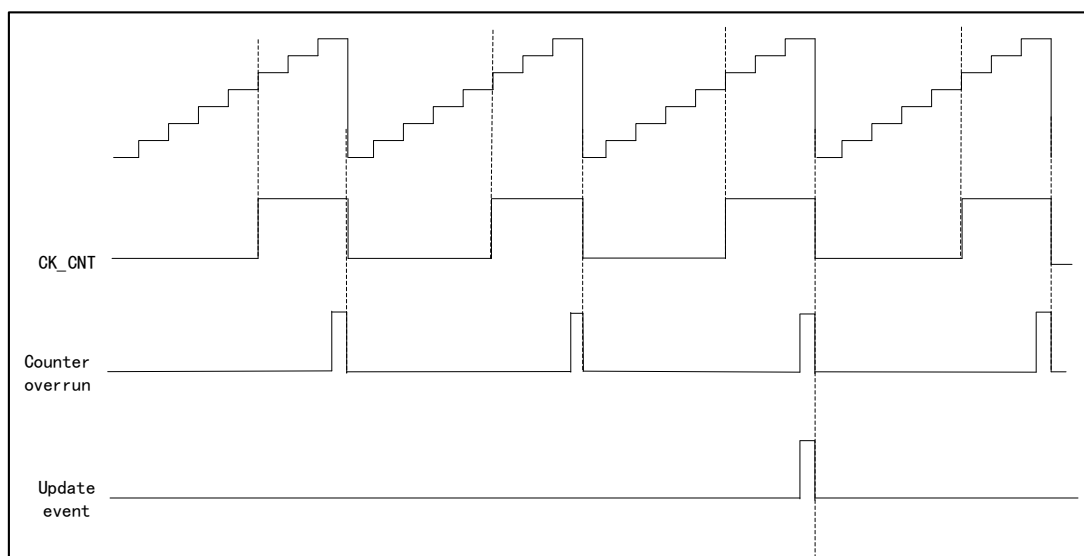
There is no repeat counter REPCNT in the basic/general-purpose timer, which means that when the overrun event or underrun event occurs in the basic/general-purpose timer, an update event will be generated directly; while in the advanced timer, because of the existence of the repeat counter, when an overrun/underrun event occurs to the advanced timer, the update event will be generated only when the value of the repeat counter is 0.

For example, if the advanced timer needs to generate an update event when an overrun/underrun event occurs, the value of the repeat counter should be set to 0.

If the repeat counter function is used in the count-up mode, every time the counter counts up to AUTORLD, an overrun event will occur. At this time, the value of the repeat counter will be decreased by 1, and an update event will be generated until the value of the repeat counter is 0.

That is, when N+1 (N is the value of repeat counter) overrun/underrun events occur, an update event will be generated.

Figure 21 Timing Diagram when Setting REPCNT=2 in Count-up Mode



### Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx\_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

### 14.4.3 Input capture

#### Input capture channel

The advanced timer has four independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

#### Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width). For example, if the selected edge appears on the input pin, the TMRx\_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx\_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

#### 14.4.4 Output compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM mode 1 and PWM mode 2, which are configured by OCxMOD bit in TMRx\_CCMx register and can control the waveform of output signal in output compare mode.

##### Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx\_CCMx register and the CCxPOL bit in the output polarity TMRx\_CCEN register.

When CCxIFLG=1 in TMRx\_STS register, if CCxIEN=1 in TMRx\_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx\_CTRL2 register, DMA request will be generated.

#### 14.4.5 PWM output mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and center alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7



Figure 22 PWM1 Count-up Mode Timing Diagram

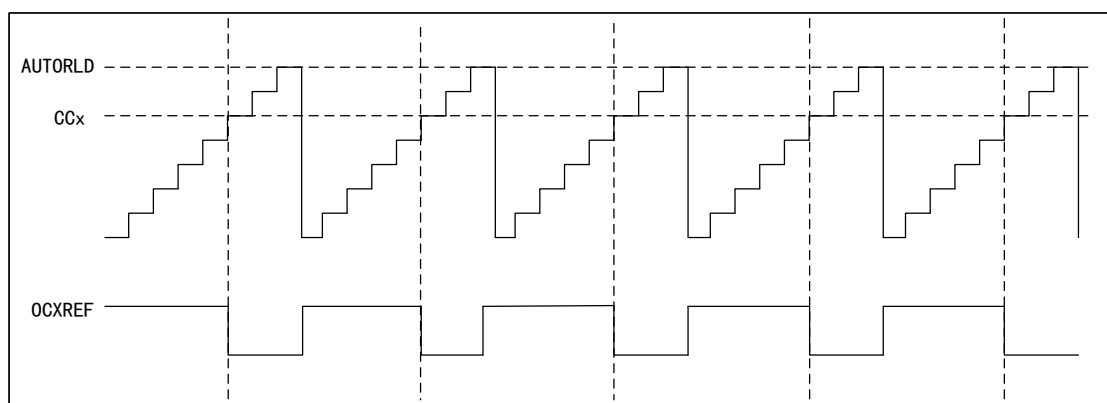


Figure 23 PWM1 Count-down Mode Timing Diagram

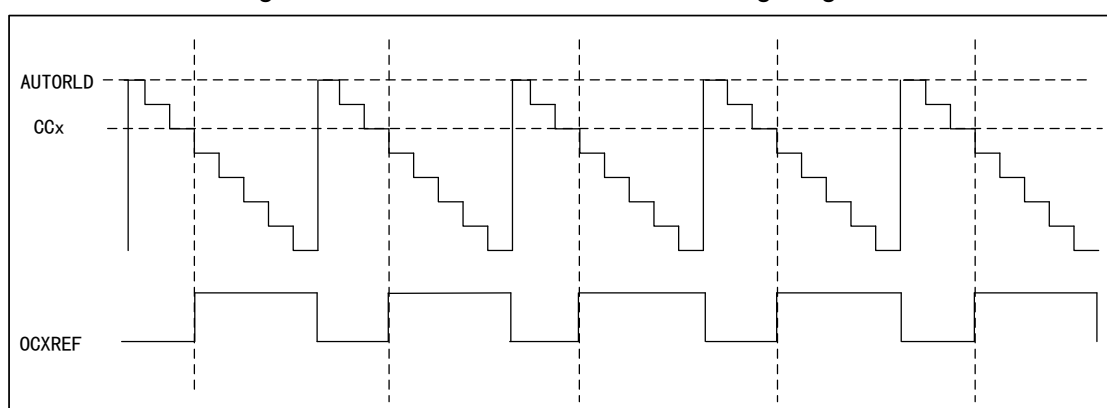
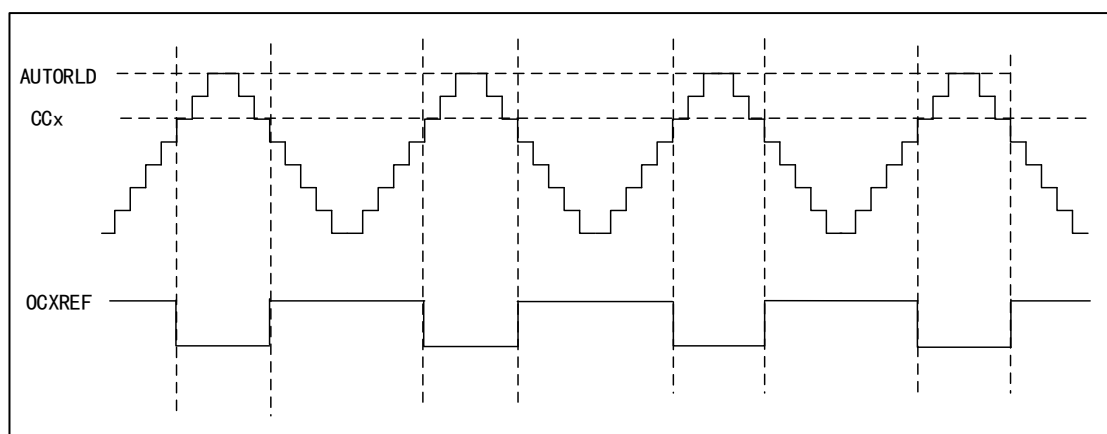


Figure 24 PWM1 Center-aligned Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 25 PWM2 Count-up Mode Timing Diagram

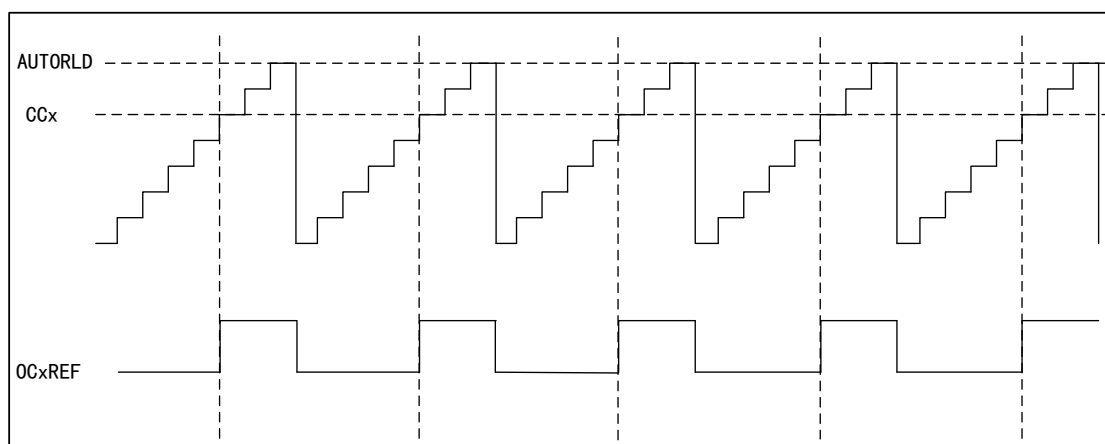


Figure 26 PWM2 Count-down Mode Timing Diagram

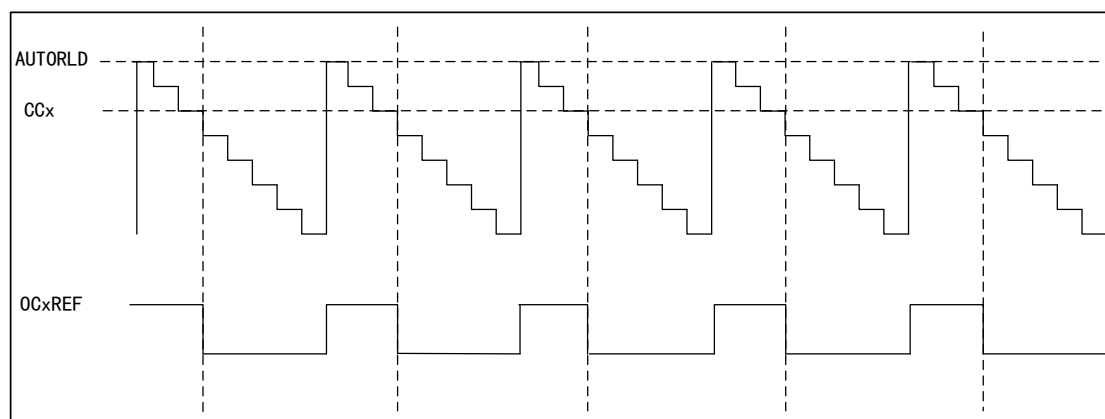
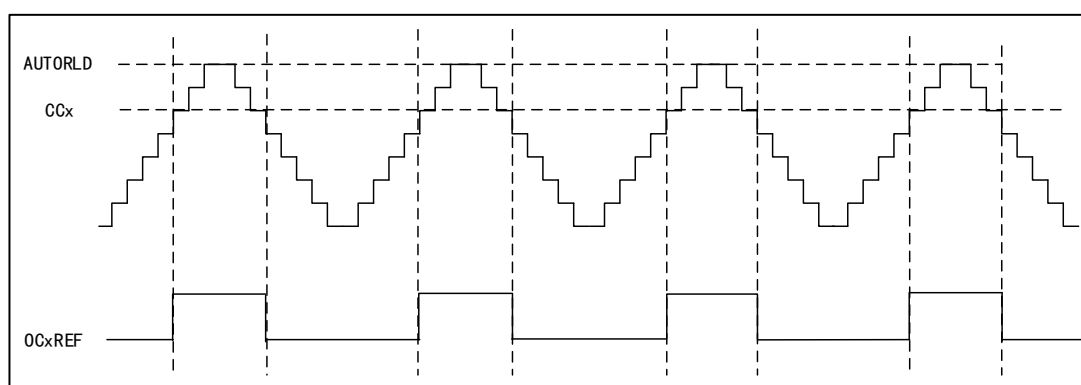


Figure 27 PWM2 Center-aligned Mode Timing Diagram



#### 14.4.6 PWM input mode

PWM input mode is a particular case of input capture.

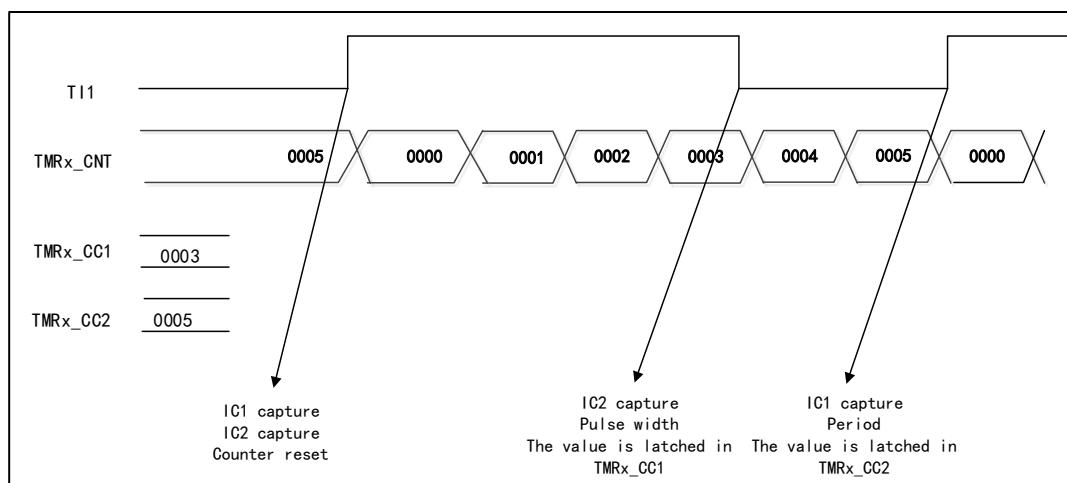
In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMRx\_CH1 and TMRx\_CH2, which need to occupy the capture registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMRx\_CH1, and the

signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMRx\_SMCTRL register)

Figure 28 PWM Input Mode Timing Diagram



#### 14.4.7 Single-pulse mode

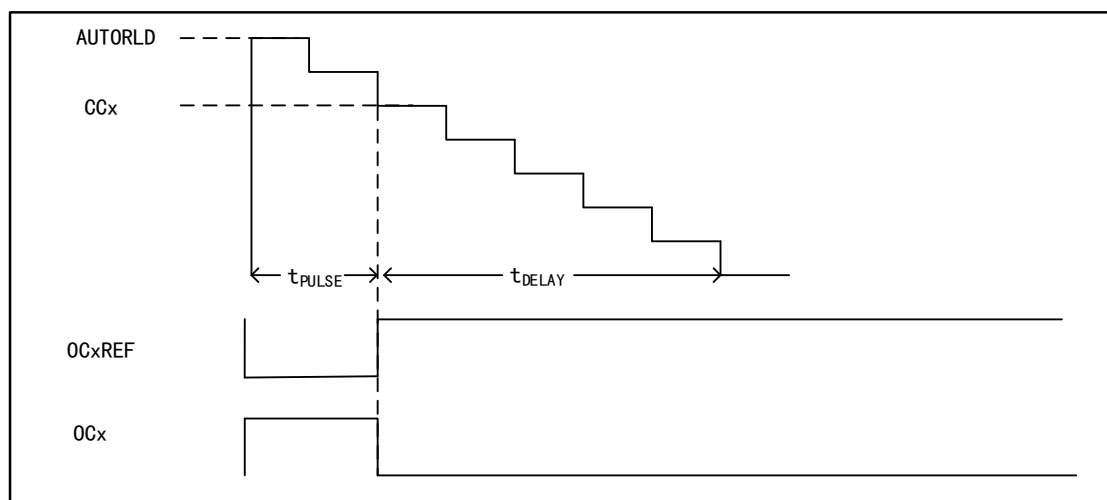
The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SPMEN bit of TMRx\_CTRL1 register, and select the single-pulse mode.

After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx\_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 29 Single-pulse Mode Timing Diagram



#### 14.4.8 Impact of the register on output waveform

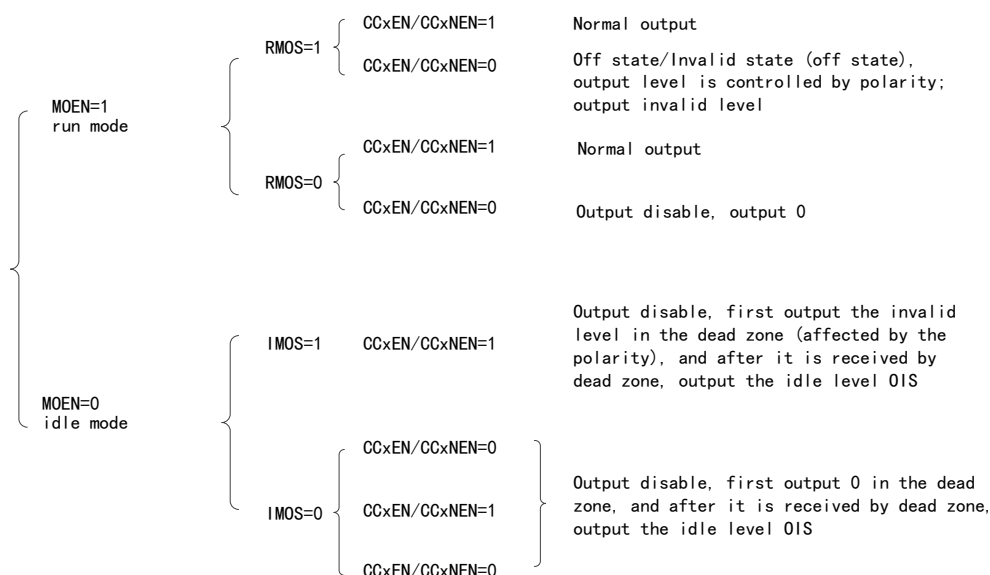
The following registers will affect the level of the timer output waveform. For details, refer to "Register Functional Description".

- (1) CCxEN and CCxNEN bits in TMRx\_CCEN register
  - CCxNEN=0 and CCxEN=0: The output is turned off (output disabled, invalid state)
  - CCxNEN=1 and CCxEN=1: The output is turned on (output enabled, normal output)
- (2) MOEN bit in TMRx\_BDT register
  - MOEN=0: Idle mode
  - MOEN=1: Run mode
- (3) OCxOIS and OCxNOIS bits in TMRx\_CTRL2 register
  - OCxOIS=0 and OCxNOIS=0: When idle (MOEN=0), the output level after the dead-time is 0
  - OCxOIS=1 and OCxNOIS=1: When idle (MOEN=0), the output level after the dead-time is 1
- (4) RMOS bit in TMRx\_BDT register
  - Application environment of RMOS: In corresponding complementary channel and timer are in run mode (MOEN=1), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)
- (5) IMOS bit in TMRx\_BDT register
  - Application environment of IMOS: In corresponding complementary channel and timer are in idle mode (MOEN=0), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

- (6) CCxPOL and CCxNPOL bits of TMRx\_CCEN register
- CCxPOL=0 and CCxNPOL=0: Output polarity, high level is valid  
CCxPOL=1 and CCxNPOL=1: Output polarity, the low level is valid

The following figure lists the register structure relationships that affect the output waveform

Figure 30 Register Structural Relationship Affecting Output Waveform



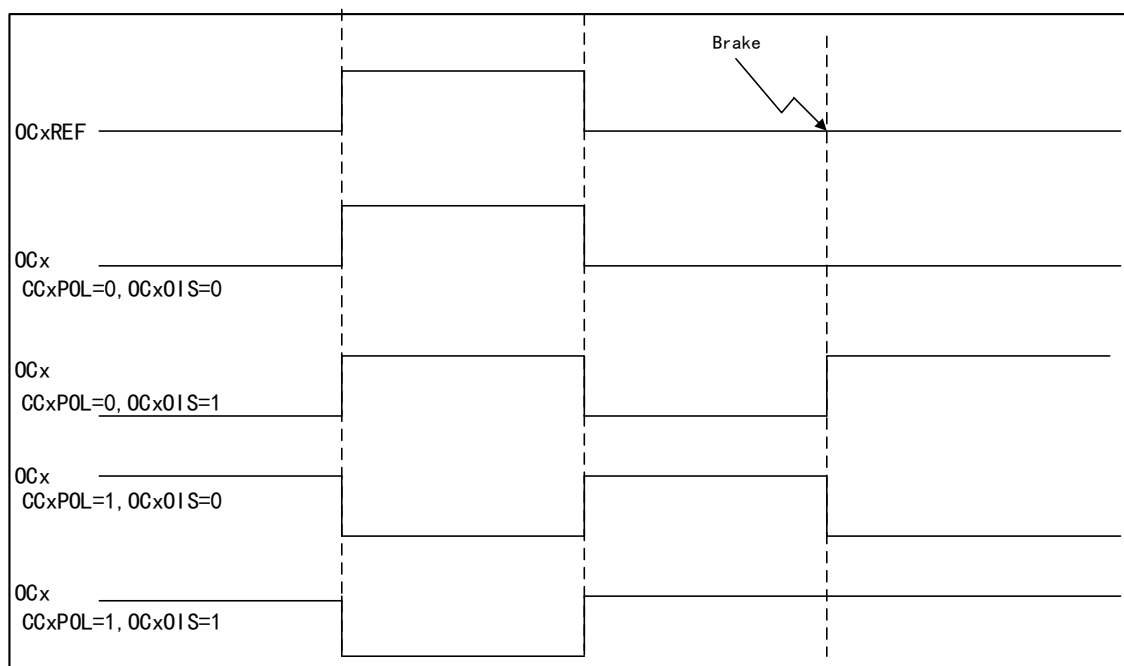
#### 14.4.9 Braking function

The signal source of braking is clock fault event and external input interface.

Besides, the BRKEN bit in TMRx\_BDT register can enable the braking function, and the BRKPOL bit can configure the polarity of braking input signal.

When a braking event occurs, the output pulse signal level can be modified according to the state of the relevant control bit.

Figure 31 Braking Event Timing Diagram

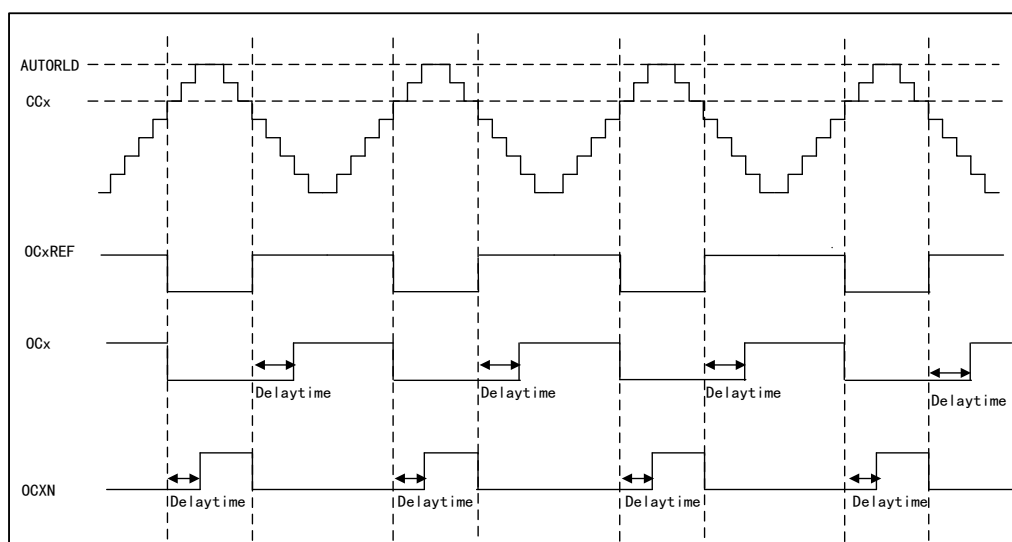


#### 14.4.10 Complementary output and dead-time insertion

Complementary output is particular output of advanced timer, and the advanced timer has three groups of complementary output channels. The insertion deadband is used to generate complementary output signals to ensure that the two-way complementary signals of channels will not be valid at the same time. The deadband is set according to the output device connected to the timer and its characteristics.

The duration of the deadband can be controlled by configuring DTS bit of TMRx\_BDT register.

Figure 32 Complementary Output of Insertion with Deadband



#### 14.4.11 Forced output mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMRx\_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMRx\_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

#### 14.4.12 Encoder interface mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection method of encoder interface is as follows:

- By setting SMFSEL bit of TMRx\_SMCTRL register, set the counter to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- Select the polarity of TI1 and TI2 by setting the CC1POL and CC2POL bits of TMRx\_CCEN register.
- Select to filter or not by setting the IC1F and IC2F bits of TMRx\_CCM1 register.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2:

- The counter will count up/down according to the jumping sequence of the input signal.
- Set CNTDIR of control register TMRx\_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end).

The change mechanism of counter count direction is shown in the figure below.

Table 63 Relationship between Count Direction and Encoder

| Effective edge           |              | Count only in TI1 |            | Count only in TI2 |            | Count in both TI1 and TI2 |            |
|--------------------------|--------------|-------------------|------------|-------------------|------------|---------------------------|------------|
| Level of relative signal |              | High              | Low        | High              | Low        | High                      | Low        |
| TI1FP1                   | Rising edge  | Count down        | Count up   | —                 |            | Count down                | Count up   |
|                          | Falling edge | Count up          | Count down |                   |            | Count up                  | Count down |
| TI2FP2                   | Rising edge  | —                 |            | Count up          | Count down | Count up                  | Count down |
|                          | Falling edge |                   |            | Count down        | Count up   | Count down                | Count up   |

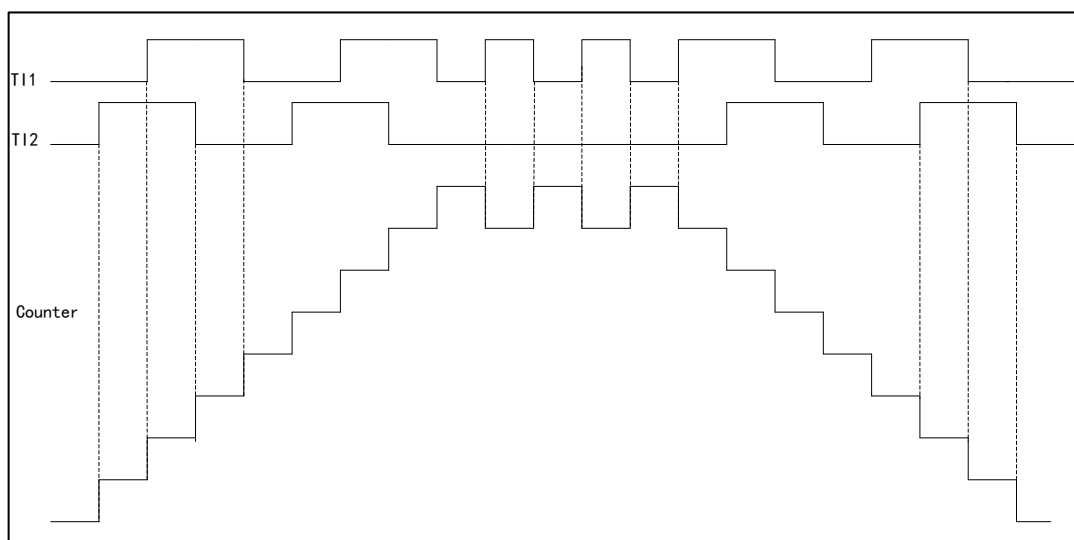
The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples:

- IC1FP1 is mapped to TI1
- IC2FP2 is mapped to TI2
- Neither IC1FP1 nor IC2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

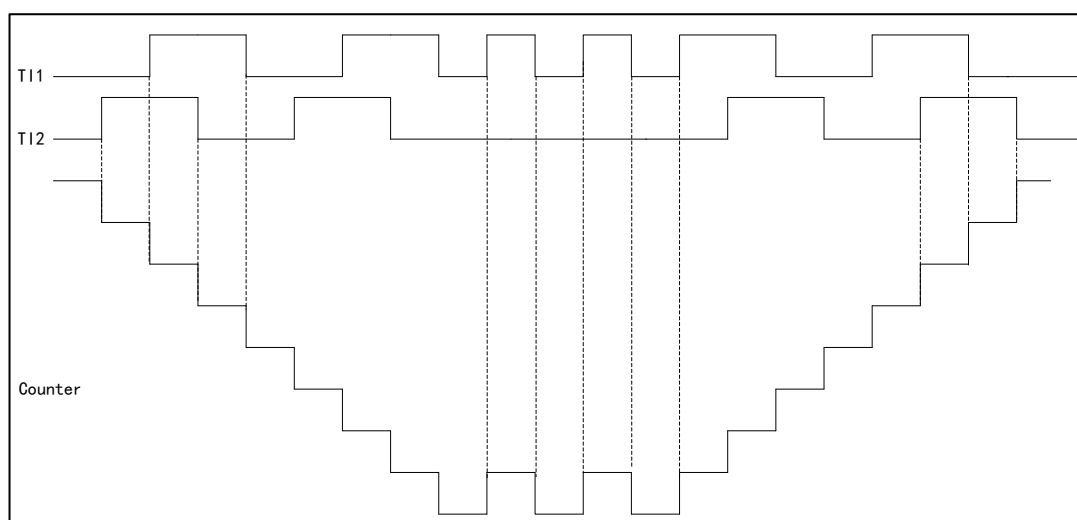


Figure 33 Counter Operation Example in Encoder Mode



For example, when T11 is at low level, and T12 is in rising edge state, the counter will count up.

Figure 34 Example of Encoder Interface Mode of IC1FP1 Reversed Phase



For example, when T11 is at low level, and the rising edge of T12 jumps, the counter will count down.

#### 14.4.13 Slave mode

TMRx timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMRx\_SMCTRL register can be set to select the mode.

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

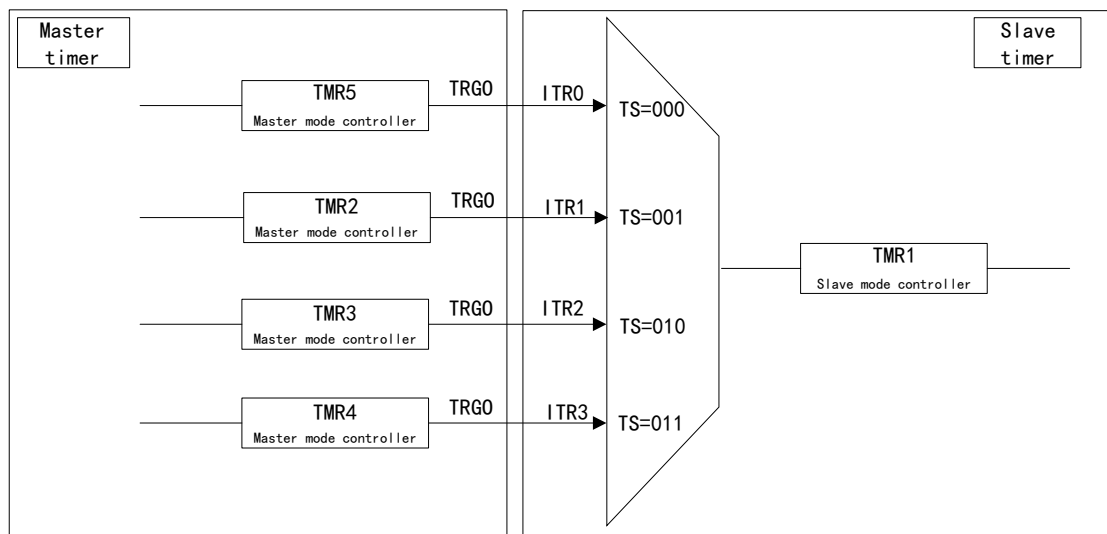
In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

#### 14.4.14 Timer interconnection

Each timer of TMRx can be connected with each other to realize synchronization or cascading between timers. It is required to configure one timer in master mode and the other timer in slave mode.

When the timer is in master mode, it can reset, start, stop and provide clock source for the counter of the slave mode timer.

Figure 35 Timer 1 Master/Slave Mode Example



When the timers are interconnected:

- A timer can be used as the prescaler of other register
- Another register can be started by the enable signal of a timer
- Another register can be started by the update event of a timer
- Another register can be selected by the enable of a timer
- Two timers can be synchronized by an external trigger

#### 14.4.15 Interrupt and DMA request

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)

- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Braking signal input event

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

#### 14.4.16 Debug mode

The TMR1/8 can be configured in debug mode and choose to stop or continue to work. It depends on the TMRx\_STS bit of DBGMCU\_APB2F register in DBGMCU module.

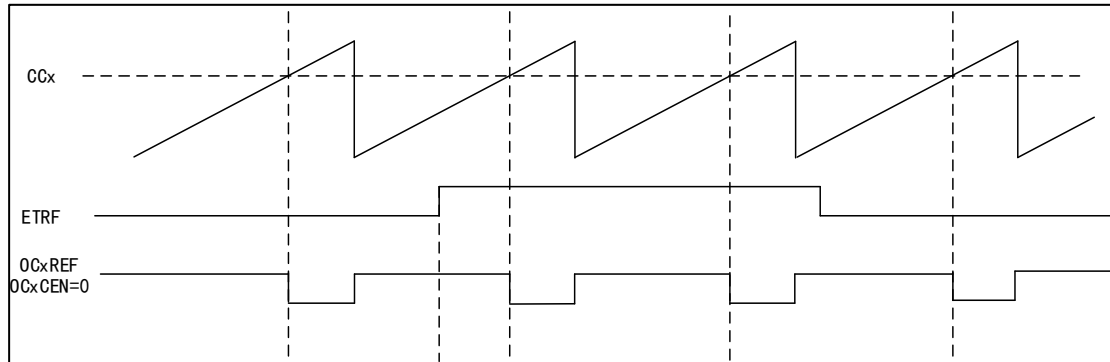
#### 14.4.17 Clear OCxREF signal when external events occur

This function is used for output compare and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCxCEN bit in capture/compare register TMRx\_CCMx is set to 1, and OCxREF signal will remain low until the next update event.

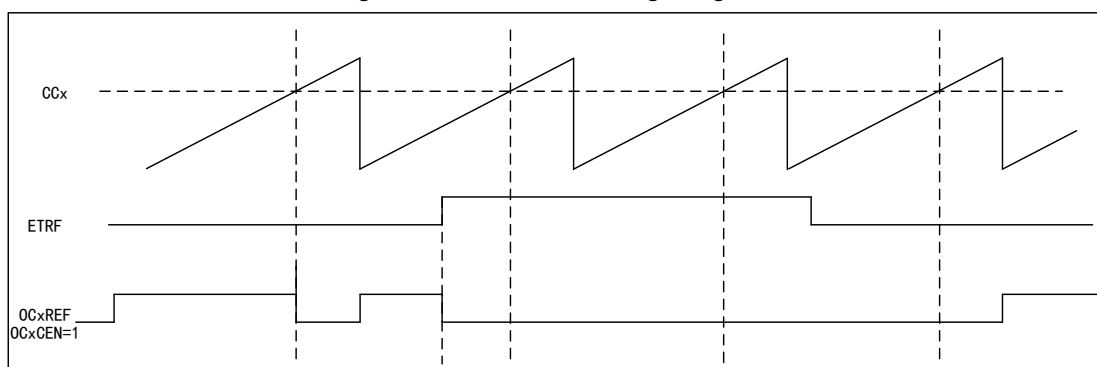
Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 36 OCxREF Timing Diagram



Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 37 OCxREF Timing Diagram



## 14.5 Register address mapping

In the following table, all registers of the advanced timer are mapped to a 16-bit addressable (address) space.

Table 64 Advanced Timer Register Address Mapping

| Register name | Description                             | Offset address |
|---------------|-----------------------------------------|----------------|
| TMRx_CTRL1    | Control register 1                      | 0x00           |
| TMRx_CTRL2    | Control register 2                      | 0x04           |
| TMRx_SMCTRL   | Slave mode control register             | 0x08           |
| TMRx_DIEN     | DMA/Interrupt enable register           | 0x0C           |
| TMRx_STS      | State register                          | 0x10           |
| TMRx_CEG      | Control event generation register       | 0x14           |
| TMRx_CCM1     | Capture/Compare mode register 1         | 0x18           |
| TMRx_CCM2     | Capture/Compare mode register 2         | 0x1C           |
| TMRx_CCEN     | Capture/Compare enable register         | 0x20           |
| TMRx_CNT      | Counter register                        | 0x24           |
| TMRx_PSC      | Prescaler register                      | 0x28           |
| TMRx_AUTORLD  | Auto reload register                    | 0x2C           |
| TMRx_REPCNT   | Repeat count register                   | 0x30           |
| TMRx_CC1      | Channel 1 capture/compare register      | 0x34           |
| TMRx_CC2      | Channel 2 capture/compare register      | 0x38           |
| TMRx_CC3      | Channel 3 capture/compare register      | 0x3C           |
| TMRx_CC4      | Channel 4 capture/compare register      | 0x40           |
| TMRx_BDT      | Braking and deadband register           | 0x44           |
| TMRx_DCTRL    | DMA control register                    | 0x48           |
| TMRx_DMADDR   | DMA address register of continuous mode | 0x4C           |

## 14.6 Register functional description

### 14.6.1 Control register 1 (TMRx\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CNTEN  | R/W | Counter Enable<br>0: Disable<br>1: Enable<br>When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.                                                                                                 |
| 1     | UD     | R/W | Update Disable<br>Update event can cause AUTORLD, PSC and CCx to generate the value of update setting.<br>0: Update event is allowed (UEV)<br>An update event can occur in any of the following situations:<br>The counter overruns/underruns;<br>Set UEG bit;<br>Update generated by slave mode controller.<br>1: Update event is disabled                                      |
| 2     | URSSEL | R/W | Update Request Source Select<br>If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit.<br>0: The counter overruns or underruns<br>Set UEG bit;<br>Update generated by slave mode controller.<br>1: The counter overruns or underruns                                  |
| 3     | SPMEN  | R/W | Single Pulse Mode Enable<br>When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed.<br>0: Disable<br>1: Enable                                                                                                     |
| 4     | CNTDIR | R/W | Counter Direction<br>This bit is read-only when the counter is configured as center-aligned mode or encoder mode.<br>0: Count up<br>1: Count down                                                                                                                                                                                                                                |
| 6:5   | CAMSEL | R/W | Center Aligned Mode Select<br>In the center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different center-aligned modes affect the timing of setting the output compare interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the center-aligned mode.<br>00: Edge alignment mode |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 01: Center-aligned mode 1 (the output compare interrupt flag bit of output channel is set to 1 when counting down)<br>10: Center-aligned mode 2 (the output compare interrupt flag bit of output channel is set to 1 when counting up)<br>11: Center-aligned mode 3 (the output compare interrupt flag bit of output channel is set to 1 when counting up/down) |
| 7     | ARPEN    | R/W | Auto-reload Preload Enable<br>When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event.<br>0: Disable<br>1: Enable                                  |
| 9:8   | CLKDIV   | R/W | Clock Divide Factor<br>For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit.<br>00: $t_{DTS}=t_{CK\_INT}$<br>01: $t_{DTS}=2 \times t_{CK\_INT}$<br>10: $t_{DTS}=4 \times t_{CK\_INT}$<br>11: Reserved                                    |
| 15:10 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                 |

#### 14.6.2 Control register 2 (TMRx\_CTRL2)

Offset address: 0x04

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CCPEN    | R/W | Capture/Compare Preloaded Enable<br>This bit affects the change of CCxEN, CCxNEN and OCxMOD values. When preloading is disabled, the program modification will immediately affect the timer setting; When preloading is enabled, it is only updated after COMG is set, so as to affect the setting of timer; this bit only works on channels with complementary output.<br>0: Disable<br>1: Enable |
| 1     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                    |
| 2     | CCUSEL   | R/W | Capture/compare Control Update Select<br>Only when the capture/compare preload is enabled (CCPEN=1), it works only for complementary output channel.<br>0: It can only be updated by setting COMG bit<br>1: It can be updated by setting COMG bit or rising edge on TRGI                                                                                                                           |
| 3     | CCDSEL   | R/W | Capture/compare DMA Select<br>0: Transmit DMA request of CCx when CCx event occurs<br>1: Transmit DMA request of CCx when an update event occurs                                                                                                                                                                                                                                                   |
| 6:4   | MMSEL    | R/W | Master Mode Signal Select                                                                                                                                                                                                                                                                                                                                                                          |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | <p>The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode.</p> <p>000: Reset; the reset signal of master mode timer is used for TRGO</p> <p>001: Enable; the counter enable signal of master mode timer is used for TRGO</p> <p>010: Update; the update event of master mode timer is used for TRGO</p> <p>011: Compare pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO</p> <p>100: Compare mode 1; OC1REF is used to trigger TRGO</p> <p>101: Compare mode 2; OC2REF is used to trigger TRGO</p> <p>110: Compare mode 3; OC3REF is used to trigger TRGO</p> <p>111: Compare mode 4; OC4REF is used to trigger TRGO</p> |
| 7     | TI1SEL   | R/W | <p>Timer Input 1 Selection</p> <p>0: TMRx_CH1 pin is connected to TI1 input</p> <p>1: TMRx_CH1, TMRx_CH2 and TMRx_CH3 pins are connected to TI1 input after exclusive</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 8     | OC1OIS   | R/W | <p>OC1 Output Idle State Configure</p> <p>Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is implemented.</p> <p>0: OC1=0</p> <p>1: OC1=1</p> <p>Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 9     | OC1NOIS  | R/W | <p>OC1N Output Idle State Configure</p> <p>Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is implemented.</p> <p>0: OC1N=0</p> <p>1: OC1N=1</p> <p>Note: When PLOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 10    | OC2OIS   | R/W | Configure OC2 output idle state. Refer to OC1OIS bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11    | OC2NOIS  | R/W | Configure OC2N output idle state. Refer to OC1NOIS bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 12    | OC3OIS   | R/W | Configure OC3 output idle state. Refer to OC1OIS bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 13    | OC3NOIS  | R/W | Configure OC3N output idle state. Refer to OC1NOIS bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 14    | OC4OIS   | R/W | Configure OC4 output idle state. Refer to OC1OIS bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 15    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 14.6.3 Slave mode control register (TMRx\_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | SMFSEL   | R/W | <p>Slave Mode Function Select</p> <p>000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock.</p> <p>001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2.</p> <p>010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1.</p> <p>011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2.</p> <p>100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register.</p> <p>101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period.</p> <p>110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI.</p> <p>111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.</p> |
| 3     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 6:4   | TRGSEL   | R/W | <p>Trigger Input Signal Select</p> <p>In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0.</p> <p>000: Internal trigger ITR0</p> <p>001: Internal trigger ITR1</p> <p>010: Internal trigger ITR2</p> <p>011: Internal trigger ITR3</p> <p>100: Channel 1 input edge detector TIF_ED</p> <p>101: Channel 1 post-filtering timer input TI1FP1</p> <p>110: Channel 2 post-filtering timer input TI2FP2</p> <p>111: External trigger input (ETRF)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 7     | MSMEN    | R/W | <p>Master/slave Mode Enable</p> <p>0: Invalid</p> <p>1: Enable the master/slave mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |



| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:8  | ETFCFG | R/W | <p>External Trigger Filter Configure</p> <p>0000: Filter disabled, sampling by <math>f_{DTS}</math></p> <p>0001: DIV=1, N=2</p> <p>0010: DIV=1, N=4</p> <p>0011: DIV=1, N=8</p> <p>0100: DIV=2, N=6</p> <p>0101: DIV=2, N=8</p> <p>0110: DIV=4, N=6</p> <p>0111: DIV=4, N=8</p> <p>1000: DIV=8, N=6</p> <p>1001: DIV=8, N=8</p> <p>1010: DIV=16, N=5</p> <p>1011: DIV=16, N=6</p> <p>1100: DIV=16, N=8</p> <p>1101: DIV=32, N=5</p> <p>1110: DIV=32, N=6</p> <p>1111: DIV=32, N=8</p> <p>Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.</p> |
| 13:12 | ETPCFG | R/W | <p>External Trigger Prescaler Configure</p> <p>The ETR (external trigger input) signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMRxCLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division.</p> <p>00: The prescaler is disabled;</p> <p>01: ETR signal 2 divided frequency</p> <p>10: ETR signal 4 divided frequency</p> <p>11: ETR signal 8 divided frequency</p>                                                                                                                                     |
| 14    | ECEN   | R/W | <p>External Clock Enable Mode2</p> <p>0: Disable</p> <p>1: Enable</p> <p>Setting ECEN bit has the same function as selecting external clock mode 1 to connect TRGI to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.</p>                                                                                                                                                    |
| 15    | ETPOL  | R/W | <p>External Trigger Polarity Configure</p> <p>This bit decides whether the external trigger ETR is reversed.</p> <p>0: The external trigger ETR is not reversed, and the high level or rising edge is valid</p> <p>1: The external trigger ETR is reversed, and the low level or falling edge is valid</p>                                                                                                                                                                                                                                                                                                 |

Table 65 TMRx Internal Trigger Connection

| Slave timer | ITR1 (TS=000) | ITR1 (TS=001) | ITR2 (TS=010) | ITR3 (TS=011) |
|-------------|---------------|---------------|---------------|---------------|
| TMR1        | TMR5          | TMR2          | TMR3          | TMR4          |

|      |      |      |      |      |
|------|------|------|------|------|
| TMR8 | TMR1 | TMR2 | TMR4 | TMR5 |
|------|------|------|------|------|

#### 14.6.4 DMA/Interrupt enable register (TMRx\_DIEN)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name   | R/W | Description                                                            |
|-------|--------|-----|------------------------------------------------------------------------|
| 0     | UIEN   | R/W | Update interrupt Enable<br>0: Disable<br>1: Enable                     |
| 1     | CC1IEN | R/W | Capture/Compare Channel1 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 2     | CC2IEN | R/W | Capture/Compare Channel2 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 3     | CC3IEN | R/W | Capture/Compare Channel3 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 4     | CC4IEN | R/W | Capture/Compare Channel4 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 5     | COMIEN | R/W | COM Interrupt Enable<br>0: Disable<br>1: Enable                        |
| 6     | TRGIEN | R/W | Trigger interrupt Enable<br>0: Disable<br>1: Enable                    |
| 7     | BRKIEN | R/W | Break interrupt Enable<br>0: Disable<br>1: Enable                      |
| 8     | UDIEN  | R/W | Update DMA Request Enable<br>0: Disable<br>1: Enable                   |
| 9     | CC1DEN | R/W | Capture/Compare Channel1 DMA Request Enable<br>0: Disable<br>1: Enable |
| 10    | CC2DEN | R/W | Capture/Compare Channel2 DMA Request Enable<br>0: Disable<br>1: Enable |
| 11    | CC3DEN | R/W | Capture/Compare Channel3 DMA Request Enable<br>0: Disable<br>1: Enable |
| 12    | CC4DEN | R/W | Capture/Compare Channel4 DMA Request Enable<br>0: Disable<br>1: Enable |

| Field | Name     | R/W | Description                                           |
|-------|----------|-----|-------------------------------------------------------|
| 13    | COMDEN   | R/W | COM DMA Request Enable<br>0: Disable<br>1: Enable     |
| 14    | TRGDEN   | R/W | Trigger DMA Request Enable<br>0: Disable<br>1: Enable |
| 15    | Reserved |     |                                                       |

#### 14.6.5 State register (TMRx\_STS)

Offset address: 0x10

Reset value: 0x0000

| Field | Name    | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|---------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UIFLG   | RC_W0 | Update Event Interrupt Generate Flag<br>0: Update event interrupt does not occur<br>1: Update event interrupt occurs<br>When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations:<br>(1) UD=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated;<br>(2) URSSEL=0 and UD=0 on TMRx_CTRL1 register, configure UEG=1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software;<br>(3) URSSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event. |
| 1     | CC1IFLG | RC_W0 | Capture/Compare Channel1 Interrupt Flag<br>When the capture/compare channel 1 is configured as output:<br>0: No matching occurred<br>1: The value of TMRx_CNT matches the value of TMRx_CC1<br>When the capture/compare channel 1 is configured as input:<br>0: Input capture did not occur<br>1: Input capture occurred<br>When capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.                                                                                                                                                                                                                                                                                                |
| 2     | CC2IFLG | RC_W0 | Capture/Compare Channel2 Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 3     | CC3IFLG | RC_W0 | Capture/Compare Channel3 Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4     | CC4IFLG | RC_W0 | Capture/Compare Channel4 Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                  |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5     | COMIFLG  | RC_W0 | COM Event Interrupt Generate Flag<br>0: COM event does not occur<br>1: COM interrupt waits for response<br>After COM event is generated, this bit is set to 1 by hardware and cleared by software.                                                                                                           |
| 6     | TRGIFLG  | RC_W0 | Trigger Event Interrupt Generate Flag<br>0: Trigger event interrupt did not occur<br>1: Trigger event interrupt occurred<br>After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.                                                                                      |
| 7     | BRKIFLG  | RC_W0 | Brake Event Interrupt Generate Flag<br>0: Brake event does not occur<br>1: Brake event occurs<br>When brake input is valid, this bit is set to 1 by hardware; when brake input is invalid, this bit can be cleared by software.                                                                              |
| 8     | Reserved |       |                                                                                                                                                                                                                                                                                                              |
| 9     | CC1RCFLG | RC_W0 | Capture/compare Channel1 Repetition Capture Flag<br>0: Repeat capture does not occur<br>1: Repeat capture occurs<br>The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture. |
| 10    | CC2RCFLG | RC_W0 | Capture/compare Channel2 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                    |
| 11    | CC3RCFLG | RC_W0 | Capture/compare Channel3 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                    |
| 12    | CC4RCFLG | RC_W0 | Capture/compare Channel4 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                    |
| 15:13 | Reserved |       |                                                                                                                                                                                                                                                                                                              |

#### 14.6.6 Control event generation register (TMRx\_CEG)

Offset address: 0x14

Reset value: 0x0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UEG  | W   | Update Event Generate<br>0: Invalid<br>1: Initialize the counter and generate the update event<br>This bit is set to 1 by software, and cleared by hardware.<br>Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared to 0. |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | CC1EG    | W   | <p>Capture/Compare Channel1 Event Generation</p> <p>0: Invalid</p> <p>1: Capture/Compare event is generated</p> <p>This bit is set to 1 by software and cleared automatically by hardware.</p> <p>If Channel 1 is in output mode:</p> <p>When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated.</p> <p>If Channel 1 is in input mode:</p> <p>The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.</p> |
| 2     | CC2EG    | W   | <p>Capture/Compare Channel2 Event Generation</p> <p>Refer to CC1EG description</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 3     | CC3EG    | W   | <p>Capture/Compare Channel3 Event Generation</p> <p>Refer to CC1EG description</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 4     | CC4EG    | W   | <p>Capture/Compare Channel4 Event Generation</p> <p>Refer to CC1EG description</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 5     | COMG     | W   | <p>Capture/Compare Control Update Event Generate</p> <p>0: Invalid</p> <p>1: Capture/Compare update event is generated</p> <p>This bit is set to 1 by software and cleared automatically by hardware.</p> <p>Note: COMG bit is valid only in complementary output channel.</p>                                                                                                                                                                                                                                                                                                                                                                                                   |
| 6     | TEG      | W   | <p>Trigger Event Generate</p> <p>0: Invalid</p> <p>1: Trigger event is generated</p> <p>This bit is set to 1 by software and cleared automatically by hardware.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7     | BEG      | W   | <p>Brake Event Generate</p> <p>0: Invalid</p> <p>1: Brake event is generated</p> <p>This bit is set to 1 by software and cleared automatically by hardware.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

#### 14.6.7 Capture/Compare mode register 1 (TMRx\_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCx in the register describes the function of the channel in the output mode, and the ICx in the register describes the function of the channel in the input mode.

**Output compare mode:**

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL | R/W | <p>Capture/Compare Channel 1 Selection</p> <p>This bit defines the input/output direction and the selected input pin.</p> <p>00: CC1 channel is output</p> <p>01: CC1 channel is input, and IC1 is mapped on TI1</p> <p>10: CC1 channel is input, and IC1 is mapped on TI2</p> <p>11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input</p> <p>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2     | OC1FEN | R/W | <p>Output Compare Channel1 Fast Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>This bit is used to improve the response of the capture/compare output to the trigger input event.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 3     | OC1PEN | R/W | <p>Output Compare Channel1 Preload Enable</p> <p>0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately.</p> <p>1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated.</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 6:4   | OC1MOD | R/W | <p>Output Compare Channel1 Mode Configure</p> <p>000: Freeze The output compare has no effect on OC1REF</p> <p>001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture compare register, OC1REF will be forced to be at high level</p> <p>010: The output value is low when matching. When the value of the counter matches the value of the capture compare register, OC1REF will be forced to be at low level</p> <p>011: Output flaps when matching. When the value of the counter matches the value of the capture compare register, flap the level of OC1REF</p> <p>100: The output is forced to be low Force OC1REF to be at low level</p> <p>101: The output is forced to be high. Force OC1REF to be at high level</p> <p>110: PWM mode 1 (set to high when the counter value&lt;output compare value; otherwise, set to low)</p> <p>111: PWM mode 2 (set to high when the counter value&gt;output compare value; otherwise, set to low)</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output compare mode changes from freeze mode to PWM mode.</p> |
| 7     | OC1CEN | R/W | <p>Output Compare Channel1 Clear Enable</p> <p>0: OC1REF is unaffected by ETRF input.</p> <p>1: When high level of ETRF input is detected, OC1REF=0</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8   | CC2SEL | R/W | Capture/Compare Channel2 Select<br>This bit defines the input/output direction and the selected input pin.<br>00: CC2 channel is output<br>01: CC2 channel is input, and IC2 is mapped on TI2<br>10: CC2 channel is input, and IC2 is mapped on TI1<br>11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0). |
| 10    | OC2FEN | R/W | Output Compare Channel2 Preload Enable                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11    | OC2PEN | R/W | Output Compare Channel2 Buffer Enable                                                                                                                                                                                                                                                                                                                                                                                                              |
| 14:12 | OC2MOD | R/W | Output Compare Channel1 Mode                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15    | OC2CEN | R/W | Output Compare Channel2 Clear Enable                                                                                                                                                                                                                                                                                                                                                                                                               |

#### Input capture mode:

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                               |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL | R/W | Capture/Compare Channel 1 Select<br>00: CC1 channel is output<br>01: CC1 channel is input, and IC1 is mapped on TI1<br>10: CC1 channel is input, and IC1 is mapped on TI2<br>11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN bit CC1EN=0).                       |
| 3:2   | IC1PSC | R/W | Input Capture Channel 1 Perscaler Configure<br>00: PSC=1<br>01: PSC=2<br>10: PSC=4<br>11: PSC=8<br>PSC is prescaled factor, which triggers capture once every PSC events.                                                                                                                                                                                                                 |
| 7:4   | IC1F   | R/W | Input Capture Channel 1 Filter Configuration<br>0000: Filter disabled, sampling by $f_{DTS}$<br>0001: DIV=1, N=2<br>0010: DIV=1, N=4<br>0011: DIV=1, N=8<br>0100: DIV=2, N=6<br>0101: DIV=2, N=8<br>0110: DIV=4, N=6<br>0111: DIV=4, N=8<br>1000: DIV=8, N=6<br>1001: DIV=8, N=8<br>1010: DIV=16, N=5<br>1011: DIV=16, N=6<br>1100: DIV=16, N=8<br>1101: DIV=32, N=5<br>1110: DIV=32, N=6 |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |        |     | 1111: DIV=32, N=8<br>Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.                                                                                                                                                                                                                           |
| 9:8   | CC2SEL | R/W | Capture/Compare Channel 2 Select<br>00: CC2 channel is output<br>01: CC2 channel is input, and IC2 is mapped on TI2<br>10: CC2 channel is input, and IC2 is mapped on TI1<br>11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0). |
| 11:10 | IC2PSC | R/W | Input Capture Channel 2 Perscaler Configuration                                                                                                                                                                                                                                                                                                                          |
| 15:12 | IC2F   | R/W | Input Capture Channel 2 Filter Configuration                                                                                                                                                                                                                                                                                                                             |

#### 14.6.8 Capture/Compare mode register 2 (TMRx\_CCM2)

Offset address: 0x1C

Reset value: 0x0000

Refer to the description of the above CCM1 register.

**Output compare mode:**

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC3SEL | R/W | Capture/Compare Channel 1 Selection<br>This bit defines the input/output direction and the selected input pin.<br>00: CC3 channel is output<br>01: CC3 channel is input, and IC3 is mapped on TI3<br>10: CC3 channel is input, and IC3 is mapped on TI4<br>11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC3EN=0). |
| 2     | OC3FEN | R/W | Output Compare Channel3 Fast Enable<br>0: Disable<br>1: Enable<br>This bit is used to improve the response of the capture/compare output to the trigger input event.                                                                                                                                                                                                                                                                                   |
| 3     | OC3PEN | R/W | Output Compare Channel3 Preload Enable                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 6:4   | OC3MOD | R/W | Output Compare Channel3 Mode Configure                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7     | OC3CEN | R/W | Output Compare Channel3 Clear Enable<br>0: OC3REF is unaffected by ETRF input.<br>1: When high level of ETRF input is detected, OC1REF=0                                                                                                                                                                                                                                                                                                               |
| 9:8   | CC4SEL | R/W | Capture/Compare Channel 4 Selection<br>This bit defines the input/output direction and the selected input pin.<br>00: CC4 channel is output<br>01: CC4 channel is input, and IC4 is mapped on TI4<br>10: CC4 channel is input, and IC4 is mapped on TI3                                                                                                                                                                                                |



| Field | Name   | R/W | Description                                                                                                                                                                                 |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |        |     | 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC4EN=0). |
| 10    | OC4FEN | R/W | Output Compare Channel4 Preload Enable                                                                                                                                                      |
| 11    | OC4PEN | R/W | Output Compare Channel4 Buffer Enable                                                                                                                                                       |
| 14:12 | OC4MOD | R/W | Output Compare Channel4 Mode Configure                                                                                                                                                      |
| 15    | OC4CEN | R/W | Output Compare Channel4 Clear Enable                                                                                                                                                        |

#### Input capture mode:

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC3SEL | R/W | Capture/Compare Channel 3 Select<br>00: CC3 channel is output<br>01: CC3 channel is input, and IC3 is mapped on TI3<br>10: CC3 channel is input, and IC3 is mapped on TI4<br>11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC3EN=0). |
| 3:2   | IC3PSC | R/W | Input Capture Channel 3 Perscaler Configuration<br>00: PSC=1<br>01: PSC=2<br>10: PSC=4<br>11: PSC=8<br>PSC is prescaled factor, which triggers capture once every PSC events.                                                                                                                                                                                            |
| 7:4   | IC3F   | R/W | Input Capture Channel 3 Filter Configuration                                                                                                                                                                                                                                                                                                                             |
| 9:8   | CC4SEL | R/W | Capture/Compare Channel 4 Select<br>00: CC4 channel is output<br>01: CC4 channel is input, and IC4 is mapped on TI4<br>10: CC4 channel is input, and IC4 is mapped on TI3<br>11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC4EN=0). |
| 11:10 | IC4PSC | R/W | Input Capture Channel 4 Perscaler Configuration                                                                                                                                                                                                                                                                                                                          |
| 15:12 | IC4F   | R/W | Input Capture Channel 4 Filter Configuration                                                                                                                                                                                                                                                                                                                             |

#### 14.6.9 Capture/Compare enable register (TMRx\_CCEN)

Offset address: 0x20

Reset value: 0x0000

| Field | Name  | R/W | Description                                                                                                                                            |
|-------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CC1EN | R/W | Capture/Compare Channel1 Output Enable<br>When the capture/compare channel 1 is configured as output:<br>0: Output is disabled<br>1: Output is enabled |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | When the capture/compare channel 1 is configured as input:<br>This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register<br>0: Capture is disabled<br>1: Capture is enabled                                                                                                                                                                                                                                                                                                  |
| 1     | CC1POL   | R/W | Capture/Compare Channel1 Output Polarity Configure<br>When CC1 channel is configured as output:<br>0: OC1 high level is valid<br>1: OC1 low level is valid<br>When CC1 channel is configured as input:<br>0: Phase not reversed: capture at the rising edge of IC1; phase not reversed when IC1 is used as external trigger.<br>1: Phase reversed, capture at the falling edge of ICC1; phase reversed when IC1 is used as external trigger.<br>Note: When the protection level is 2 or 3, this bit cannot be modified |
| 2     | CC1NEN   | R/W | Capture/Compare Channel1 Complementary Output Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3     | CC1NPOL  | R/W | Capture/Compare Channel1 Complementary Output Polarity<br>0: OC1N high level is valid<br>1: OC1N low level is valid<br>Note: When the protection level is 2 or 3, this bit cannot be modified                                                                                                                                                                                                                                                                                                                          |
| 4     | CC2EN    | R/W | Enable output of capture/compare channel 2 (Capture/Compare Channel2 Output Enable)<br>Refer to CCEN_CC1EN                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5     | CC2POL   | R/W | Capture/Compare Channel2 Output Polarity Configure<br>Refer to CCEN_CC1POL                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 6     | CC2NEN   | R/W | Capture/Compare Channel1 Complementary Output Enable<br>Refer to CCEN_CC1NEN                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7     | CC2NPOL  | R/W | Capture/Compare Channel2 Complementary Output Polarity Configure<br>Refer to CCEN_CC1NPOL                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 8     | CC3EN    | R/W | Capture/Compare Channel3 Output Enable<br>Refer to CCEN_CC1EN                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | CC3POL   | R/W | Capture/Compare Channel3 Output Polarity Configure<br>Refer to CCEN_CC1POL                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 10    | CC3NEN   | R/W | Capture/Compare Channel3 Complementary Output Enable<br>Refer to CCEN_CC1NEN                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11    | CC3NPOL  | R/W | Capture/Compare Channel3 Complementary Output Polarity Configure<br>Refer to CCEN_CC1NPOL                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 12    | CC4EN    | R/W | Capture/Compare Channel4 Output Enable<br>Refer to CCEN_CC1EN                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 13    | CC4POL   | R/W | Capture/Compare Channel4 Output Polarity<br>Refer to CCEN_CC1POL                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15:14 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

#### 14.6.10 Counter register (TMRx\_CNT)

Offset address: 0x24

Reset value: 0x0000

| Field | Name | R/W | Description   |
|-------|------|-----|---------------|
| 15:0  | CNT  | R/W | Counter Value |

#### 14.6.11 Prescaler register (TMRx\_PSC)

Offset address: 0x28

Reset value: 0x0000

| Field | Name | R/W | Description                                                                        |
|-------|------|-----|------------------------------------------------------------------------------------|
| 15:0  | PSC  | R/W | Prescaler Value<br>Clock frequency of counter (CK_CNT) = $f_{CK\_PSC} / (PSC + 1)$ |

#### 14.6.12 Auto reload register (TMRx\_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF FFFF

| Field | Name    | R/W | Description                                                                              |
|-------|---------|-----|------------------------------------------------------------------------------------------|
| 15:0  | AUTORLD | R/W | Auto Reload Value<br>When the value of auto reload is empty, the counter will not count. |

#### 14.6.13 Repeat count register (TMRx\_REPCNT)

Offset address: 0x30

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | REPCNT   | R/W | Repetition Counter Value<br>When the count value of the repeat counter is reduced to 0, an update event will be generated, and the counter will start counting again from the REPCNT value; the new value newly written to this register is valid only when an update event occurs in next cycle. |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                                                                   |

#### 14.6.14 Channel 1 capture/compare register (TMRx\_CC1)

Offset address: 0x34

Reset value: 0x0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | CC1  | R/W | Capture/Compare Channel 1 Value<br>When the capture/compare channel 1 is configured as input mode:<br>CC1 contains the counter value transmitted by the last input capture channel 1 event.<br>When the capture/compare channel 1 is configured as output mode:<br>CC1 contains the current load capture/compare register value<br>Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1.<br>When the output compare preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output comparison results; |

| Field | Name | R/W | Description                                                                                                                                                            |
|-------|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |      |     | If the output compare preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output compare result when an update event is generated. |

#### 14.6.15 Channel 2 capture/compare register (TMRx\_CC2)

Offset address: 0x38

Reset value: 0x0000

| Field | Name | R/W | Description                                          |
|-------|------|-----|------------------------------------------------------|
| 15:0  | CC2  | R/W | Capture/Compare Channel 2 Value<br>Refer to TMRx_CC1 |

#### 14.6.16 Channel 3 capture/compare register (TMRx\_CC3)

Offset address: 0x3C

Reset value: 0x0000

| Field | Name | R/W | Description                                          |
|-------|------|-----|------------------------------------------------------|
| 15:0  | CC3  | R/W | Capture/Compare Channel 3 Value<br>Refer to TMRx_CC1 |

#### 14.6.17 Channel 4 capture/compare register (TMRx\_CC4)

Offset address: 0x40

Reset value: 0x0000

| Field | Name | R/W | Description                                          |
|-------|------|-----|------------------------------------------------------|
| 15:0  | CC4  | R/W | Capture/Compare Channel 4 Value<br>Refer to TMRx_CC1 |

#### 14.6.18 Brake and deadband register (TMRx\_BDT)

Offset address: 0x44

Reset value: 0x0000

Note: According to the lock setting, AOEN, BRKPOL, BRKEN, IMOS, RMOS and DTS[7:0] bits all can be write-protected, and it is necessary to configure them when writing to TMRx\_BDT register for the first time.

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | DTS  | R/W | <p>Dead Time Setup</p> <p>DT is the dead duration, and the relationship between DT and register DTS is as follows:</p> <p><math>DTS[7:5]=0xx \Rightarrow DT=DTS[7:0] \times T_{DTS}, T_{DTS}=T_{DTS};</math></p> <p><math>DTS[7:5]=10x \Rightarrow DT=(64+DTS[5:0]) \times T_{DTS}, T_{DTS}=2 \times T_{DTS};</math></p> <p><math>DTS[7:5]=110 \Rightarrow DT=(32+DTS[4:0]) \times T_{DTS}, T_{DTS}=8 \times T_{DTS};</math></p> <p><math>DTS[7:5]=111 \Rightarrow DT=(32+DTS[4:0]) \times T_{DTS}, T_{DTS}=16 \times T_{DTS};</math></p> <p>For example: assuming <math>T_{DTS}=125ns</math> (8MHZ), the dead time setting is as follows:</p> <p>If the step time is 125ns, the dead time can be set from 0 to 15875ns;</p> <p>If the step time is 250ns, the dead time can be set from 16us to 31750ns;</p> <p>If the step time is 1us, the dead time can be set from 32us to 63us;</p> <p>If the step time is 2us, the dead time can be set from 64us to 126us.</p> |

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |         |     | Note: Once LOCK level (LOCKCFG bit in TMRx_BDT register) is set to 1, 2 or 3, these bits cannot be modified.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 9:8   | LOCKCFG | R/W | <p>Lock Write Protection Mode Configuration</p> <p>00: Without Lock write protection level; the register can be written directly</p> <p>01: Lock write protection level 1<br/>It cannot be written to DTS, BRKEN, BRKPOL and AOEN bits of TMRx_BDT, and OCxOIS and OCxNOIS bits of TMRx_CTRL2 register.</p> <p>02: Lock write protection level 2<br/>It is not allowed to write to all bits with protection level 1 and write to the CCxPOL and OCxNPOL bits in TMRx_CCEN register and the RMOS and IMOS bits in TMRx_BDT register.</p> <p>11: Lock write protection level 3<br/>It is not allowed to write to all bits with protection level 2, and write to the OCxMOD and OCxPEN bits of TMRx_CCMx register.</p> <p>Note: After system reset, the lock write protect bit can only be written once.</p> |
| 10    | IMOS    | R/W | <p>Idle Mode Off-state Configure</p> <p>Idle mode means MOEN=0; disable means CCxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=0 and CCxEN changes from 0 to 1.</p> <p>0: OCx/OCxN output is disabled</p> <p>1: If CCxEN=1, the invalid level is output during the dead time (the specific level value is affected by the polarity configuration), and the idle level is output after the dead time</p>                                                                                                                                                                                                                                                                                                                                           |
| 11    | RMOS    | R/W | <p>Run Mode Off-state Configure</p> <p>Run mode means MOEN=1; disable means CCxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=1 and CCxEN changes from 0 to 1.</p> <p>0: OCx/OCxN output is disabled</p> <p>1: OCx/OCxN first output invalid level (the specific level value is affected by the polarity configuration)</p>                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12    | BRKEN   | R/W | <p>Brake Function Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>Note: When the protection level is 1, this bit cannot be modified.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13    | BRKPOL  | R/W | <p>Brake Polarity Configure</p> <p>0: The brake input BRK is valid at low level</p> <p>1: The brake input BRK is valid at high level</p> <p>Note: When the protection level is 1, this bit cannot be modified. Writing to this bit requires an APB clock delay before it can be used.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 14    | AOEN    | R/W | <p>Automatic Output Enable</p> <p>0: MOEN can only be set to 1 by software</p> <p>1: MOEN can be set to 1 by software or be automatically set to 1 in next update event (braking input is ineffective)</p> <p>Note: When the protection level is 1, this bit cannot be modified.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 15    | MOEN    | R/W | <p>PWM Main Output Enable</p> <p>0: Disable the output of OCx and OCxN or force the output of idle state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                           |
|-------|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |      |     | <p>1: When CCxEN and CCxNEN bits of the TMRx_CCEN register are set, turn on OCx and OCxN output</p> <p>When the brake input is valid, it is cleared by hardware asynchronously.</p> <p>Note: Setting to 1 by software or setting to 1 automatically depends on AOEN bit of the TMRx_BDT register.</p> |

#### 14.6.19 DMA control software (TMRx\_DCTRL)

Offset address: 0x48

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | DBADDR   | R/W | <p>DMA Base Address Setup</p> <p>These bits define the base address of DMA in continuous mode (when reading or writing TMRx_DMADDR register), and DBADDR is defined as the offset from the address of TMRx_CTRL1 register:</p> <p>00000: TMRx_CTRL1<br/> 00001: TMRx_CTRL2<br/> 00010: TMRx_SMCTRL<br/> .....</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 7:5   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 12:8  | DBLEN    | R/W | <p>DMA Burst Transfer Length Setup</p> <p>These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits.</p> <p>When reading/writing TMRx_DMADDR register, the timer will conduct a continuous transmission;</p> <p>00000: Transmission once<br/> 00001: Transmission twice<br/> 00010: Transmission for three times<br/> .....<br/> 10001: Transmission for 18 times</p> <p>The transmission address formula is as follows:<br/> Transmission address=TMRx_CTRL1 address (slave address)<br/> +DBADDR+DMA index; DMA index=DBLEN</p> <p>For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMRx_CTRL1 means the address of the data to be written/read,</p> <p>Data transmission will occur to: TMRx_CTRL1 address + seven registers starting from DBADDR.</p> <p>The data transmission will change according to different DMA data length:</p> <p>(1) When the transmission data is set to 16 bits, the data will be transmitted to seven registers</p> <p>(2) When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.</p> |
| 15:13 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

#### 14.6.20 DMA address register of continuous mode (TMRx\_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | DMADDR | R/W | <p>DMA Register for Burst Transfer</p> <p>Read or write operation access of TMRx_DMADDR register may lead to access operation of the register in the following address:</p> <p><math>\text{TMRx\_CTRL1 address} + (\text{DBADDR} + \text{DMA index}) \times 4</math></p> <p>Wherein:</p> <p>"TMRx_CTRL1 address" is the address of control register 1 (TMRx_CTRL1);</p> <p>"DBADDR" is the base address defined in TMRx_DCTRL register;</p> <p>"DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMRx_DCTRL register.</p> |

## 15 General-purpose Timer (TMR2/3/4/5)

### 15.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform. It includes a 32-bit auto reload counter (for count-up, count-down and center-aligned count).

The timer and timer are independent of each other, and they can achieve synchronization and cascading.

### 15.2 Main characteristics

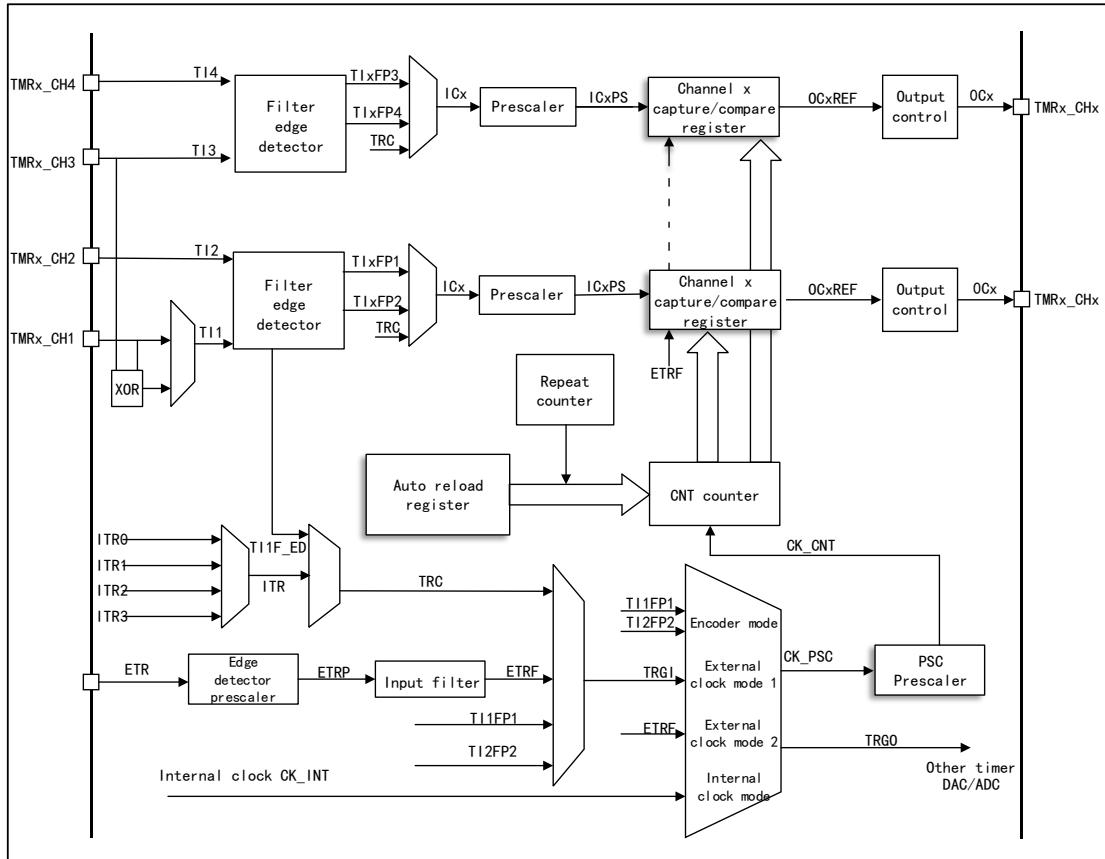
- (1) Timebase unit
  - Counter: 32-bit counter, count-up, count-down and center alignment count.
  - Prescaler: 16-bit programmable prescaler
  - Auto reloading function
- (2) Clock source selection
  - Internal clock
  - External input
  - External trigger
  - Internal trigger
- (3) Input capture function
  - Counting function
  - PWM input
  - Encoder interface mode
- (4) Output compare function
  - PWM output mode
  - Forced output mode
  - Single-pulse mode
- (5) Master/Slave mode controller of timer
  - Timers can be synchronized and cascaded
  - Support multiple slave modes and synchronization signals
- (6) Interrupt and DMA request event
  - Update event (counter overrun/underrun, counter initialization)
  - Trigger event (counter start, stop, internal/external trigger)
  - Input capture
  - Output compare



- (7) Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes

## 15.3 Structure block diagram

Figure 38 General-purpose Timer Structure Block Diagram



## 15.4 Functional description

### 15.4.1 Clock source selection

The general-purpose timer has four clock sources.

#### Internal clock

It is TMRx\_CLK from RCM, which is the driving clock of the timer. When the slave mode controller is disabled, the clock source CK\_PSC of the prescaler is driven by the internal clock CK\_INT.

#### External clock mode 1

The trigger signal generated from the input channel T11/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of channel 1 after double-edge detection of the rising edge and the falling edge

is logically equal or the future signal is TI1F\_ED signal, which is double-edge signal of TIF\_ED. Specially the PWM input can only be input by TI1/2.

## External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to slave mode controller through trigger input selector to control the work of counter.

## Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

### 15.4.2 Timebase unit

The time base unit in the general-purpose timer contains three registers

- 32-bit counter register (CNT)
- 32-bit auto reload register (AUTORLD)
- 16-bit prescaler register (PSC)

## Counter CNT

There are three counting modes for the counter in the general-purpose timer

- Count-up mode
- Count-down mode
- Center-aligned mode

## Count-up mode

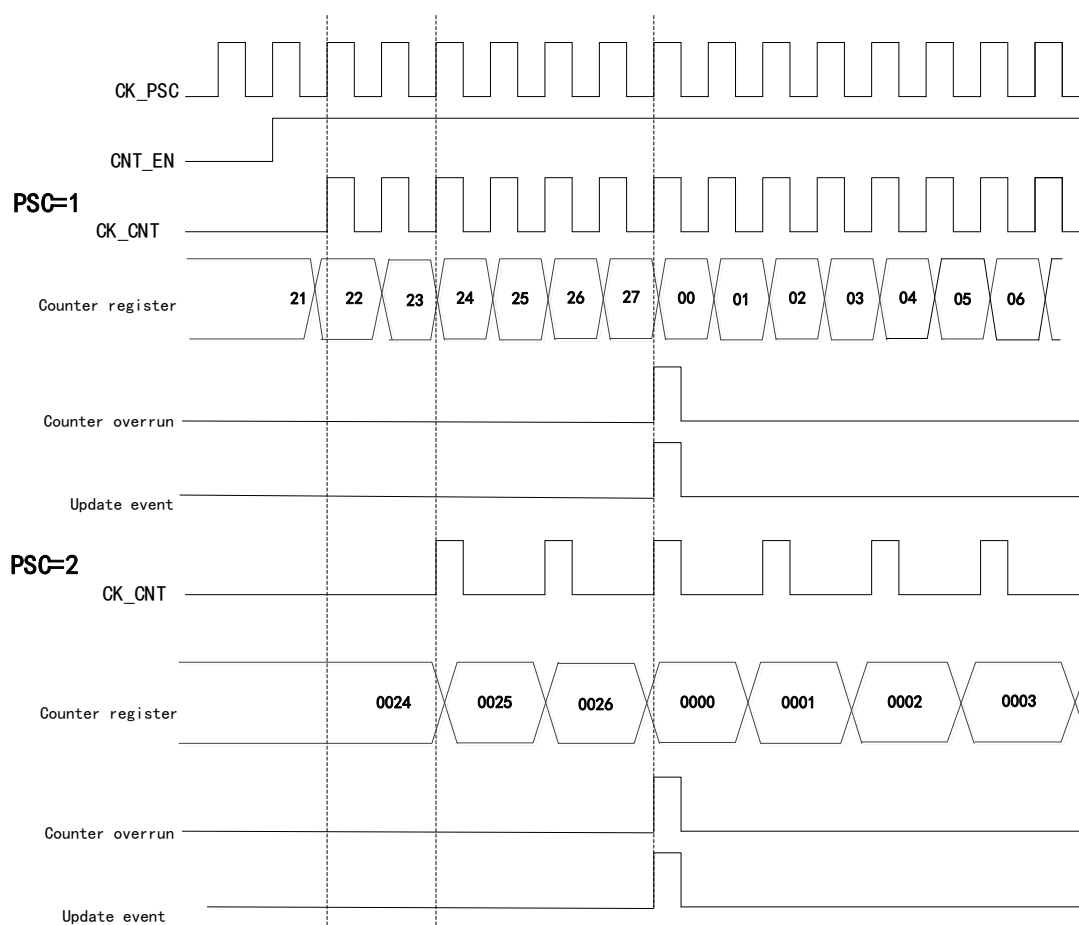
Set to the count-up mode by CNTDIR bit of configuration control register (TMRx\_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx\_CNT) is equal to the value of the auto reload (TMRx\_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMRx\_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMRx\_CTRL1.

The figure below is timing diagram when division factor is 1 or 2 in count-up mode.

Figure 39 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



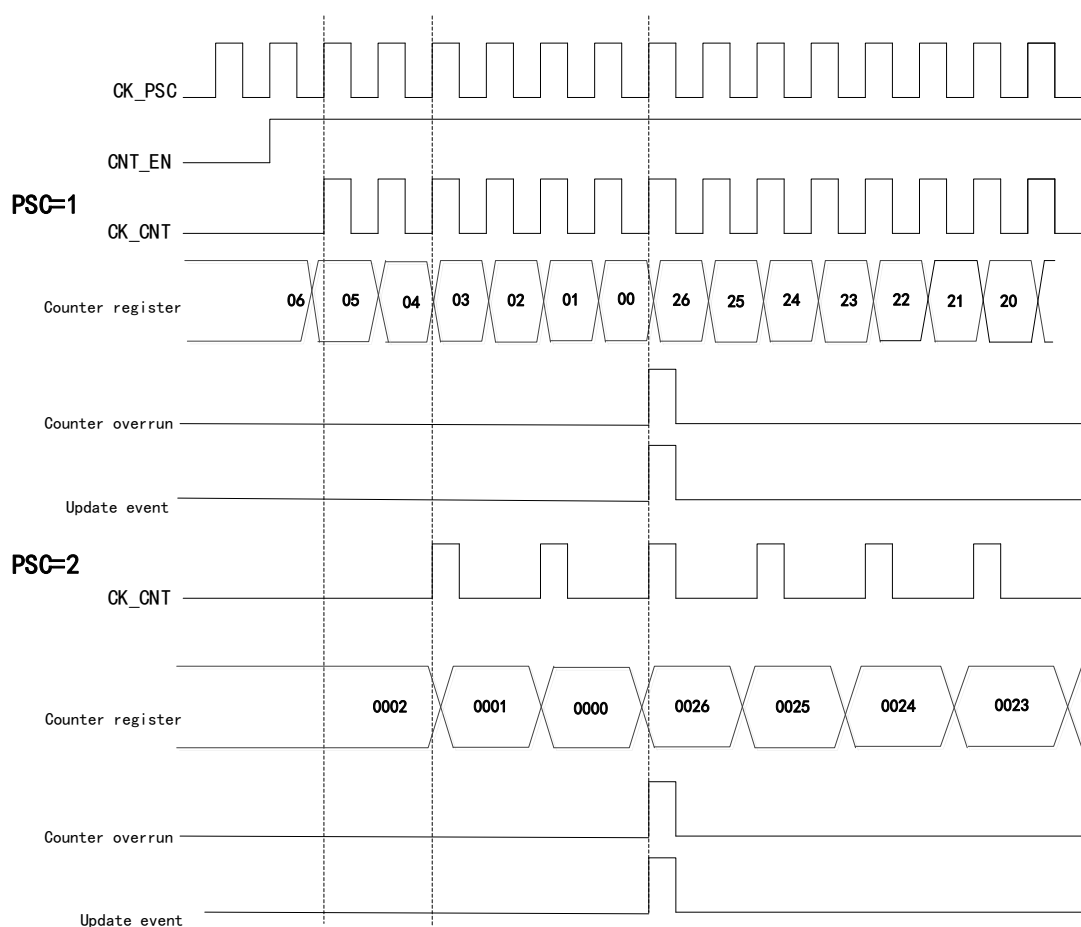
### Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMRx\_CTRL1).

When the counter is in count-down mode, the counter will start to count down from the value of the auto reload (TMRx\_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMRx\_AUTORLD). Meanwhile, a count-down overrun event will be generated, and the value of the auto reload (TMRx\_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the UD bit of the TMRx\_CTRL1 register.

Figure 40 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

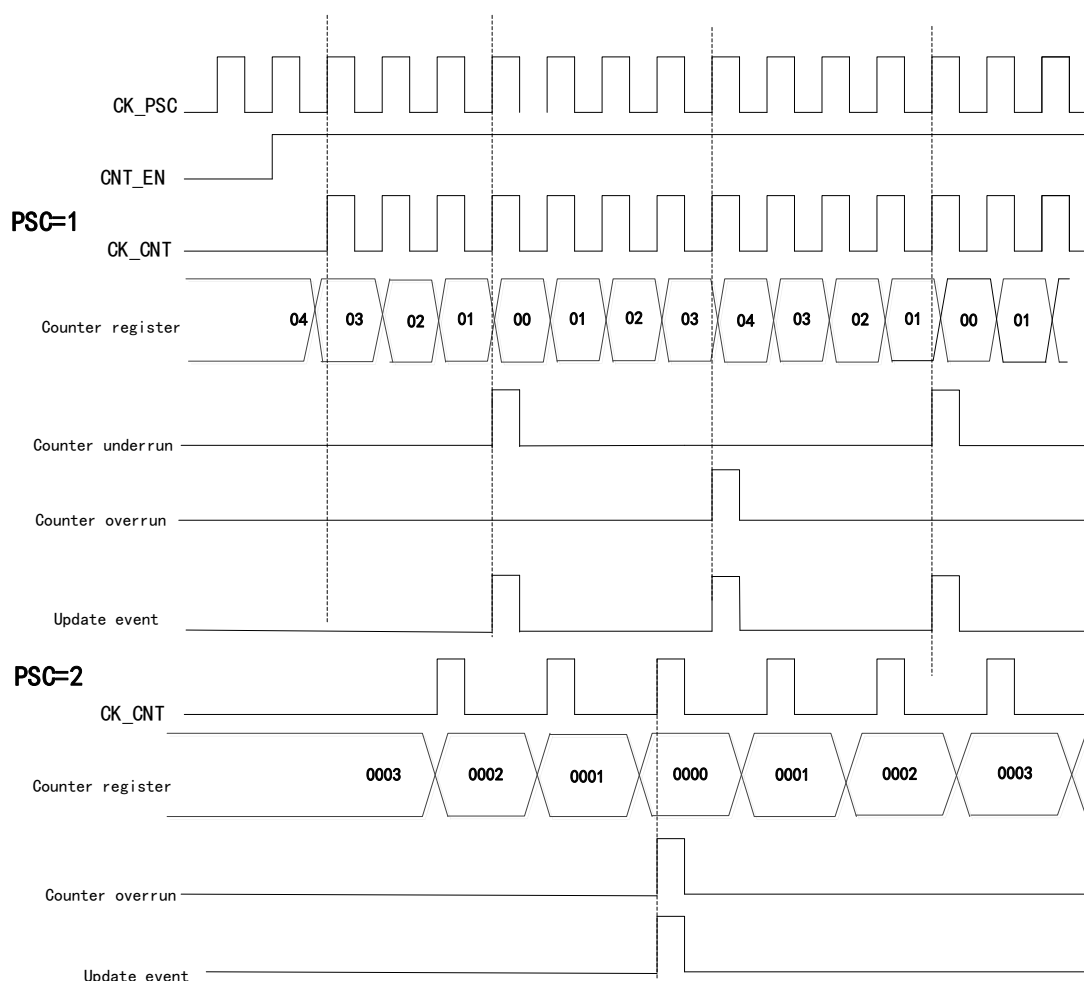


### Center-aligned mode

Set to the center-aligned mode by CAMSEL bit of configuration control register (TMRx\_CTRL1).

When the counter is in center-aligned mode, the counter counts up from 0 to the value of auto reload (TMRx\_AUTORLD), then counts down to 0 from the value of the auto reload (TMRx\_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 41 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



## Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx\_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

### 15.4.3 Input capture

#### Input capture channel

The general-purpose timer has four independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the

signal will pass through the prescaler, which is used to set how many events to capture at a time.

### Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width). For example, if the selected edge appears on the input pin, the TMRx\_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx\_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

#### 15.4.4 Output compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM mode 1 and PWM mode 2, which are configured by OCxMOD bit in TMRx\_CCMx register and can control the waveform of output signal in output compare mode.

### Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx\_CCMx register and the CCxPOL bit in the output polarity TMRx\_CCEN register.

When CCxIFLG=1 in TMRx\_STS register, if CCxIEN=1 in TMRx\_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx\_CTRL2 register, DMA request will be generated.

#### 15.4.5 PWM output mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle

is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and center alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7:

Figure 42 PWM1 Count-up Mode Timing Diagram

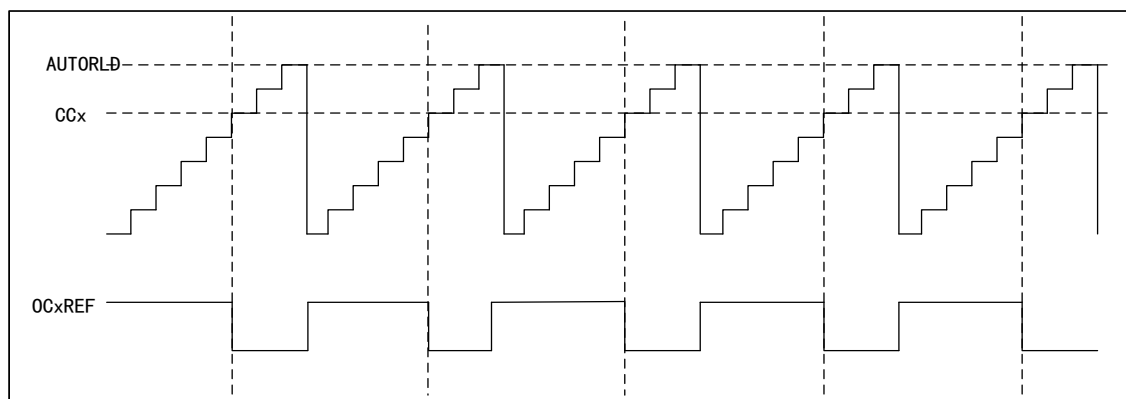


Figure 43 PWM1 Count-down Mode Timing Diagram

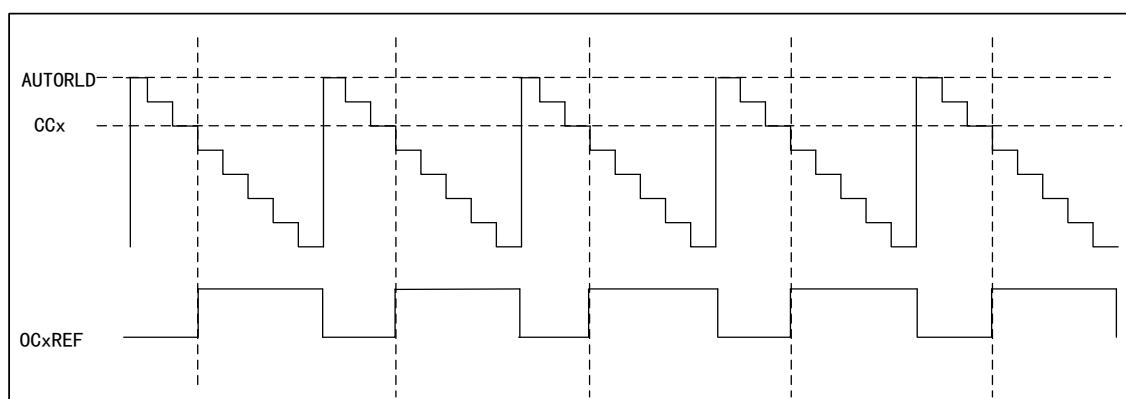
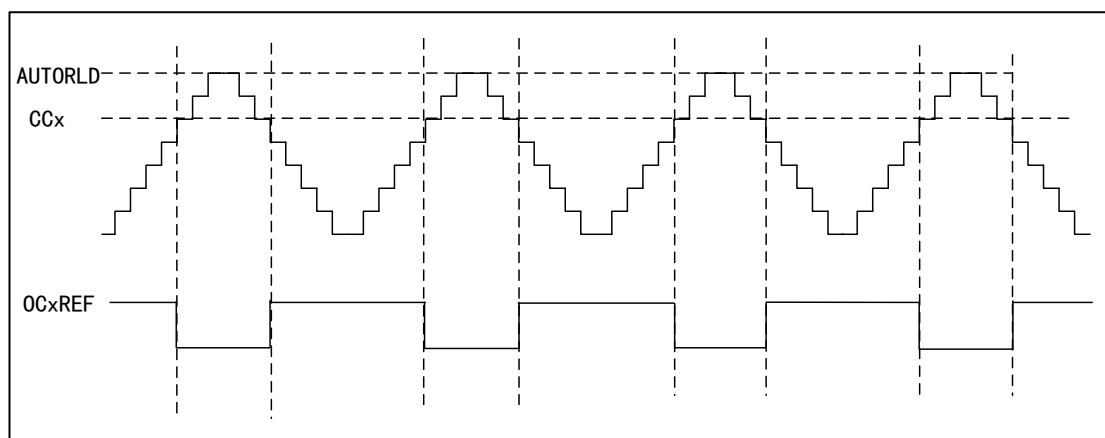


Figure 44 PWM1 Center-aligned Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 45 PWM2 Count-up Mode Timing Diagram

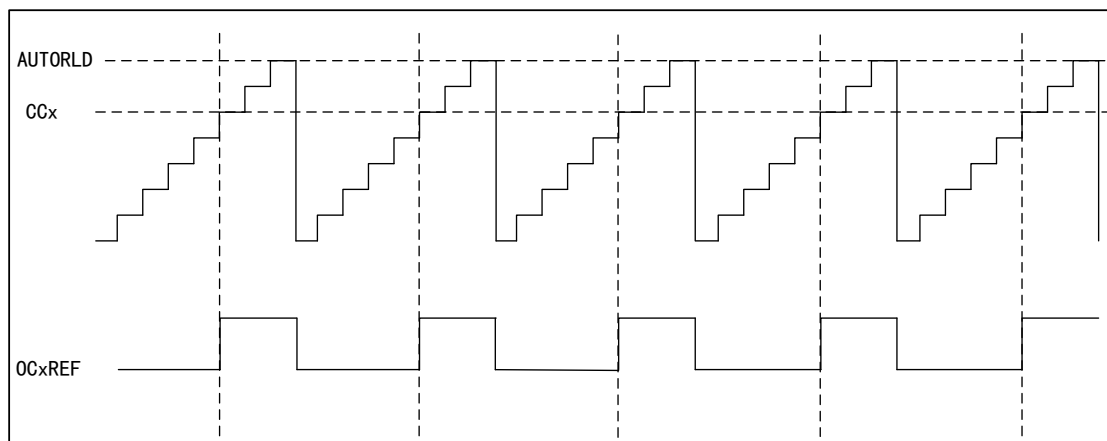


Figure 46 PWM2 Count-down Mode Timing Diagram

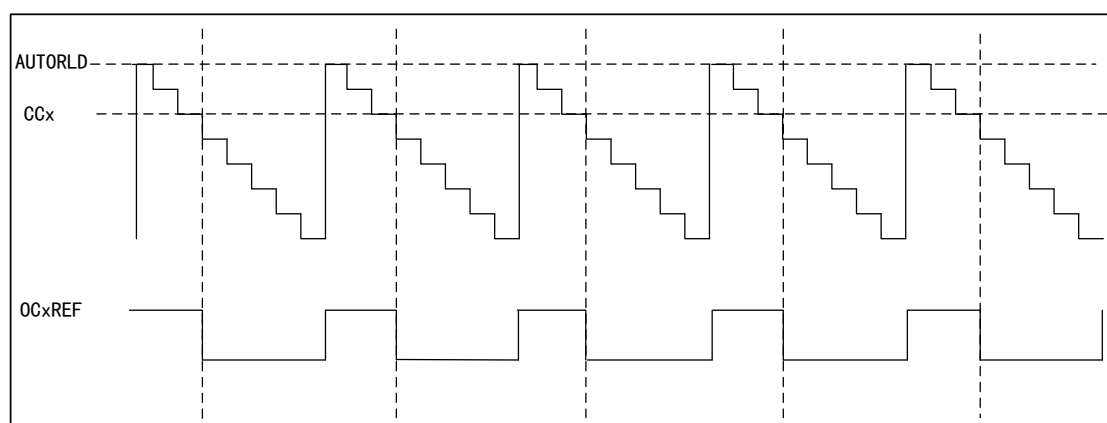
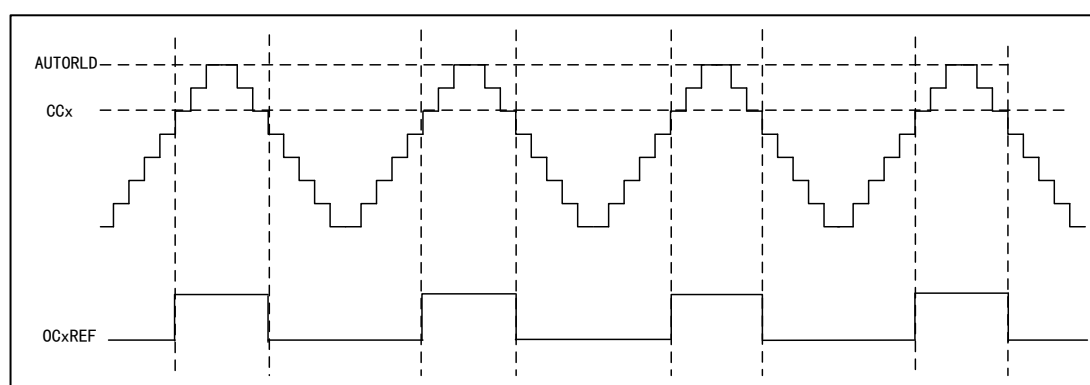


Figure 47 PWM2 Center-aligned Mode Timing Diagram



#### 15.4.6 PWM input mode

PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave

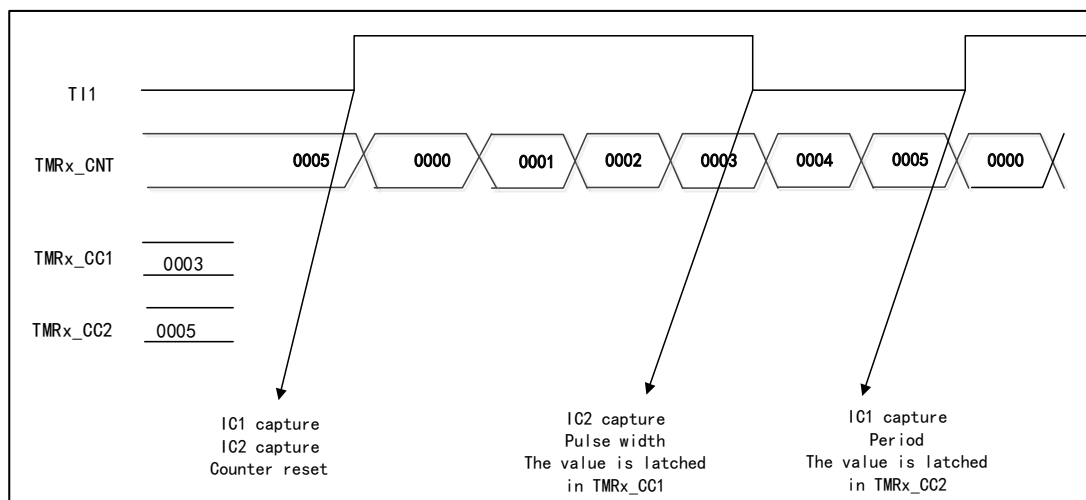


mode controller, input can be performed only through the channels TMRx\_CH1 and TMRx\_CH2, which need to occupy the capture registers of CH1 and CH2.

In PWM input mode, the PWM signal enters from TMRx\_CH1, and the signal will be divided into two channels, one can measure the period, and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMRx\_SMCTRL register)

Figure 48 PWM Input Mode Timing Diagram



#### 15.4.7 Single-pulse mode

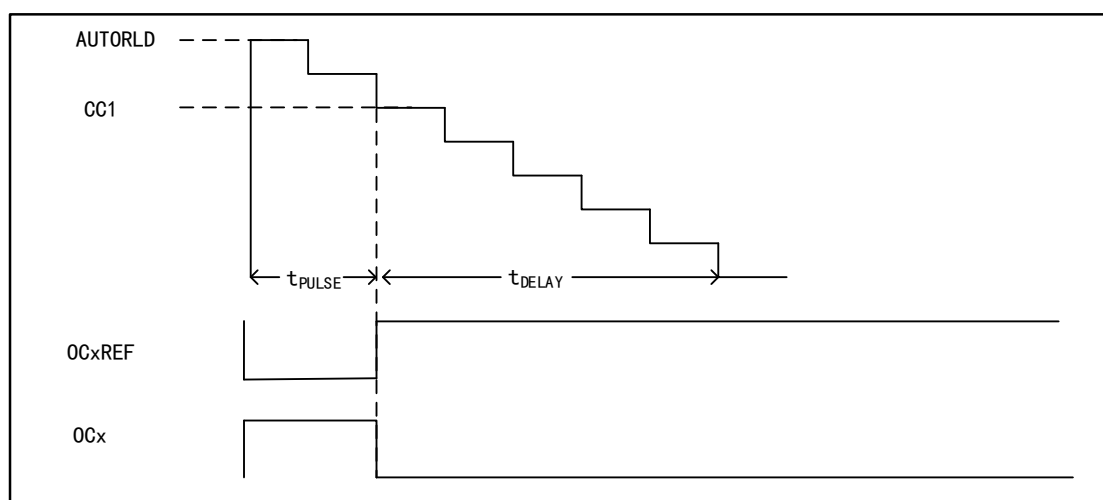
The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SP MEN bit of TMRx\_CTRL1 register, and select the single-pulse mode.

After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx\_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 49 Timing Diagram in Single-pulse Mode



#### 15.4.8 Forced output mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMRx\_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMRx\_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

#### 15.4.9 Encoder interface mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection method of encoder interface is as follows:

- By setting SMFSEL bit of TMRx\_SMCTRL register, set the counter to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- Select the polarity of TI1 and TI2 by setting the CC1POL and CC2POL bits of TMRx\_CCEN register.
- Select to filter or not by setting the IC1F and IC2F bits of TMRx\_CCM1 register.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2

- The counter will count up/down according to the jumping sequence of the input signal

- Set CNTDIR of control register TMRx\_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end)

The change mechanism of counter count direction is shown in the figure below:

Table 66 Relationship between Count Direction and Encoder

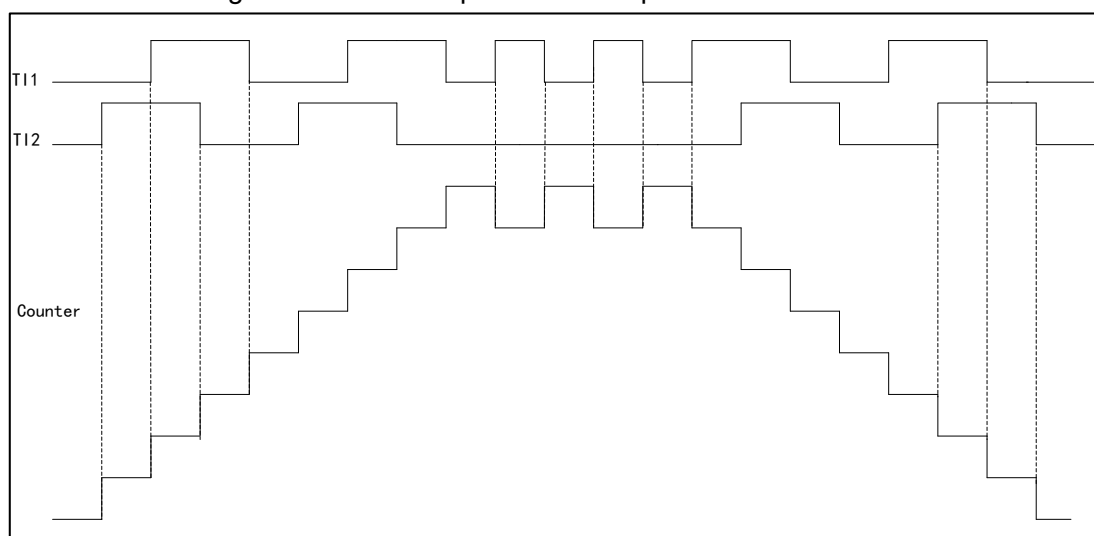
| Effective edge           |              | Count only in TI1 |            | Count only in TI2 |            | Count in both TI1 and TI2 |            |
|--------------------------|--------------|-------------------|------------|-------------------|------------|---------------------------|------------|
| Level of relative signal |              | High              | Low        | High              | Low        | High                      | Low        |
| TI1FP1                   | Rising edge  | Count down        | Count up   | —                 |            | Count down                | Count up   |
|                          | Falling edge | Count up          | Count down |                   |            | Count up                  | Count down |
| TI2FP2                   | Rising edge  | —                 |            | Count up          | Count down | Count up                  | Count down |
|                          | Falling edge |                   |            | Count down        | Count up   | Count down                | Count up   |

The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples:

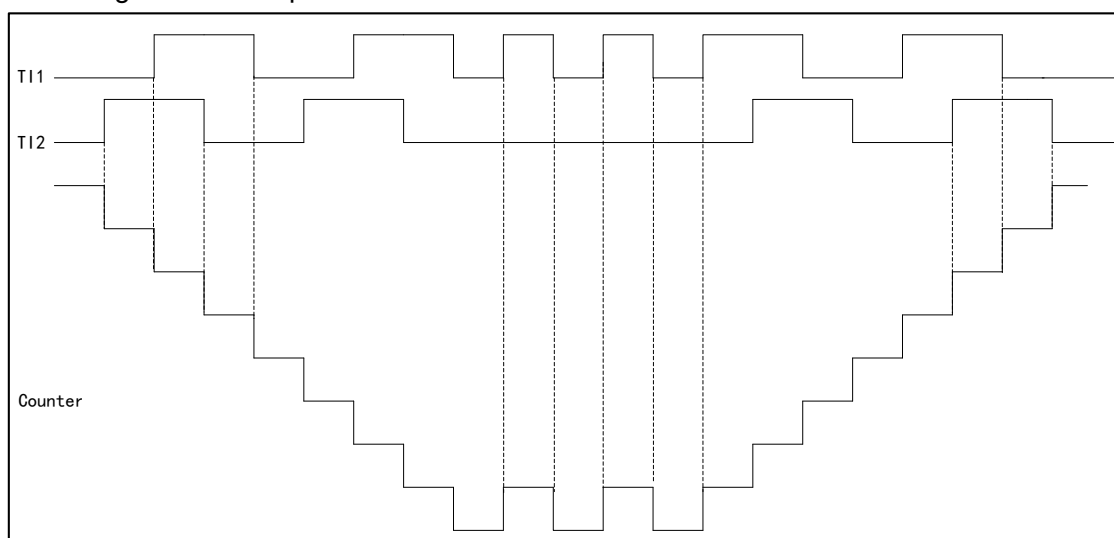
- IC1FP1 is mapped to TI1
- IC2FP2 is mapped to TI2
- Neither IC1FP1 nor IC2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

Figure 50 Counter Operation Example in Encoder Mode



For example, when TI1 is at low level, and TI2 is in rising edge state, the counter will count up.

Figure 51 Example of Encoder Interface Mode of IC1FP1 Reversed Phase



For example, when T11 is at low level, and the rising edge of T12 jumps, the counter will count down.

#### 15.4.10 Slave mode

TMRx timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMRx\_SMCTRL register can be set to select the mode

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

#### 15.4.11 Timer interconnection

See the chapter of "14.4.14 Timer Interconnection" for details.

#### 15.4.12 Interrupt and DMA request

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

#### 15.4.13 Debug mode

The TMR2/3/4/5 can be configured in debug mode and choose to stop or continue to work. It depends on the TMRx\_STS bit of DBGMCU\_APB1F register in DBGMCU module.

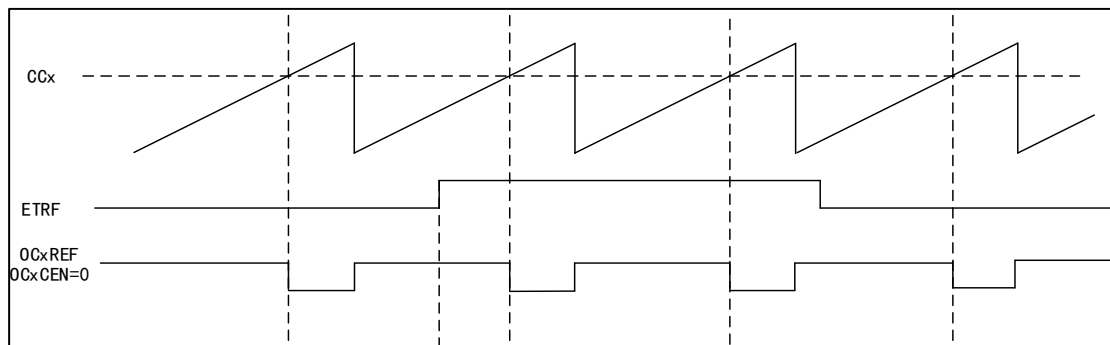
#### 15.4.14 Clear OCxREF signal when external events occur

This function is used for output compare and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCxCEN bit in capture/compare register TMRx\_CCMx is set to 1, and OCxREF signal will remain low until the next update event.

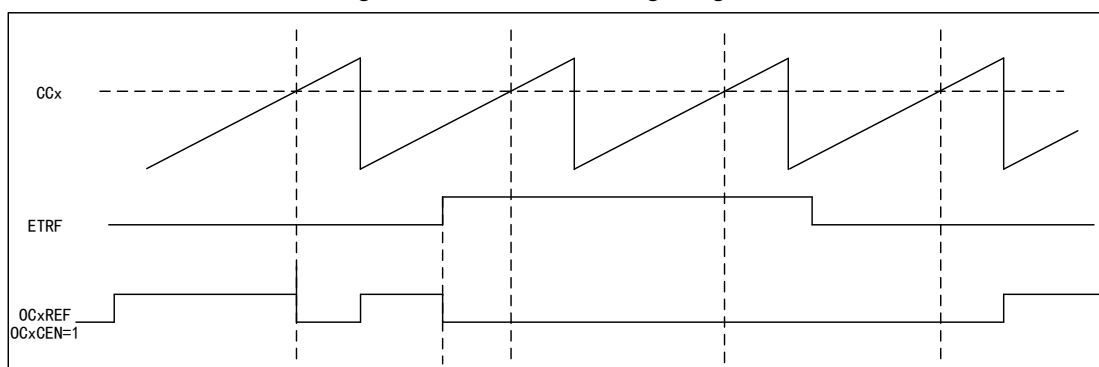
Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 52 OCxREF Timing Diagram



Set TMRx to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 53 OCxREF Timing Diagram



## 15.5 Register address mapping

In the following table, all registers of the general-purpose timer are mapped to a 16-bit addressable (address) space.

Table 67 General-purpose Timer Register Address Mapping

| Register name | Description                                 | Offset address |
|---------------|---------------------------------------------|----------------|
| TMRx_CTRL1    | Control register 1                          | 0x00           |
| TMRx_CTRL2    | Control register 2                          | 0x04           |
| TMRx_SMCTRL   | Slave mode control register                 | 0x08           |
| TMRx_DIEN     | DMA/Interrupt enable register               | 0x0C           |
| TMRx_STS      | State register                              | 0x10           |
| TMRx_CEG      | Control event generation register           | 0x14           |
| TMRx_CCM1     | Capture/Compare mode register 1             | 0x18           |
| TMRx_CCM2     | Capture/Compare mode register 2             | 0x1C           |
| TMRx_CCEN     | Enable the capture/compare channel register | 0x20           |
| TMRx_CNT      | Counter register                            | 0x24           |
| TMRx_PSC      | Prescaler register                          | 0x28           |
| TMRx_AUTORLD  | Auto reload register                        | 0x2C           |
| TMRx_CC1      | Channel 1 capture/compare register          | 0x34           |
| TMRx_CC2      | Channel 2 capture/compare register          | 0x38           |
| TMRx_CC3      | Channel 3 capture/compare register          | 0x3C           |
| TMRx_CC4      | Channel 4 capture/compare register          | 0x40           |
| TMRx_DCTRL    | DMA control register                        | 0x48           |
| TMRx_DMADDR   | DMA address register of continuous mode     | 0x4C           |
| TMR2_OPT      | TMR2 option register                        | 0x50           |
| TMR5_OPT      | TMR5 option register                        | 0x50           |

## 15.6 Register functional description

### 15.6.1 Control register 1 (TMRx\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CNTEN  | R/W | Counter Enable<br>0: Disable<br>1: Enable<br>When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.                                                                                                 |
| 1     | UD     | R/W | Update Disable<br>Update event can cause AUTORLD, PSC and CCx to generate the value of update setting.<br>0: Update event is allowed (UEV)<br>An update event can occur in any of the following situations:<br>The counter overruns/underruns;<br>Set UEG bit;<br>Update generated by slave mode controller.<br>1: Update event is disabled                                      |
| 2     | URSSEL | R/W | Update Request Source Select<br>If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit.<br>0: The counter overruns or underruns<br>Set UEG bit<br>Update generated by slave mode controller<br>1: The counter overruns or underruns                                    |
| 3     | SPMEN  | R/W | Single Pulse Mode Enable<br>When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed.<br>0: Disable<br>1: Enable                                                                                                     |
| 4     | CNTDIR | R/W | Counter Direction.<br>When the counter is configured in central alignment mode or encoder mode, the bit is read-only.<br>0: Count up<br>1: Count down                                                                                                                                                                                                                            |
| 6:5   | CAMSEL | R/W | Center Aligned Mode Select<br>In the center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different center-aligned modes affect the timing of setting the output compare interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the center-aligned mode.<br>00: Edge alignment mode |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 01: Center-aligned mode 1 (the output compare interrupt flag bit of output channel is set to 1 when counting down)<br>10: Center-aligned mode 2 (the output compare interrupt flag bit of output channel is set to 1 when counting up)<br>11: Center-aligned mode 3 (the output compare interrupt flag bit of output channel is set to 1 when counting up/down) |
| 7     | ARPEN    | R/W | Auto-reload Preload Enable<br>When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event.<br>0: Disable<br>1: Enable                                  |
| 9:8   | CLKDIV   | R/W | Clock Divide Factor<br>For the configuration of digital filter, CK_INT provides the clock, and the clock of the digital filter can be adjusted by setting this bit.<br>00: $t_{DTS}=t_{CK\_INT}$<br>01: $t_{DTS}=2 \times t_{CK\_INT}$<br>10: $t_{DTS}=4 \times t_{CK\_INT}$<br>11: Reserved                                                                    |
| 15:10 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                 |

### 15.6.2 Control register 2 (TMRx\_CTRL2)

Offset address: 0x04

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3     | CCDSEL   | R/W | Capture/compare DMA Select<br>0: Transmit DMA request of CCx when CCx event occurs<br>1: Transmit DMA request of CCx when an update event occurs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 6:4   | MMSEL    | R/W | Master Mode Signal Select<br>The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode.<br>000: Reset; the reset signal of master mode timer is used for TRGO<br>001: Enable; the counter enable signal of master mode timer is used for TRGO<br>010: Update; the update event of master mode timer is used for TRGO<br>011: Compare pulses; when the master mode timer captures/compares successfully ( $CCxIFLG=1$ ), a pulse signal is output for TRGO<br>100: Compare mode 1; OC1REF is used to trigger TRGO<br>101: Compare mode 2; OC2REF is used to trigger TRGO<br>110: Compare mode 3; OC3REF is used to trigger TRGO<br>111: Compare mode 4; OC4REF is used to trigger TRGO |



| Field | Name     | R/W | Description                                                                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7     | TI1SEL   | R/W | Timer Input 1 Selection<br>0: TMRx_CH1 pin is connected to TI1 input<br>1: TMRx_CH1, TMRx_CH2 and TMRx_CH3 pins are connected to TI1 input after exclusive |
| 15:8  | Reserved |     |                                                                                                                                                            |

### 15.6.3 Slave mode control register (TMRx\_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | SMFSEL   | R/W | Slave Mode Function Select<br>000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock.<br>001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2.<br>010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1.<br>011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2.<br>100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register.<br>101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period.<br>110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI.<br>111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work. |
| 3     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 6:4   | TRGSEL   | R/W | Trigger Input Signal Select<br>In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0.<br>000: Internal trigger ITR0<br>001: Internal trigger ITR1<br>010: Internal trigger ITR2<br>011: Internal trigger ITR3<br>100: Channel 1 input edge detector TIF_ED<br>101: Channel 1 post-filtering timer input TI1FP1<br>110: Channel 2 post-filtering timer input TI2FP2<br>111: External trigger input (ETRF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7     | MSMEN    | R/W | Master/slave Mode Enable<br>0: Invalid<br>1: Enable the master/slave mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:8  | ETFCFG | R/W | <p>External Trigger Filter Configure</p> <p>0000: Filter disabled, sampling by <math>f_{DTS}</math></p> <p>0001: DIV=1, N=2</p> <p>0010: DIV=1, N=4</p> <p>0011: DIV=1, N=8</p> <p>0100: DIV=2, N=6</p> <p>0101: DIV=2, N=8</p> <p>0110: DIV=4, N=6</p> <p>0111: DIV=4, N=8</p> <p>1000: DIV=8, N=6</p> <p>1001: DIV=8, N=8</p> <p>1010: DIV=16, N=5</p> <p>1011: DIV=16, N=6</p> <p>1100: DIV=16, N=8</p> <p>1101: DIV=32, N=5</p> <p>1110: DIV=32, N=6</p> <p>1111: DIV=32, N=8</p> <p>Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.</p> |
| 13:12 | ETPCFG | R/W | <p>External Trigger Prescaler Configure</p> <p>The ETR (external trigger input) signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMRxCLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division.</p> <p>00: The prescaler is disabled;</p> <p>01: ETR signal 2 divided frequency</p> <p>10: ETR signal 4 divided frequency</p> <p>11: ETR signal 8 divided frequency</p>                                                                                                                                     |
| 14    | ECEN   | R/W | <p>Enable external clock mode 2 (External Clock Enable Mode2)</p> <p>0: Disable</p> <p>1: Enable</p> <p>Setting ECEN bit has the same function as selecting external clock mode 1 to connect TRG1 to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.</p>                                                                                                                     |
| 15    | ETPOL  | R/W | <p>External Trigger Polarity Configure</p> <p>This bit decides whether the external trigger ETR is reversed.</p> <p>0: The external trigger ETR is not reversed, and the high level or rising edge is valid</p> <p>1: The external trigger ETR is reversed, and the low level or falling edge is valid</p>                                                                                                                                                                                                                                                                                                 |

Table 68 TMRx Internal Trigger Connection

| Slave timer | ITR0 (TS=000) | ITR1 (TS=001) | ITR2 (TS=010) | ITR3 (TS=011) |
|-------------|---------------|---------------|---------------|---------------|
| TMR2        | TMR1          | TMR8          | TMR3          | TMR4          |

|      |      |      |      |      |
|------|------|------|------|------|
| TMR3 | TMR1 | TMR2 | TMR5 | TMR4 |
| TMR4 | TMR1 | TMR2 | TMR3 | TMR8 |
| TMR5 | TMR2 | TMR3 | TMR4 | TMR8 |

#### 15.6.4 DMA/Interrupt enable register (TMRx\_DIEN)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name     | R/W | Description                                                            |
|-------|----------|-----|------------------------------------------------------------------------|
| 0     | UIEN     | R/W | Update interrupt Enable<br>0: Disable<br>1: Enable                     |
| 1     | CC1IEN   | R/W | Capture/Compare Channel1 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 2     | CC2IEN   | R/W | Capture/Compare Channel2 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 3     | CC3IEN   | R/W | Capture/Compare Channel3 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 4     | CC4IEN   | R/W | Capture/Compare Channel4 Interrupt Enable<br>0: Disable<br>1: Enable   |
| 5     | Reserved |     |                                                                        |
| 6     | TRGIEN   | R/W | Trigger interrupt Enable<br>0: Disable<br>1: Enable                    |
| 7     | Reserved |     |                                                                        |
| 8     | UDIEN    | R/W | Update DMA Request Enable<br>0: Disable<br>1: Enable                   |
| 9     | CC1DEN   | R/W | Capture/Compare Channel1 DMA Request Enable<br>0: Disable<br>1: Enable |
| 10    | CC2DEN   | R/W | Capture/Compare Channel2 DMA Request Enable<br>0: Disable<br>1: Enable |
| 11    | CC3DEN   | R/W | Capture/Compare Channel3 DMA Request Enable<br>0: Disable<br>1: Enable |
| 12    | CC4DEN   | R/W | Capture/Compare Channel4 DMA Request Enable<br>0: Disable<br>1: Enable |
| 13    | Reserved |     |                                                                        |

| Field | Name     | R/W | Description                                           |
|-------|----------|-----|-------------------------------------------------------|
| 14    | TRGDEN   | R/W | Trigger DMA Request Enable<br>0: Disable<br>1: Enable |
| 15    | Reserved |     |                                                       |

### 15.6.5 State register (TMRx\_STS)

Offset address: 0x10

Reset value: 0x0000

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UIFLG    | RC_W0 | Update Event Interrupt Generate Flag<br>0: Update event interrupt does not occur<br>1: Update event interrupt occurs<br>When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations:<br>(1) UD=0 on TMRx_CTRL1 register, and when the value overruns/underruns, an update event will be generated;<br>(2) URSEL=0 and UD=0 on TMRx_CTRL1 register, configure UG = 1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software;<br>(3) URSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event. |
| 1     | CC1IFLG  | RC_W0 | Capture/Compare Channel1 Interrupt Flag<br>When the capture/compare channel 1 is configured as output:<br>0: No matching occurred<br>1: The value of TMRx_CNT matches the value of TMRx_CC1<br>When the capture/compare channel 1 is configured as input:<br>0: Input capture did not occur<br>1: Input capture occurred<br>When capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.                                                                                                                                                                                                                                                                         |
| 2     | CC2IFLG  | RC_W0 | Capture/Compare Channel2 new Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3     | CC3IFLG  | RC_W0 | Capture/Compare Channel3 Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4     | CC4IFLG  | RC_W0 | Captuer/Compare Channel4 Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 5     | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 6     | TRGIFLG  | RC_W0 | Trigger Event Interrupt Generate Flag<br>0: Trigger event interrupt did not occur<br>1: Trigger event interrupt occurred<br>After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 8:7   | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                  |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9     | CC1RCFLG | RC_W0 | Capture/compare Channel1 Repetition Capture Flag<br>0: Repeat capture does not occur<br>1: Repeat capture occurs<br>The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture. |
| 10    | CC2RCFLG | RC_W0 | Capture/compare Channel2 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                    |
| 11    | CC3RCFLG | RC_W0 | Capture/compare Channel3 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                    |
| 12    | CC4RCFLG | RC_W0 | Capture/compare Channel4 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                    |
| 15:13 | Reserved |       |                                                                                                                                                                                                                                                                                                              |

### 15.6.6 Control event generation register (TMRx\_CEG)

Offset address: 0x14

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UEG      | W   | Update Event Generate<br>0: Invalid<br>1: Initialize the counter and generate the update event<br>This bit is set to 1 by software, and cleared by hardware.<br>Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared to 0.                                                                                                                                                                                          |
| 1     | CC1EG    | W   | Capture/Compare Channel1 Event Generation<br>0: Invalid<br>1: Capture/Compare event is generated<br>This bit is set to 1 by software and cleared automatically by hardware.<br>If Channel 1 is in output mode<br>When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated.<br>If Channel 1 is in input mode<br>The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1. |
| 2     | CC2EG    | W   | Capture/Compare Channel2 Event Generation<br>Refer to CC1EG description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 3     | CC3EG    | W   | Capture/Compare Channel3 Event Generation<br>Refer to CC1EG description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4     | CC4EG    | W   | Capture/Compare Channel4 Event Generation<br>Refer to CC1EG description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 5     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| Field | Name     | R/W | Description                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 6     | TEG      | W   | Trigger Event Generate<br>0: Invalid<br>1: Trigger event is generated<br>This bit is set to 1 by software and cleared automatically by hardware. |
| 15:7  | Reserved |     |                                                                                                                                                  |

### 15.6.7 Capture/Compare mode register 1 (TMRx\_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCx in the register describes the function of the channel in the output mode, and the ICx in the register describes the function of the channel in the input mode.

**Output compare mode:**

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL | R/W | Capture/Compare Channel 1 Selection<br>This bit defines the input/output direction and the selected input pin.<br>00: CC1 channel is output<br>01: CC1 channel is input, and IC1 is mapped on TI1<br>10: CC1 channel is input, and IC1 is mapped on TI2<br>11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).                                                                                                                                                |
| 2     | OC1FEN | R/W | Output Compare Channel1 Fast Enable<br>0: Disable<br>1: Enable<br>This bit is used to improve the response of the capture/compare output to the trigger input event.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3     | OC1PEN | R/W | Output Compare Channel1 Preload Enable<br>0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately.<br>1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated.<br>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain. |
| 6:4   | OC1MOD | R/W | Output Compare Channel1 Mode Configure<br>000: Freeze The output compare has no effect on OC1REF<br>001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level                                                                                                                                                                                                                                                                                                                           |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |        |     | <p>010: The output value is low when matching. When the value of the counter matches the value of the capture/compare register, OC1REF will be forced to be at low level</p> <p>011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF</p> <p>100: The output is forced to be low Force OC1REF to be at low level</p> <p>101: The output is forced to be high. Force OC1REF to be at high level</p> <p>110: PWM mode 1 (set to high when the counter value &lt; output compare value; otherwise, set to low)</p> <p>111: PWM mode 2 (set to high when the counter value &gt; output compare value; otherwise, set to low)</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output compare mode changes from freeze mode to PWM mode.</p> |
| 7     | OC1CEN | R/W | <p>Output Compare Channel1 Clear Enable</p> <p>0: OC1REF is unaffected by ETRF input.</p> <p>1: When high level of ETRF input is detected, OC1REF=0</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9:8   | CC2SEL | R/W | <p>Capture/Compare Channel2 Select</p> <p>This bit defines the input/output direction and the selected input pin.</p> <p>00: CC2 channel is output</p> <p>01: CC2 channel is input, and IC2 is mapped on TI2</p> <p>10: CC2 channel is input, and IC2 is mapped on TI1</p> <p>11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input</p> <p>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 10    | OC2FEN | R/W | Output Compare Channel2 Preload Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11    | OC2PEN | R/W | Output Compare Channel2 Buffer Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 14:12 | OC2MOD | R/W | Output Compare Channel1 Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15    | OC2CEN | R/W | Output Compare Channel2 Clear Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

#### Input capture mode:

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL | R/W | <p>Capture/Compare Channel 1 Select</p> <p>00: CC1 channel is output</p> <p>01: CC1 channel is input, and IC1 is mapped on TI1</p> <p>10: CC1 channel is input, and IC1 is mapped on TI2</p> <p>11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input</p> <p>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).</p> |
| 3:2   | IC1PSC | R/W | <p>Input Capture Channel 1 Prescaler Configure</p> <p>00: PSC=1</p> <p>01: PSC=2</p> <p>10: PSC=4</p> <p>11: PSC=8</p>                                                                                                                                                                                                                                                                              |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |        |     | PSC is prescaled factor, which triggers capture once every PSC events.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 7:4   | IC1F   | R/W | Input Capture Channel 1 Filter Configuration<br>0000: Filter disabled, sampling by $f_{DTS}$<br>0001: DIV=1, N=2<br>0010: DIV=1, N=4<br>0011: DIV=1, N=8<br>0100: DIV=2, N=6<br>0101: DIV=2, N=8<br>0110: DIV=4, N=6<br>0111: DIV=4, N=8<br>1000: DIV=8, N=6<br>1001: DIV=8, N=8<br>1010: DIV=16, N=5<br>1011: DIV=16, N=6<br>1100: DIV=16, N=8<br>1101: DIV=32, N=5<br>1110: DIV=32, N=6<br>1111: DIV=32, N=8<br>Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events. |
| 9:8   | CC2SEL | R/W | Capture/Compare Channel 2 Select<br>00: CC2 channel is output<br>01: CC2 channel is input, and IC2 is mapped on TI2<br>10: CC2 channel is input, and IC2 is mapped on TI1<br>11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0).                                                                                                                                                                    |
| 11:10 | IC2PSC | R/W | Input Capture Channel 2 Perscaler Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:12 | IC2F   | R/W | Input Capture Channel 2 Filter Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 15.6.8 Capture/Compare mode register 2 (TMRx\_CCM2)

Offset address: 0x1C

Reset value: 0x0000

Refer to the description of the above CCM1 register.

**Output compare mode:**

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC3SEL | R/W | Capture/Compare Channel 1 Selection<br>This bit defines the input/output direction and the selected input pin.<br>00: CC3 channel is output<br>01: CC3 channel is input, and IC3 is mapped on TI3<br>10: CC3 channel is input, and IC3 is mapped on TI4<br>11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC3EN=0). |



| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | OC3FEN | R/W | Output Compare Channel3 Fast Enable<br>0: Disable<br>1: Enable<br>This bit is used to improve the response of the capture/compare output to the trigger input event.                                                                                                                                                                                                                                                                                   |
| 3     | OC3PEN | R/W | Output Compare Channel3 Preload Enable                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 6:4   | OC3MOD | R/W | Output Compare Channel3 Mode Configure                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7     | OC3CEN | R/W | Output Compare Channel3 Clear Enable<br>0: OC3REF is unaffected by ETRF input.<br>1: When high level of ETRF input is detected, OC1REF=0                                                                                                                                                                                                                                                                                                               |
| 9:8   | CC4SEL | R/W | Capture/Compare Channel 4 Selection<br>This bit defines the input/output direction and the selected input pin.<br>00: CC4 channel is output<br>01: CC4 channel is input, and IC4 is mapped on TI4<br>10: CC4 channel is input, and IC4 is mapped on TI3<br>11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC4EN=0). |
| 10    | OC4FEN | R/W | Output Compare Channel4 Preload Enable                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11    | OC4PEN | R/W | Output Compare Channel4 Buffer Enable                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 14:12 | OC4MOD | R/W | Output Compare Channel4 Mode Configure                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15    | OC4CEN | R/W | Output Compare Channel4 Clear Enable                                                                                                                                                                                                                                                                                                                                                                                                                   |

#### Input capture mode:

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC3SEL | R/W | Capture/Compare Channel 3 Select<br>00: CC3 channel is output<br>01: CC3 channel is input, and IC3 is mapped on TI3<br>10: CC3 channel is input, and IC3 is mapped on TI4<br>11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC3EN=0). |
| 3:2   | IC3PSC | R/W | Input Capture Channel 3 Perscaler Configuration<br>00: PSC=1<br>01: PSC=2<br>10: PSC=4<br>11: PSC=8<br>PSC is prescaled factor, which triggers capture once every PSC events.                                                                                                                                                                                            |
| 7:4   | IC3F   | R/W | Input Capture Channel 3 Filter Configuration                                                                                                                                                                                                                                                                                                                             |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8   | CC4SEL | R/W | Capture/Compare Channel 4 Select<br>00: CC4 channel is output<br>01: CC4 channel is input, and IC4 is mapped on TI4<br>10: CC4 channel is input, and IC4 is mapped on TI3<br>11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC4EN=0). |
| 11:10 | IC4PSC | R/W | Input Capture Channel 4 Perscaler Configuration                                                                                                                                                                                                                                                                                                                          |
| 15:12 | IC4F   | R/W | Input Capture Channel 4 Filter Configuration                                                                                                                                                                                                                                                                                                                             |

### 15.6.9 Enable capture/compare channel register (TMRx\_CCEN)

Offset address: 0x20

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CC1EN    | R/W | Capture/Compare Channel1 Output Enable<br>When the capture/compare channel 1 is configured as output:<br>0: Output is disabled<br>1: Output is enabled<br>When the capture/compare channel 1 is configured as input:<br>This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register<br>0: Capture is disabled<br>1: Capture is enabled                                                                                                                                        |
| 1     | CC1POL   | R/W | Capture/Compare Channel1 Output Polarity Configure<br>When CC1 channel is configured as output:<br>0: OC1 high level is valid<br>1: OC1 low level is valid<br>When CC1 channel is configured as input:<br>0: Phase not reversed: capture at the rising edge of IC1; phase not reversed when IC1 is used as external trigger.<br>1: Phase reversed, capture at the falling edge of ICC1; phase reversed when IC1 is used as external trigger.<br>Note: When the protection level is 2 or 3, this bit cannot be modified |
| 3:2   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4     | CC2EN    | R/W | Capture/Compare Channel2 Output Enable<br>Refer to CCEN_CC1EN                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | CC2POL   | R/W | Capture/Compare Channel2 Output Polarity Configure<br>Refer to CCEN_CC1POL                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 7:6   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 8     | CC3EN    | R/W | Capture/Compare Channel3 Output Enable<br>Refer to CCEN_CC1EN                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | CC3POL   | R/W | Capture/Compare Channel3 Output Polarity Configure<br>Refer to CCEN_CC1POL                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| Field | Name     | R/W | Description                                                      |
|-------|----------|-----|------------------------------------------------------------------|
| 11:10 | Reserved |     |                                                                  |
| 12    | CC4EN    | R/W | Capture/Compare Channel4 Output Enable<br>Refer to CCEN_CC1EN    |
| 13    | CC4POL   | R/W | Capture/Compare Channel4 Output Polarity<br>Refer to CCEN_CC1POL |
| 15:14 | Reserved |     |                                                                  |

Table 69 Output Control Bit of Standard OCx Channel

| CCxEN bit | OCx output state                     |
|-----------|--------------------------------------|
| 0         | Output is disabled (OCx=0, OCx_EN=0) |
| 1         | OCx=OCxREF+polarity, OCx_EN=1        |

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

#### 15.6.10 Counter register (TMRx\_CNT)

Offset address: 0x24

Reset value: 0x0000

| Field | Name | R/W | Description   |
|-------|------|-----|---------------|
| 31:0  | CNT  | R/W | Counter Value |

#### 15.6.11 Prescaler register (TMRx\_PSC)

Offset address: 0x28

Reset value: 0x0000

| Field | Name | R/W | Description                                                                         |
|-------|------|-----|-------------------------------------------------------------------------------------|
| 15:0  | PSC  | R/W | Prescaler Value<br>Clock frequency of counter (CK_CNT)=f <sub>CK_PSC</sub> /(PSC+1) |

#### 15.6.12 Auto reload register (TMRx\_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF FFFF

| Field | Name    | R/W | Description                                                                              |
|-------|---------|-----|------------------------------------------------------------------------------------------|
| 31:0  | AUTORLD | R/W | Auto Reload Value<br>When the value of auto reload is empty, the counter will not count. |

#### 15.6.13 Channel 1 capture/compare register (TMRx\_CC1)

Offset address: 0x34

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | CC1  | R/W | <p>Capture/Compare Channel 1 Value</p> <p>Capture/Compare Channel 1 configured in input mode:<br/>CC1 contains counter value from the last input capture event of channel 1.</p> <p>Capture/Compare Channel 1 configured in output mode:<br/>CC1 contains the current value loaded into the capture/compare register.</p> <p>The value of the capture/compare channel 1, CC1, is compared with the counter value CNT. An output signal is generated on OC1.</p> <p>When output compare preload is disabled (OC1PEN=0 in the TMRx_CCM1 register), the written value immediately affects the output compare result.</p> <p>When output compare preload is enabled (OC1PEN=1 in the TMRx_CCM1 register), the written value affects the output compare result at the update event.</p> |

#### 15.6.14 Channel 2 capture/compare register (TMRx\_CC2)

Offset address: 0x38

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                     |
|-------|------|-----|-----------------------------------------------------------------|
| 31:0  | CC2  | R/W | <p>Capture/Compare Channel 2 Value</p> <p>Refer to TMRx_CC1</p> |

#### 15.6.15 Channel 3 capture/compare register (TMRx\_CC3)

Offset address: 0x3C

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                     |
|-------|------|-----|-----------------------------------------------------------------|
| 31:0  | CC3  | R/W | <p>Capture/Compare Channel 3 Value</p> <p>Refer to TMRx_CC1</p> |

#### 15.6.16 Channel 4 capture/compare register (TMRx\_CC4)

Offset address: 0x40

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                     |
|-------|------|-----|-----------------------------------------------------------------|
| 31:0  | CC4  | R/W | <p>Capture/Compare Channel 4 Value</p> <p>Refer to TMRx_CC1</p> |

#### 15.6.17 DMA control software (TMRx\_DCTRL)

Offset address: 0x48

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                             |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | DBADDR | R/W | <p>DMA Base Address Setup</p> <p>These bits define the base address of DMA in continuous mode (when reading or writing TMRx_DMADDR register), and DBADDR is defined as the offset from the address of TMRx_CTRL1 register:</p> <p>00000: TMRx_CTRL1</p> <p>00001: TMRx_CTRL2</p> <p>00010: TMRx_SMCTRL</p> <p>.....</p> |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 12:8  | DBLEN    | R/W | <p>DMA Burst Transfer Length Setup</p> <p>These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits.</p> <p>When reading/writing TMRx_DMADDR register, the timer will conduct a continuous transmission;</p> <p>00000: Transmission once</p> <p>00001: Transmission twice</p> <p>00010: Transmission for three times</p> <p>.....</p> <p>10001: Transmission for 18 times</p> <p>The transmission address formula is as follows:</p> <p>Transmission address=TMRx_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN</p> <p>For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMRx_CTRL1 means the address of the data to be written/read,</p> <p>Data transmission will occur to: TMRx_CTRL1 address + seven registers starting from DBADDR.</p> <p>The data transmission will change according to different DMA data length:</p> <ol style="list-style-type: none"> <li>1) When the transmission data is set to 16 bits, the data will be transmitted to seven registers</li> <li>2) When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.</li> </ol> |
| 15:13 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

### 15.6.18 DMA address register of continuous mode (TMRx\_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | DMADDR | R/W | <p>DMA Register for Burst Transfer</p> <p>Read or write operation access of TMRx_DMADDR register may lead to access operation of the register in the following address:</p> <p>TMRx_CTRL1 address + (DBADDR+DMA index) ×4</p> <p>Wherein:</p> <p>"TMRx_CTRL1 address" is the address of control register 1 (TMRx_CTRL1);</p> <p>"DBADDR" is the base address defined in TMRx_DCTRL register;</p> <p>"DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMRx_DCTRL register.</p> |

### 15.6.19 TMR2 option register (MR2\_OPT)

Offset address: 0x50

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                          |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:0   | Reserved |     |                                                                                                                                                                                                                                                      |
| 11:10 | RMPSEL   | R/W | Timer2 Internal Trigger 1 Remap Select<br>00: TMR8_TRGOUT<br>01: PTP trigger output is connected to TMR2_ITR1<br>10: OTG_FS1 SOF is connected to TMR2_ITR1 input<br>11: OTG_FS2 SOF is connected to TMR2_ITR1 input<br>Note: Clear through software. |
| 15:12 | Reserved |     |                                                                                                                                                                                                                                                      |

### 15.6.20 TMR5 option register (TMR5\_OPT)

Offset address: 0x50

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                     |
| 7:6   | RMPSEL   | R/W | Timer5 Channel4 Input Remap Select<br>00: TMR5 Channel 4 is connected to GPIO<br>01: LSICLK internal clock is connected to TMR5_CH 4 input for calibration<br>10: LSECLK internal clock is connected to TMR5_CH4 input for calibration<br>11: RTC wake-up interrupt is connected to TMR5_CH4 input for calibration<br>Note: Clear through software. |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                     |

## 16 General-purpose Timer (TMR9/10/11/12/13/14)

### 16.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform. It includes a 16-bit auto reload counter (for count-up).

### 16.2 Main characteristics of TMR9/12

- (1) Timebase unit
  - Counter: 16-bit counter, count-up
  - Prescaler: 16-bit programmable prescaler
  - Auto reloading function
- (2) Clock source
  - Internal clock
- (3) Timer function
  - Input capture
  - Output compare
  - PWM output mode
  - Forced output mode
  - Single-pulse mode output
- (4) Master/Slave mode controller of timer
  - Timers can be synchronized and cascaded
  - Support multiple slave modes and synchronization signals
- (5) Interrupt event
  - Update event (counter overrun, counter initialization)
  - Trigger event (counter start, stop, internal/external trigger)
  - Input capture
  - Output compare

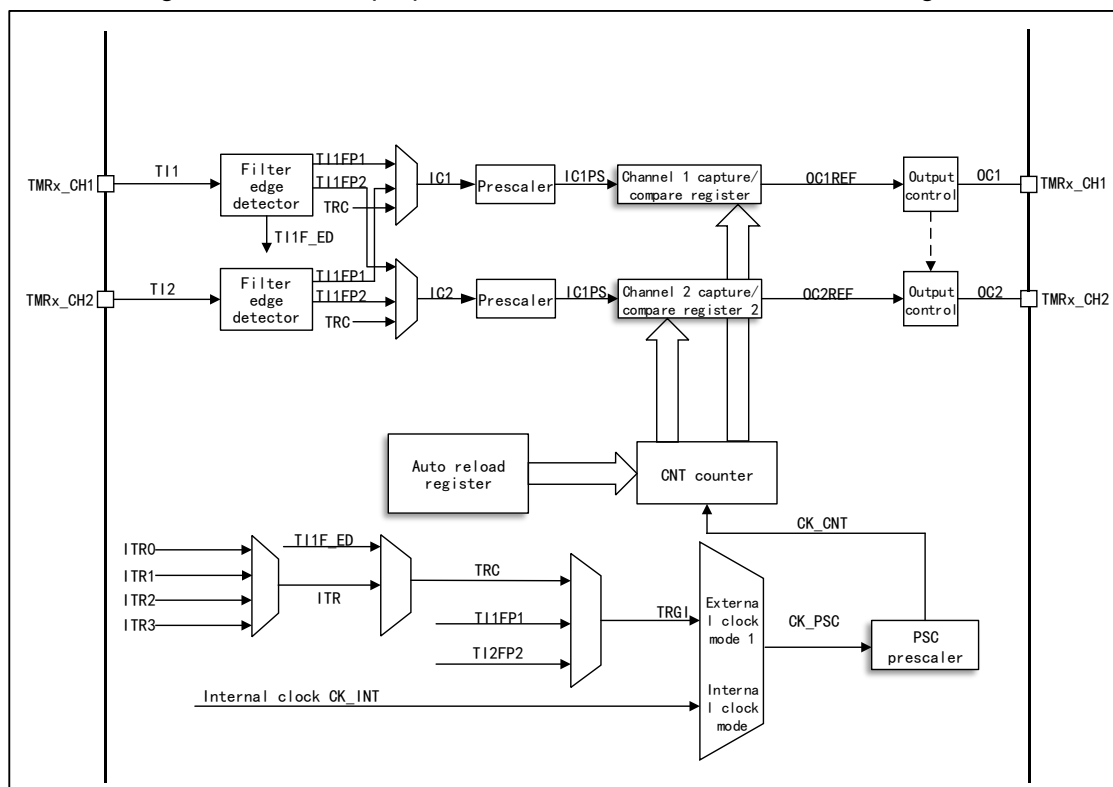
### 16.3 Main characteristics of TMR10/11/13/14

- (1) Timebase unit
  - Counter: 16-bit counter, count-up
  - Prescaler: 16-bit programmable prescaler
  - Auto reloading function
- (2) Clock source
  - Internal clock

- (3) Timer function
  - Input capture
  - Output compare
  - PWM output mode
  - Forced output mode
  - Single-pulse mode output
- (4) Interrupt and DMA request event
  - Update event (counter overrun, counter initialization)
  - Input capture
  - Output compare

## 16.4 TMR9/12 structure block diagram

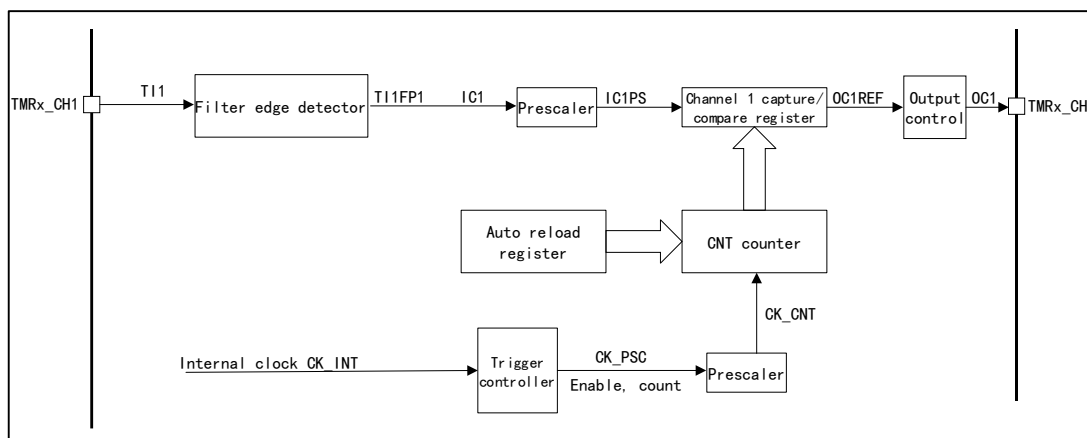
Figure 54 General-purpose Timer TMR9/12 Structure Block Diagram





## 16.5 TMR10/11/13/14 structure block diagram

Figure 55 General-purpose Timer TMR10/11/13/14 Structure Block Diagram



## 16.6 Functional description

### 16.6.1 Clock source

#### Internal clock

It is TMRx\_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK\_PSC of the prescaler is driven by the internal clock CK\_INT.

### 16.6.2 Timebase unit

The time base unit in the general-purpose timer contains three registers

- 16-bit counter register (CNT)
- 16-bit auto reload register (AUTORLD)
- 16-bit prescaler register (PSC)

#### Counter CNT

The counter in the general-purpose timer only has count-up mode.

#### Count-up mode

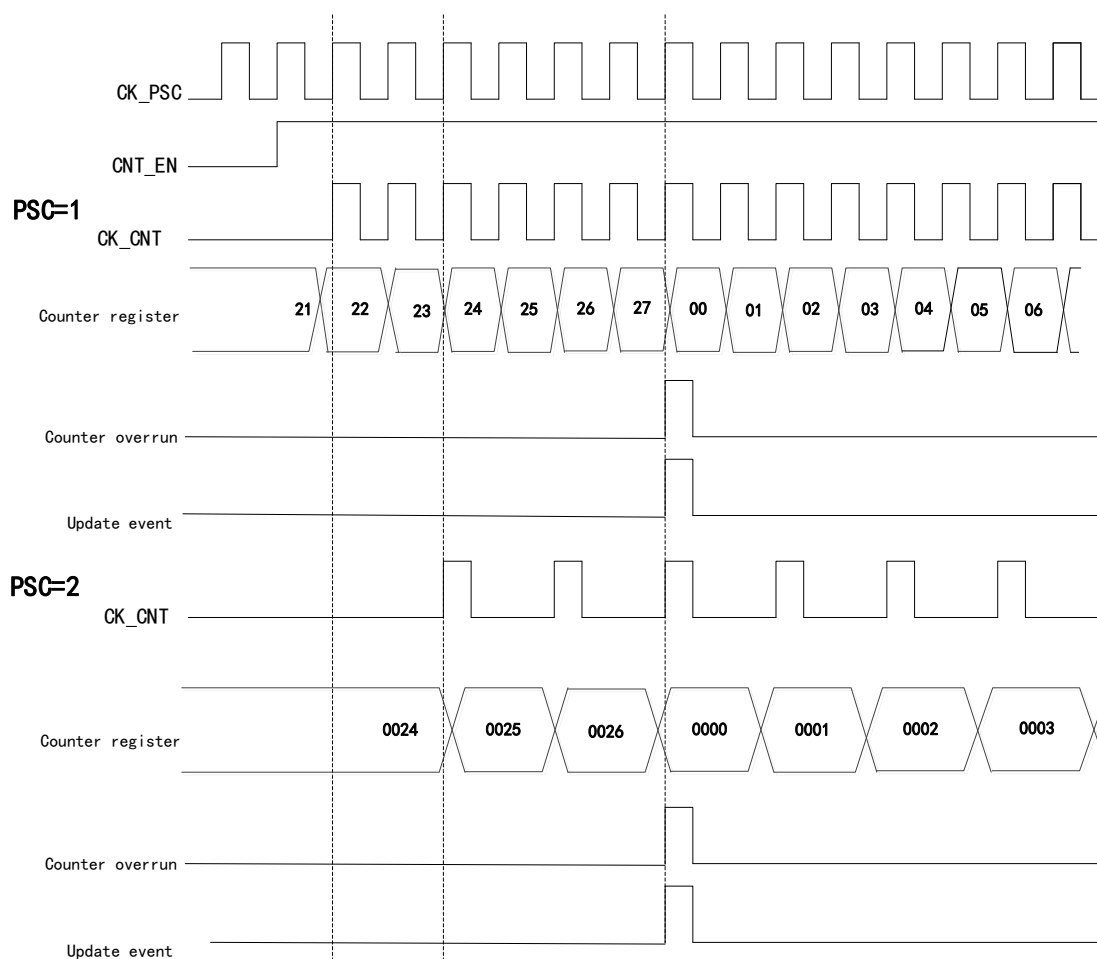
When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx\_CNT) is equal to the value of the auto reload (TMRx\_AUTORLD), the counter will start to count again from 0. A count-up overrun event will be generated, and the value of the auto reload (TMRx\_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the

auto reload register and the prescaler register will be updated. The update event can be disabled by UD bit of configuration control register TMRx\_CTRL1.

The figure below is timing diagram when division factor is 1 or 2 in count-up mode.

Figure 56 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



## Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx\_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

### 16.6.3 Input capture

#### Input capture channel

The general-purpose timer has four independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

### **Input capture application**

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMRx\_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx\_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

### **16.6.4 Output compare**

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM mode 1 and PWM mode 2, which are configured by OCxMOD bit in TMRx\_CCMx register and can control the waveform of output signal in output compare mode.

### **Output compare application**

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx\_CCMx register and the CCxPOL bit in the output polarity TMRx\_CCEN register.

When CCxIFLG=1 in TMRx\_STS register, if CCxIEN=1 in TMRx\_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx\_CTRL2 register, DMA

request will be generated.

### 16.6.5 PWM input mode (only applicable to TMR9/12)

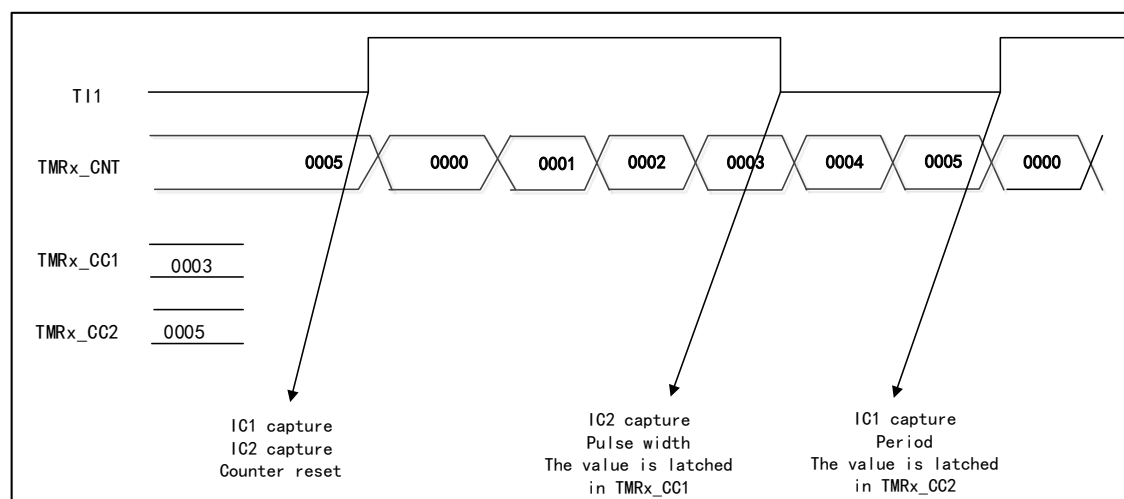
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMRx\_CH1 and TMRx\_CH2, which need to occupy the capture registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMRx\_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMRx\_SMCTRL register).

Figure 57 PWM Input Mode Timing Diagram



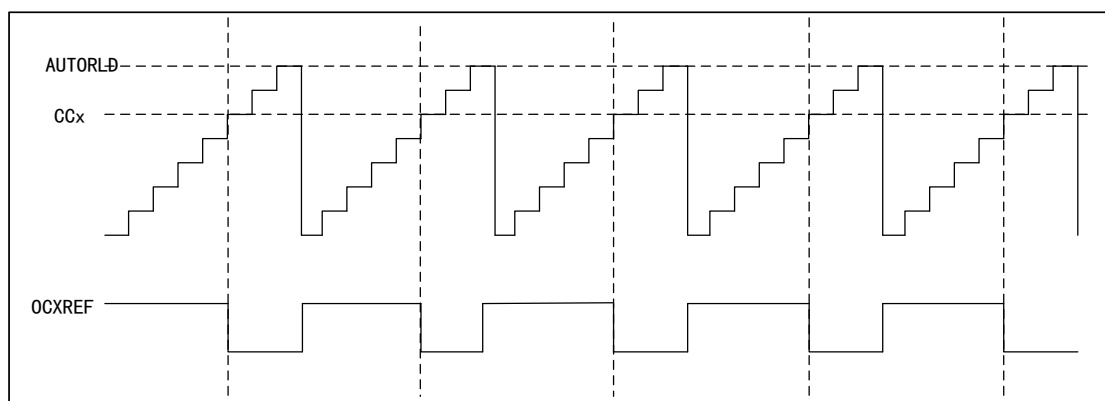
### 16.6.6 PWM output mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 can only count-up; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORD=7.

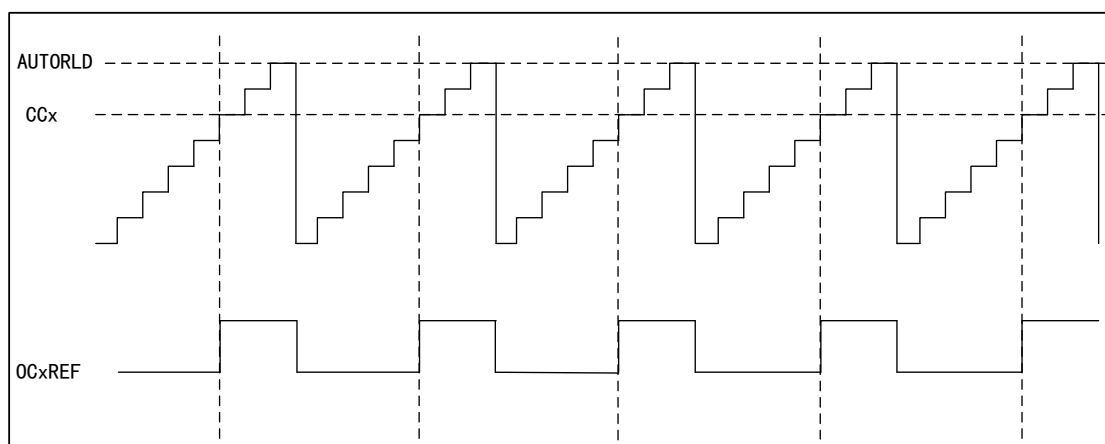
Figure 458 PWM1 Count-up Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7.

Figure 59 PWM2 Count-up Mode Timing Diagram



### 16.6.7 Single-pulse mode

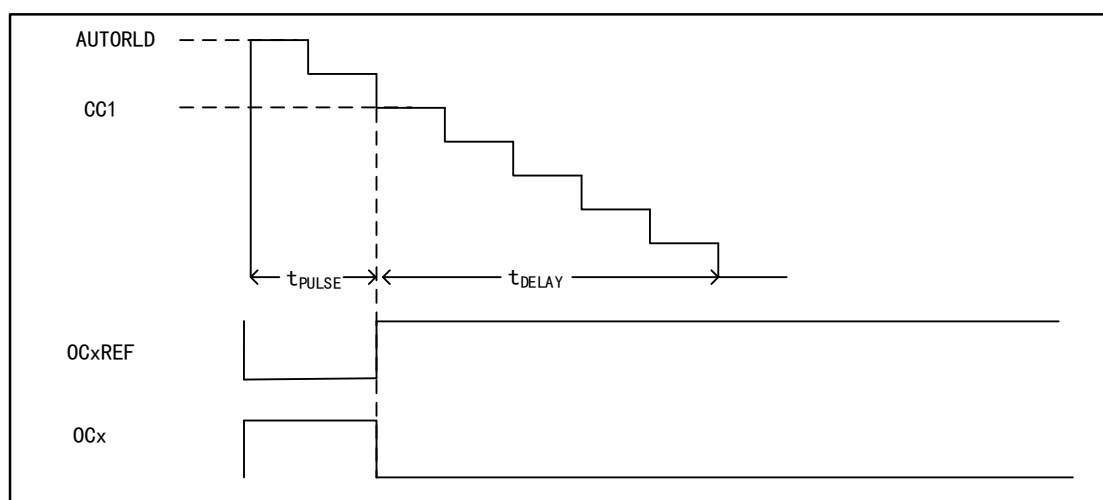
The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SP MEN bit of TMRx\_CTRL1 register, and select the single-pulse mode.

After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx\_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 60 Single-pulse Mode Timing Diagram



### 16.6.8 Forced output mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMRx\_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMRx\_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

### 16.6.9 Debug mode

The TMR9/10/11/12/13/14 can be configured in debug mode and choose to stop or continue to work. It depends on the TMRx\_STS bit of DBGMCU\_APB1F register or DBGMCU\_APB2F register in DBGMCU module.

## 16.7 TMR9/12 register address mapping

In the following table, all registers of TMR9/12 are mapped to a 16-bit addressable (address) space.

Table 70 TMR9/12 Register Address Mapping

| Register name | Description                       | Offset address |
|---------------|-----------------------------------|----------------|
| TMRx_CTRL1    | Control register 1                | 0x00           |
| Reserve       | -                                 | 0x04           |
| TMRx_SMCTRL   | Slave mode control register       | 0x08           |
| TMRx_DIEN     | DMA/Interrupt enable register     | 0x0C           |
| TMRx_STS      | State register                    | 0x10           |
| TMRx_CEG      | Control event generation register | 0x14           |

| Register name | Description                        | Offset address |
|---------------|------------------------------------|----------------|
| TMRx_CCM1     | Capture/Compare mode register 1    | 0x18           |
| TMRx_CCEN     | Capture/Compare enable register    | 0x20           |
| TMRx_CNT      | Counter register                   | 0x24           |
| TMRx_PSC      | Prescaler register                 | 0x28           |
| TMRx_AUTORLD  | Auto reload register               | 0x2C           |
| TMRx_CC1      | Channel 1 capture/compare register | 0x34           |
| TMRx_CC2      | Channel 2 capture/compare register | 0x38           |

## 16.8 TMR9/12 register functional description

### 16.8.1 Control register 1 (TMRx\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CNTEN    | R/W | Counter Enable<br>0: Disable<br>1: Enable<br>When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.    |
| 1     | UD       | R/W | Update Disable<br>Update event can cause AUTORLD, PSC and CCx to generate the value of update setting.<br>0: Update event is allowed (UEV)<br>An update event can occur in any of the following situations:<br>The counter overruns;<br>Set UEG bit.<br>1: Update event is disabled |
| 2     | URSSEL   | R/W | Update Request Source Select<br>If interrupt is enabled, the update event can generate update interrupt. Different update request sources can be selected through this bit.<br>0: The counter overruns;<br>Set UEG bit.<br>1: The counter overruns                                  |
| 3     | SPMEN    | R/W | Single Pulse Mode Enable<br>When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed.<br>0: Disable<br>1: Enable        |
| 6:4   | Reserved |     |                                                                                                                                                                                                                                                                                     |
| 7     | ARPEN    | R/W | Auto-reload Preload Enable                                                                                                                                                                                                                                                          |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event.<br>0: Disable<br>1: Enable |
| 9:8   | CLKDIV   | R/W | Clock Divide Factor<br>For the configuration of digital filter, CK_INT provides the clock, and the clock of the digital filter can be adjusted by setting this bit.<br>00: $t_{DTS}=t_{CK\_INT}$<br>01: $t_{DTS}=2\times t_{CK\_INT}$<br>10: $t_{DTS}=4\times t_{CK\_INT}$<br>11: Reserved       |
| 15:10 | Reserved |     |                                                                                                                                                                                                                                                                                                  |

### 16.8.2 Slave mode control register (TMRx\_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | SMFSEL   | R/W | Slave Mode Function Select<br>000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock.<br>001: Reserved<br>010: Reserved<br>011: Reserved<br>100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register.<br>101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period.<br>110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI.<br>111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work. |
| 3     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 6:4   | TRGSEL   | R/W | Trigger Input Signal Select<br>In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0.<br>000: Internal trigger ITR0<br>001: Internal trigger ITR1<br>010: Internal trigger ITR2<br>011: Internal trigger ITR3<br>100: Channel 1 input edge detector TIF_ED<br>101: Channel 1 post-filtering timer input TI1FP1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |



| Field | Name     | R/W | Description                                                               |
|-------|----------|-----|---------------------------------------------------------------------------|
|       |          |     | 110: Channel 2 post-filtering timer input TI2FP2<br>111: Reserved         |
| 7     | MSMEN    | R/W | Master/slave Mode Enable<br>0: Invalid<br>1: Enable the master/slave mode |
| 15:8  | Reserved |     |                                                                           |

Table 71 TMRx Internal Trigger Connection

| Slaver timer | ITR0 (TS=000) | ITR1 (TS=001) | ITR2 (TS=010) | ITR3 (TS=011) |
|--------------|---------------|---------------|---------------|---------------|
| TMR2         | TMR1          | TMR8          | TMR3          | TMR4          |
| TMR3         | TMR1          | TMR2          | TMR5          | TMR4          |
| TMR4         | TMR1          | TMR2          | TMR3          | TMR8          |
| TMR5         | TMR2          | TMR3          | TMR4          | TMR8          |
| TMR9         | TMR2          | TMR3          | TMR10         | TMR11         |
| TMR12        | TMR4          | TMR5          | TMR13         | TMR14         |

### 16.8.3 DMA/Interrupt enable register (TMRx\_DIEN)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name     | R/W | Description                                                          |
|-------|----------|-----|----------------------------------------------------------------------|
| 0     | UIEN     | R/W | Update interrupt Enable<br>0: Disable<br>1: Enable                   |
| 1     | CC1IEN   | R/W | Capture/Compare Channel1 Interrupt Enable<br>0: Disable<br>1: Enable |
| 2     | CC2IEN   | R/W | Capture/Compare Channel2 Interrupt Enable<br>0: Disable<br>1: Enable |
| 5:3   | Reserved |     |                                                                      |
| 6     | TRGIEN   | R/W | Trigger interrupt Enable<br>0: Disable<br>1: Enable                  |
| 15:7  | Reserved |     |                                                                      |

### 16.8.4 State register (TMRx\_STS)

Offset address: 0x10

Reset value: 0x0000

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UIFLG    | RC_W0 | Update Event Interrupt Generate Flag<br>0: Update event interrupt does not occur<br>1: Update event interrupt occurs<br>When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations:<br>(1) UD=0 on TMRx_CTRL1 register, and when overruns, an update event will be generated;<br>(2) URSEL=0 and UD=0 on TMRx_CTRL1 register, configure UG = 1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software;<br>(3) URSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event. |
| 1     | CC1IFLG  | RC_W0 | Capture/Compare Channel1 Interrupt Flag<br>When the capture/compare channel 1 is configured as output:<br>0: No matching occurred<br>1: The value of TMRx_CNT matches the value of TMRx_CC1<br>When the capture/compare channel 1 is configured as input:<br>0: Input capture did not occur<br>1: Input capture occurred<br>When a capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.                                                                                                                                                                                                                                                   |
| 2     | CC2IFLG  | RC_W0 | Capture/Compare Channel2 new Interrupt Flag<br>Refer to STS_CC1IFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5:3   | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 6     | TRGIFLG  | RC_W0 | Trigger Event Interrupt Generate Flag<br>0: Trigger event interrupt did not occur<br>1: Trigger event interrupt occurred<br>After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8:7   | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | CC1RCFLG | RC_W0 | Capture/compare Channel1 Repetition Capture Flag<br>0: Repeat capture does not occur<br>1: Repeat capture occurs<br>The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.                                                                                                                                                                                                                                                                                                                                                                                                             |
| 10    | CC2RCFLG | RC_W0 | Capture/compare Channel2 Repetition Capture Flag<br>Refer to STS_CC1RCFLG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:11 | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### 16.8.5 Control event generation register (TMRx\_CEG)

Offset address: 0x14

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UEG      | W   | Update Event Generate<br>0: Invalid<br>1: Initialize the counter and generate the update event<br>This bit is set to 1 by software, and cleared by hardware.<br>Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared to 0.                                                                                                                                  |
| 1     | CC1EG    | W   | Capture/Compare Channel1 Event Generation<br>0: Invalid<br>1: Capture/Compare event is generated<br>This bit is set to 1 by software and cleared automatically by hardware.<br>If Channel 1 is in output mode:<br>When CC1IFLG=1, if CC1IEN bit is set, the corresponding interrupt will be generated.<br>If Channel 1 is in input mode:<br>The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN bit is also set, the corresponding interrupt will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1. |
| 2     | CC2EG    | W   | Capture/Compare Channel2 Event Generation<br>Refer to CC1EG description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5:3   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 6     | TEG      | W   | Trigger Event Generate<br>0: Invalid<br>1: Trigger event is generated<br>This bit is set to 1 by software and cleared automatically by hardware.                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15:7  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

#### 16.8.6 Capature/Compare mode register 1 (TMRx\_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCx in the register describes the function of the channel in the output mode, and the ICx in the register describes the function of the channel in the input mode.

**Output compare mode:**

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL   | R/W | <p>Capture/Compare Channel 1 Select</p> <p>This bit defines the input/output direction and the selected input pin.</p> <p>00: CC1 channel is output</p> <p>01: CC1 channel is input, and IC1 is mapped on TI1</p> <p>10: CC1 channel is input, and IC1 is mapped on TI2</p> <p>11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input</p> <p>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2     | OC1FEN   | R/W | <p>Output Compare Channel1 Fast Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>This bit is used to improve the response of the capture/compare output to the trigger input event.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3     | OC1PEN   | R/W | <p>Output Compare Channel1 Preload Enable</p> <p>0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately.</p> <p>1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated.</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6:4   | OC1MOD   | R/W | <p>Output Compare Channel1 Mode Configure</p> <p>000: Freeze The output compare has no effect on OC1REF</p> <p>001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level</p> <p>010: The output value is low when matching. When the value of the counter matches the value of the capture/compare register, OC1REF will be forced to be at low level</p> <p>011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF</p> <p>100: The output is forced to be low Force OC1REF to be at low level</p> <p>101: The output is forced to be high. Force OC1REF to be at high level</p> <p>110: PWM mode 1 (set to high when the counter value&lt;output compare value; otherwise, set to low)</p> <p>111: PWM mode 2 (set to high when the counter value&gt;output compare value; otherwise, set to low)</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the compare result changes or when the output compare mode changes from freeze mode to PWM mode.</p> |
| 7     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8   | CC2SEL   | R/W | Capture/Compare Channel2 Select<br>This bit defines the input/output direction and the selected input pin.<br>00: CC2 channel is output<br>01: CC2 channel is input, and IC2 is mapped on TI2<br>10: CC2 channel is input, and IC2 is mapped on TI1<br>11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0). |
| 10    | OC2FEN   | R/W | Output Compare Channel2 Preload Enable                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11    | OC2PEN   | R/W | Output Compare Channel2 Buffer Enable                                                                                                                                                                                                                                                                                                                                                                                                              |
| 14:12 | OC2MOD   | R/W | Output Compare Channel2 Mode                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

#### Input capture mode:

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL | R/W | Capture/Compare Channel 1 Select<br>00: CC1 channel is output<br>01: CC1 channel is input, and IC1 is mapped on TI1<br>10: CC1 channel is input, and IC1 is mapped on TI2<br>11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN bit CC1EN=0).                   |
| 3:2   | IC1PSC | R/W | Input Capture Channel 1 Prescaler Configure<br>00: PSC=1<br>01: PSC=2<br>10: PSC=4<br>11: PSC=8<br>PSC is prescaled factor, which triggers capture once every PSC events.                                                                                                                                                                                                             |
| 7:4   | IC1F   | R/W | Input Capture Channel 1 Filter Configure<br>0000: Filter disabled, sampling by $f_{DTS}$<br>0001: DIV=1, N=2<br>0010: DIV=1, N=4<br>0011: DIV=1, N=8<br>0100: DIV=2, N=6<br>0101: DIV=2, N=8<br>0110: DIV=4, N=6<br>0111: DIV=4, N=8<br>1000: DIV=8, N=6<br>1001: DIV=8, N=8<br>1010: DIV=16, N=5<br>1011: DIV=16, N=6<br>1100: DIV=16, N=8<br>1101: DIV=32, N=5<br>1110: DIV=32, N=6 |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |        |     | 1111: DIV=32, N=8<br>Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.                                                                                                                                                                                                                           |
| 9:8   | CC2SEL | R/W | Capture/Compare Channel 2 Select<br>00: CC2 channel is output<br>01: CC2 channel is input, and IC2 is mapped on TI2<br>10: CC2 channel is input, and IC2 is mapped on TI1<br>11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC2EN=0). |
| 11:10 | IC2PSC | R/W | Input Capture Channel 2 Perscaler Configuration                                                                                                                                                                                                                                                                                                                          |
| 15:12 | IC2F   | R/W | Input Capture Channel 2 Filter Configuration                                                                                                                                                                                                                                                                                                                             |

### 16.8.7 Capture/Compare enable register (TMRx\_CCEN)

Offset address: 0x20

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CC1EN  | R/W | Capture/Compare Channel1 Output Enable<br>When the capture/compare channel 1 is configured as output:<br>0: Output is disabled<br>1: Output is enabled<br>When the capture/compare channel 1 is configured as input:<br>This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register<br>0: Capture is disabled<br>1: Capture is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1     | CC1POL | R/W | Capture/Compare Channel1 Output Polarity Configure<br>When CC1 channel is configured as output:<br>0: OC1 high level is valid<br>1: OC1 low level is valid<br>When CC1 channel is configured as input:<br>CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time<br>00: Non-phase-inverting/rising edge:<br>TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).<br>01: Inverted phase/Falling edge:<br>TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).<br>10: Reserved<br>11: Non-phase-inverting/Rising and falling edges:<br>TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Reserved |     |                                                                                                                                                                                                                                                                                                                   |
| 3     | CC1NPOL  | R/W | Capture/Compare Channel1 Output Polarity Configure<br>When CC1 channel is configured as output:<br>CC1NPOL remains in cleared state all the time<br>When CC1 channel is configured as input:<br>This bit and CC1POL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time. |
| 4     | CC2EN    | R/W | Capture/Compare Channel2 Output Enable<br>Refer to CCEN_CC1EN                                                                                                                                                                                                                                                     |
| 5     | CC2POL   | R/W | Capture/Compare Channel2 Output Polarity Configure<br>Refer to CCEN_CC1POL                                                                                                                                                                                                                                        |
| 6     | Reserved |     |                                                                                                                                                                                                                                                                                                                   |
| 7     | CC2NPOL  | R/W | Capture/Compare Channel2 Output Polarity Configure<br>Refer to CCEN_CC1NPOL                                                                                                                                                                                                                                       |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                   |

Table 72 Output Control Bit of Standard OCx Channel

| CCxEN bit | OCx output state                     |
|-----------|--------------------------------------|
| 0         | Output is disabled (OCx=0, OCx_EN=0) |
| 1         | OCx=OCxREF+polarity, OCx_EN=1        |

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

### 16.8.8 Counter register (TMRx\_CNT)

Offset address: 0x24

Reset value: 0x0000

| Field | Name | R/W | Description   |
|-------|------|-----|---------------|
| 15:0  | CNT  | R/W | Counter Value |

### 16.8.9 Prescaler register (TMRx\_PSC)

Offset address: 0x28

Reset value: 0x0000

| Field | Name | R/W | Description                                                                         |
|-------|------|-----|-------------------------------------------------------------------------------------|
| 15:0  | PSC  | R/W | Prescaler Value<br>Clock frequency of counter (CK_CNT)=f <sub>CK_PSC</sub> /(PSC+1) |

### 16.8.10 Auto reload register (TMRx\_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

| Field | Name    | R/W | Description                                                                              |
|-------|---------|-----|------------------------------------------------------------------------------------------|
| 15:0  | AUTORLD | R/W | Auto Reload Value<br>When the value of auto reload is empty, the counter will not count. |

### 16.8.11 Channel 1 capture/compare register (TMRx\_CC1)

Offset address: 0x34

Reset value: 0x0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | CC1  | R/W | <p>Capture/Compare Channel 1 Value</p> <p>When the capture/compare channel 1 is configured as input mode:<br/>CC1 contains the counter value transmitted by the last input capture channel 1 event.</p> <p>When the capture/compare channel 1 is configured as output mode:<br/>CC1 contains the current load capture/compare register value</p> <p>Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1.</p> <p>When the output compare preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output comparison results;</p> <p>If the output compare preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output compare result when an update event is generated.</p> |

### 16.8.12 Channel 2 capture/compare register (TMRx\_CC2)

Offset address: 0x38

Reset value: 0x0000

| Field | Name | R/W | Description                                                     |
|-------|------|-----|-----------------------------------------------------------------|
| 15:0  | CC2  | R/W | <p>Capture/Compare Channel 2 Value</p> <p>Refer to TMRx_CC1</p> |

## 16.9 TMR10/11/13/14 register address mapping

In the following table, all registers of TMR10/11/13/14 are mapped to a 16-bit addressable (address) space.

Table 73 TMR10/11/13/14 Register Address Mapping

| Register name | Description                        | Offset address |
|---------------|------------------------------------|----------------|
| TMRx_CTRL1    | Control register 1                 | 0x00           |
| TMRx_DIEN     | DMA/Interrupt enable register      | 0x0C           |
| TMRx_STS      | State register                     | 0x10           |
| TMRx_CEG      | Control event generation register  | 0x14           |
| TMRx_CCM1     | Capture/Compare mode register 1    | 0x18           |
| TMRx_CCEN     | Capture/Compare enable register    | 0x20           |
| TMRx_CNT      | Counter register                   | 0x24           |
| TMRx_PSC      | Prescaler register                 | 0x28           |
| TMRx_AUTORLD  | Auto reload register               | 0x2C           |
| TMRx_CC1      | Channel 1 capture/compare register | 0x34           |



| Register name | Description     | Offset address |
|---------------|-----------------|----------------|
| TMR11_OPT     | Option register | 0x50           |

## 16.10 TMR10/11/13/14 register functional description

### 16.10.1 Control register 1 (TMRx\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CNTEN    | R/W | Counter Enable<br>0: Disable<br>1: Enable<br>When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.                                               |
| 1     | UD       | R/W | Update Disable<br>Update event can cause AUTORLD, PSC and CCx to generate the value of update setting.<br>0: Update event is allowed (UEV)<br>An update event can occur in any of the following situations:<br>The counter overruns;<br>Set UEG bit.<br>1: Update event is disabled                                            |
| 2     | URSSEL   | R/W | Update Request Source Select<br>If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit.<br>0: The counter overruns;<br>Set UEG bit.<br>1: The counter overruns                                                       |
| 6:3   | Reserved |     |                                                                                                                                                                                                                                                                                                                                |
| 7     | ARPEN    | R/W | Auto-reload Preload Enable<br>When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event.<br>0: Disable<br>1: Enable |
| 9:8   | CLKDIV   | R/W | Clock Divide Factor<br>For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit.<br>00: $t_{DTS}=t_{CK\_INT}$<br>01: $t_{DTS}=2 \times t_{CK\_INT}$<br>10: $t_{DTS}=4 \times t_{CK\_INT}$<br>11: Reserved   |

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 15:10 | Reserved |     |             |

### 16.10.2 DMA/Interrupt enable register (TMRx\_DIEN)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name     | R/W | Description                                                          |
|-------|----------|-----|----------------------------------------------------------------------|
| 0     | UIEN     | R/W | Update interrupt Enable<br>0: Disable<br>1: Enable                   |
| 1     | CC1IEN   | R/W | Capture/Compare Channel1 Interrupt Enable<br>0: Disable<br>1: Enable |
| 15:2  | Reserved |     |                                                                      |

### 16.10.3 State register (TMRx\_STS)

Offset address: 0x10

Reset value: 0x0000

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UIFLG    | RC_W0 | Update Event Interrupt Generate Flag<br>0: Update event interrupt does not occur<br>1: Update event interrupt occurs<br><br>When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations:<br>(1) UD=0 on TMRx_CTRL1 register, and when counter overruns, an update event will be generated;<br>(2) URSEL=0 and UD=0 on TMRx_CTRL1 register, configure UG = 1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software. |
| 1     | CC1IFLG  | RC_W0 | Capture/Compare Channel1 Interrupt Flag<br>When the capture/compare channel 1 is configured as output:<br>0: No matching occurred<br>1: The value of TMRx_CNT matches the value of TMRx_CC1<br>When the capture/compare channel 1 is configured as input:<br>0: Input capture did not occur<br>1: Input capture occurred<br><br>When a capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.                                                                                                                                   |
| 8:2   | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                  |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9     | CC1RCFLG | RC_W0 | Capture/compare Channel1 Repetition Capture Flag<br>0: Repeat capture does not occur<br>1: Repeat capture occurs<br>The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture. |
| 15:10 | Reserved |       |                                                                                                                                                                                                                                                                                                              |

#### 16.10.4 Control event generation register (TMRx\_CEG)

Offset address: 0x14

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UEG      | W   | Update Event Generate<br>0: Invalid<br>1: Initialize the counter and generate the update event<br>This bit is set to 1 by software, and cleared by hardware.<br>Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared to 0.                                                                                                                                          |
| 1     | CC1EG    | W   | Capture/Compare Channel1 Event Generation<br>0: Invalid<br>1: Capture/Compare event is generated<br>This bit is set to 1 by software and cleared automatically by hardware.<br>If Channel 1 is in output mode:<br>When CC1IFLG=1, if CC1IEN bit is set, the corresponding interrupt request will be generated.<br>If Channel 1 is in input mode:<br>The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN bit is also set, the corresponding interrupt will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1. |
| 15:2  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

#### 16.10.5 Capture/Compare mode register 1 (TMRx\_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

**Output compare mode:**

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL   | R/W | <p>Capture/Compare Channel 1 Select</p> <p>This bit defines the input/output direction and the selected input pin.</p> <p>00: CC1 channel is output</p> <p>01: CC1 channel is input, and IC1 is mapped on TI1</p> <p>10: Reserved</p> <p>11: Reserved</p> <p>Note: This bit can be written only when the channel is closed (TMRx_CCEN register CC1EN=0).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2     | OC1FEN   | R/W | <p>Output Compare Channel1 Fast Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>This bit is used to improve the response of the capture/compare output to the trigger input event.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 3     | OC1PEN   | R/W | <p>Output Compare Channel1 Preload Enable</p> <p>0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately.</p> <p>1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated.</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 6:4   | OC1MOD   | R/W | <p>Output Compare Channel1 Mode Configure</p> <p>000: Freeze The output compare has no effect on OC1REF</p> <p>001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level</p> <p>010: The output value is low when matching. When the value of the counter matches the value of the capture/compare register, OC1REF will be forced to be at low level</p> <p>011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF</p> <p>100: The output is forced to be low Force OC1REF to be at low level</p> <p>101: The output is forced to be high. Force OC1REF to be at high level</p> <p>110: PWM mode 1 (set to high when the counter value&lt;output compare value; otherwise, set to low)</p> <p>111: PWM mode 2 (set to high when the counter value&gt;output compare value; otherwise, set to low)</p> <p>Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output compare mode changes from freeze mode to PWM mode.</p> |
| 15:7  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

#### Input capture mode:

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | CC1SEL   | R/W | Capture/Compare Channel 1 Select<br>00: CC1 channel is output<br>01: CC1 channel is input, and IC1 is mapped on TI1<br>10: Reserved<br>11: Reserved<br>Note: This bit can be written only when the channel is closed (TMRx_CCEN bit CC1EN=0).                                                                                                                                                                                                                                                                                           |
| 3:2   | IC1PSC   | R/W | Input Capture Channel 1 Perscaler Configure<br>00: PSC=1<br>01: PSC=2<br>10: PSC=4<br>11: PSC=8<br>PSC is prescaled factor, which triggers capture once every PSC events.                                                                                                                                                                                                                                                                                                                                                               |
| 7:4   | IC1F     | R/W | Input Capture Channel 1 Filter Configure<br>0000: Filter disabled, sampling by $f_{DTS}$<br>0001: DIV=1, N=2<br>0010: DIV=1, N=4<br>0011: DIV=1, N=8<br>0100: DIV=2, N=6<br>0101: DIV=2, N=8<br>0110: DIV=4, N=6<br>0111: DIV=4, N=8<br>1000: DIV=8, N=6<br>1001: DIV=8, N=8<br>1010: DIV=16, N=5<br>1011: DIV=16, N=6<br>1100: DIV=16, N=8<br>1101: DIV=32, N=5<br>1110: DIV=32, N=6<br>1111: DIV=32, N=8<br>Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events. |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

### 16.10.6 Capture/Compare enable register (TMRx\_CCEN)

Offset address: 0x20

Reset value: 0x0000

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CC1EN | R/W | Capture/Compare Channel1 Output Enable<br>When the capture/compare channel 1 is configured as output:<br>0: Output is disabled<br>1: Output is enabled<br>When the capture/compare channel 1 is configured as input:<br>This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register<br>0: Capture is disabled |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 1: Capture is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1     | CC1POL   | R/W | <p>Capture/Compare Channel1 Output Polarity Configure</p> <p>When CC1 channel is configured as output:</p> <p>0: OC1 high level is valid</p> <p>1: OC1 low level is valid</p> <p>When CC1 channel is configured as input:</p> <p>CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time</p> <p>00: Non-phase-inverting/rising edge:</p> <p>TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).</p> <p>01: Inverted phase/Falling edge:</p> <p>TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).</p> <p>10: Reserved</p> <p>11: Non-phase-inverting/Rising and falling edges:</p> <p>TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).</p> |
| 2     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 3     | CC1NPOL  | R/W | <p>Capture/Compare Channel1 Output Polarity Configure</p> <p>When CC1 channel is configured as output:</p> <p>CC1NPOL remains in cleared state all the time</p> <p>When CC1 channel is configured as input:</p> <p>This bit and CC1POL control the polarity of the triggered or captured signals TI1FP1 at the same time.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 15:4  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

Table 74 Output Control Bit of Standard OCx Channel

| CCxEN bit | OCx output state                     |
|-----------|--------------------------------------|
| 0         | Output is disabled (OCx=0, OCx_EN=0) |
| 1         | OCx=OCxREF+polarity, OCx_EN=1        |

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

### 16.10.7 Counter register (TMRx\_CNT)

Offset address: 0x24

Reset value: 0x0000

| Field | Name | R/W | Description   |
|-------|------|-----|---------------|
| 15:0  | CNT  | R/W | Counter Value |

### 16.10.8 Prescaler register (TMRx\_PSC)

Offset address: 0x28

Reset value: 0x0000

| Field | Name | R/W | Description                                                                        |
|-------|------|-----|------------------------------------------------------------------------------------|
| 15:0  | PSC  | R/W | Prescaler Value<br>Clock frequency of counter (CK_CNT) = $f_{CK\_PSC} / (PSC + 1)$ |

#### 16.10.9 Auto reload register (TMRx\_AUTORD)

Offset address: 0x2C

Reset value: 0xFFFF

| Field | Name   | R/W | Description                                                                              |
|-------|--------|-----|------------------------------------------------------------------------------------------|
| 15:0  | AUTORD | R/W | Auto Reload Value<br>When the value of auto reload is empty, the counter will not count. |

#### 16.10.10 Channel 1 capture/compare register (TMRx\_CC1)

Offset address: 0x34

Reset value: 0x0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | CC1  | R/W | Capture/Compare Channel 1 Value<br>When the capture/compare channel 1 is configured as input mode:<br>CC1 contains the counter value transmitted by the last input capture channel 1 event.<br>When the capture/compare channel 1 is configured as output mode:<br>CC1 contains the current load capture/compare register value<br>Compare the value CC1 of the capture/compare channel 1 with the value CNT of the counter to generate the output signal on OC1.<br>When the output compare preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output comparison results;<br>If the output compare preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output compare result when an update event is generated. |

#### 16.10.11 Option register (TMR11\_OPT)

Offset address: 0x50

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                              |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | RMPSEL   | R/W | Timer11 Input 1 Remap Select<br>00: TMR11 channel 1 is connected to GPIO<br>01: TMR11 channel 1 is connected to GPIO<br>10: HSECLK_RTC clock is connected to TMR11_CH1 input<br>11: TMR11 channel 1 is connected to GPIO |
| 15:2  | Reserved |     |                                                                                                                                                                                                                          |

## 17 Basic Timer (TMR6/7)

### 17.1 Introduction

The basic timers TMR6 and TMR7 have an unsigned 16-bit counter, auto reload register, prescaler and trigger controller.

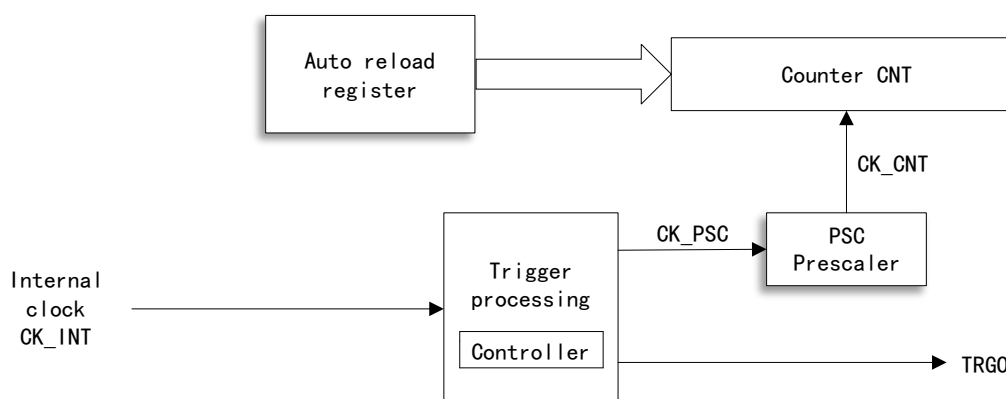
The basic timer can be used as a general-purpose timer to generate a time reference, and it also provides a clock for the DAC. Through configuration, it can generate DMA requests.

### 17.2 Main characteristics

- (1) Counter: 16-bit counter, which can only count up
- (2) Prescaler: 16-bit programmable prescaler
- (3) Clock source: There is only internal clock
- (4) Single-pulse mode
- (5) Provide clock for DAC

### 17.3 Structure block diagram

Figure 61 Basic Timer Structure Block Diagram



### 17.4 Functional description

#### 17.4.1 Clock source selection

The basic timer is driven by internal clock source TMRx\_CLK.

Configure the CNTEN bit of TMRx\_CTRL1 register to enable the counter; when CNTEN bit is set, the internal clock CK\_INT can generate CK\_CNT to drive the counter through the controller and prescaler.



### 17.4.2 Timebase unit

The time base unit in the basic timer contains three registers:

- 16-bit counter register (CNT)
- 16-bit auto reload register (AUTORLD)
- 16-bit prescaler register (PSC)

#### Counter CNT

The basic timer only has one count mode: count-up

##### Count-up mode

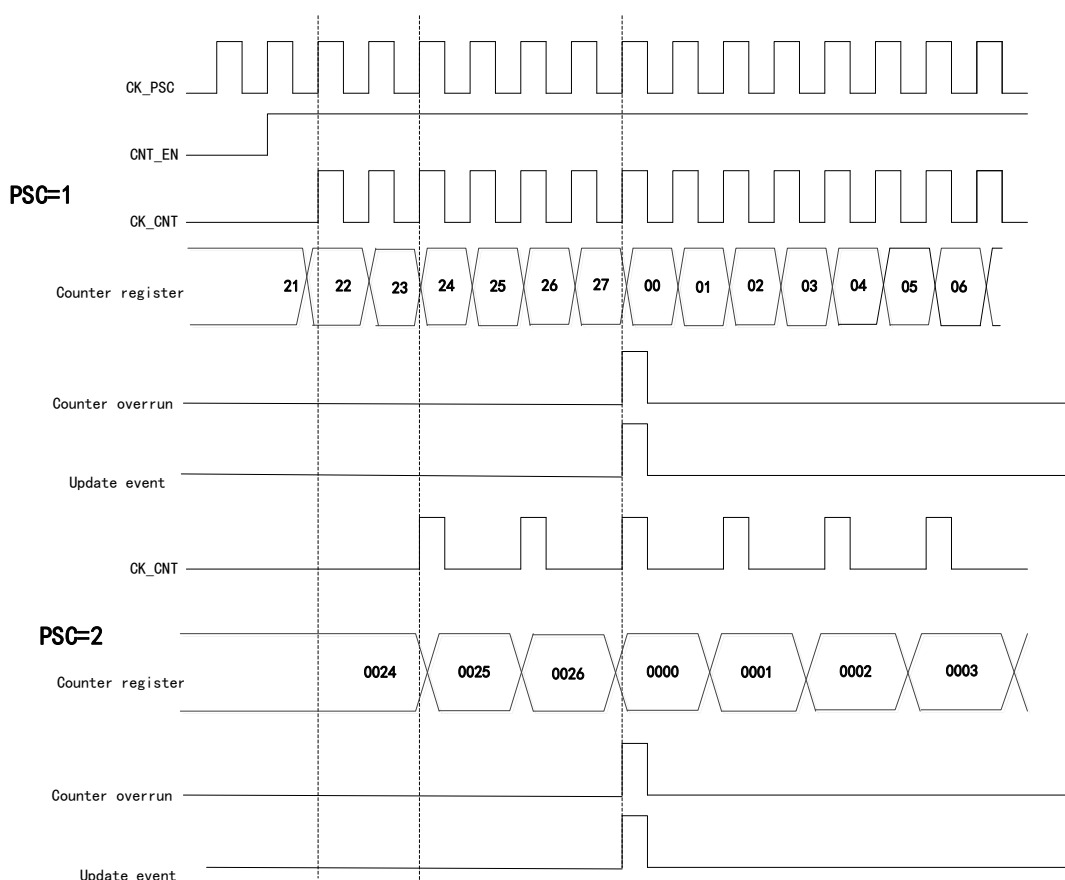
When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx\_CNT) is equal to the value of the auto reload (TMRx\_AUTORLD), then the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMRx\_AUTORLD) is written in advance.

Disable the update event and set UD bit of TMRx\_CTRL1 register to 1.

Generate the update interrupt or DMA request and set URSSEL bit in TMRx\_CTRL1 register.

When an update event occurs, both the auto reload register and the prescaler register will be updated.

Figure 62 Timer Timing Diagram, the internal clock division factor is 1 or 2



## Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx\_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

### 17.4.3 Debug mode

The TMR6/7 can be configured in debug mode and choose to stop or continue to work. It depends on the TMRx\_STS bit of DBGMCU\_APB1F register in DBGMCU module.

## 17.5 Register address mapping

In the following table, all registers of the basic timer are mapped to a 16-bit addressable (address) space.

Table 75 TMR6/7 Register Address Mapping

| Register name | Description                       | Offset address |
|---------------|-----------------------------------|----------------|
| TMRx_CTRL1    | Control register 1                | 0x00           |
| TMRx_CTRL2    | Control register 2                | 0x04           |
| TMRx_DIEN     | DMA/Interrupt enable register     | 0x0C           |
| TMRx_STS      | State register                    | 0x10           |
| TMRx_CEG      | Control event generation register | 0x14           |
| TMRx_CNT      | Counter register                  | 0x24           |
| TMRx_PSC      | Prescaler register                | 0x28           |
| TMRx_AUTORLD  | Auto reload register              | 0x2C           |

## 17.6 Register functional description

### 17.6.1 Control register 1 (TMRx\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                       |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CNTEN  | R/W | Counter Enable<br>0: Disable<br>1: Enable<br>When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.                                                  |
| 1     | UD     | R/W | Update Disable<br>Update event can cause AUTORLD, PSC and CCx to generate the value of update setting.<br>0: Update event is allowed (UEV)<br>An update event can occur in any of the following situations:<br>The counter overruns;<br>Set UEG bit;<br>Update generated by slave mode controller.<br>1: Update event is disabled |
| 2     | URSSEL | R/W | Update Request Source Select<br>If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit.<br>0: The counter overruns;<br>Set UEG bit;<br>Update generated by slave mode controller.<br>1: The counter overruns            |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3     | SPMEN    | R/W | Single Pulse Mode Enable<br>When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed.<br>0: Disable<br>1: Enable                                                   |
| 6:4   | Reserved |     |                                                                                                                                                                                                                                                                                                                                |
| 7     | ARPEN    | R/W | Auto-reload Preload Enable<br>When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event.<br>0: Disable<br>1: Enable |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                |

### 17.6.2 Control register 2 (TMRx\_CTRL2)

Offset address: 0x04

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 6:4   | MMSEL    | R/W | Master Mode Signal Select<br>The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode.<br>000: Reset; the reset signal of master mode timer is used for TRGO<br>001: Enable; the counter enable signal of master mode timer is used for TRGO<br>010: Update; the update event of master mode timer is used for TRGO<br>Others: Reserved |
| 15:7  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

### 17.6.3 DMA/Interrupt enable register (TMRx\_DIEN)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name     | R/W | Description                                          |
|-------|----------|-----|------------------------------------------------------|
| 0     | UIEN     | R/W | Update interrupt Enable<br>0: Disable<br>1: Enable   |
| 7:1   | Reserved |     |                                                      |
| 8     | UDIEN    | R/W | Update DMA Request Enable<br>0: Disable<br>1: Enable |
| 15:9  | Reserved |     |                                                      |

#### 17.6.4 State register (TMRx\_STS)

Offset address: 0x10

Reset value: 0x0000

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UIFLG    | RC_W0 | Update Event Interrupt Generate Flag<br>0: Update event interrupt does not occur<br>1: Update event interrupt occurs<br>When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations:<br>(1) UD=0 on TMRx_CTRL1 register, and when overruns, an update event will be generated;<br>(2) URSEL=0 and UD=0 on TMRx_CTRL1 register, configure UG = 1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software. |
| 15:1  | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

#### 17.6.5 Control event generation register (TMRx\_CEG)

Offset address: 0x14

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | UEG      | W   | Update Event Generate<br>0: Invalid<br>1: Initialize the counter and generate the update event<br>This bit is set to 1 by software, and cleared by hardware.<br>Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared to 0. |
| 15:1  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

#### 17.6.6 Counter register (TMRx\_CNT)

Offset address: 0x24

Reset value: 0x0000

| Field | Name | R/W | Description   |
|-------|------|-----|---------------|
| 15:0  | CNT  | R/W | Counter Value |

#### 17.6.7 Prescaler register (TMRx\_PSC)

Offset address: 0x28

Reset value: 0x0000

| Field | Name | R/W | Description                                                                        |
|-------|------|-----|------------------------------------------------------------------------------------|
| 15:0  | PSC  | R/W | Prescaler Value<br>Clock frequency of counter (CK_CNT) = $f_{CK\_PSC} / (PSC + 1)$ |

### 17.6.8 Auto reload register (TMRx\_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

| Field | Name    | R/W | Description                                                                              |
|-------|---------|-----|------------------------------------------------------------------------------------------|
| 15:0  | AUTORLD | R/W | Auto Reload Value<br>When the value of auto reload is empty, the counter will not count. |

## 18 Watchdog Timer (WDT)

### 18.1 Introduction

The watchdog is used to monitor system failures caused by software errors. There are two watchdog devices on the chip: independent watchdog and window watchdog, which improve the security, and make the time more accurate and the use more flexible.

The independent watchdog will reset only when the counter is reduced to 0, and the value of refresh counter will not be reset until it is not reduced to 0.

The window watchdog will reset when the counter decreases to 0x3F. When the count value of the counter is before the window value of the configuration register, the refresh counter will also be reset.

### 18.2 Independent watchdog timer (IWDT)

#### 18.2.1 Introduction

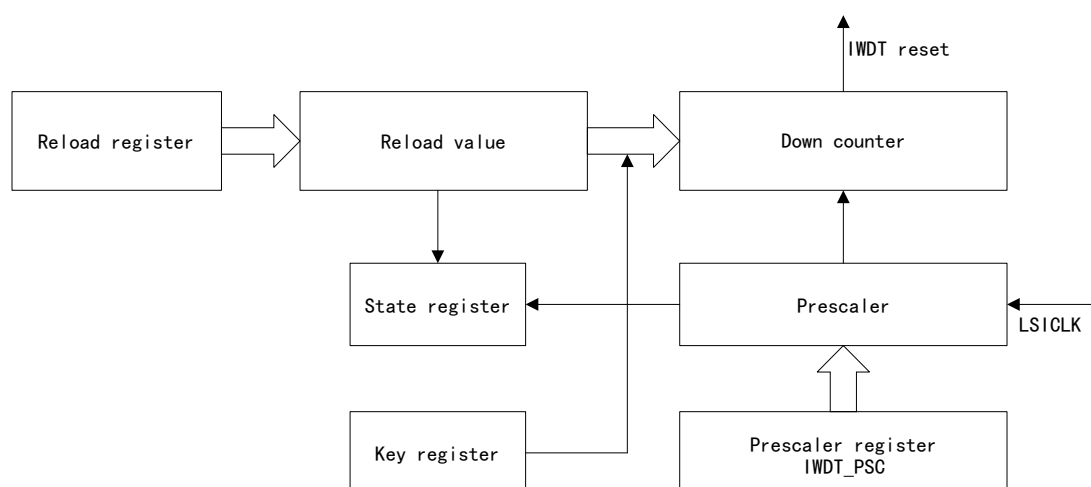
The independent watchdog consists of an 8-bit prescaler IWDT\_PSC, 12-bit count-down counter, 12-bit reload register IWDT\_CNTRLD, key register IWDT\_KEY and state register IWDT\_STS.

The independent watchdog has an independent clock source, and even if the master clock fails, it is still valid.

The independent watchdog is applicable to the situations where an independent environment is required but the accuracy requirement is not high.

#### 18.2.2 Structure block diagram

Figure 63 Independent Watchdog Structure Block Diagram



Note: The watchdog function is in the V<sub>DD</sub> power supply area and can work normally in the shutdown or standby mode.

## 18.2.3 Functional description

### 18.2.3.1 Key register

Write 0xCCCC in the key register to enable the independent watchdog, then the counter starts to count down, and when the counter counts to 0x000, a reset will be generated.

Write 0xAAAA in the key register, and the value of the reload register will be reloaded to the counter to prevent the watchdog from resetting.

Write 0x5555 in the key register to rewrite the value of the prescaler register and the reload register.

### 18.2.3.2 Register access protection

The prescaler register and reload register have the function of write protection. If you want to rewrite these two registers, you need to write 0x5555 in the key register. If you write other value in the key register, the protection of the register will be started again.

Write 0xAAAA to the key register and the write protection function will also be enabled.

### 18.2.3.3 Hardware watchdog

After the "hardware watchdog" function is enabled, and the system is powered on and reset, the watchdog will run automatically. If 0xAAAA is not written to the key register, reset will be generated after the counter finishes counting.

### 18.2.3.4 Debug mode

The independent watchdog can be configured in debug mode and choose to stop or continue to work. Depend on DBGMCU\_APB1F register IWDG\_STS bit.

Table 76 Min/max timeout when LSICLK=28kHz

| PSC | Min timeout value | Max timeout value |
|-----|-------------------|-------------------|
| 0   | 0.125ms           | 512ms             |
| 1   | 0.25ms            | 1024ms            |
| 2   | 0.5ms             | 2048ms            |
| 3   | 1ms               | 4096ms            |
| 44  | 2ms               | 8192ms            |
| 5   | 4ms               | 16384ms           |
| 6   | 8ms               | 32768ms           |



## 18.3 Window watchdog timer (WWDT)

### 18.3.1 Introduction

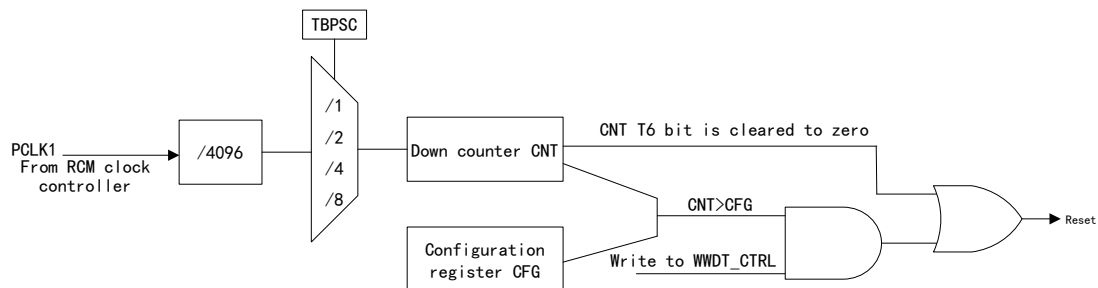
The window watchdog contains a 7-bit free-running down counter, prescaler and control register WWDT\_CTRL, configuration register WWDT\_CFG and state register WWDT\_STS.

The window watchdog clock comes from PCLK1, and the counter clock is obtained from the CK counter clock through frequency division by prescaler (configured by the configuration register).

The window watchdog is applicable when precise timing is needed.

### 18.3.2 Structure block diagram

Figure 64 Window Watchdog Structure Block Diagram



### 18.3.3 Functional description

Enable window watchdog timer. The reset conditions are:

- When the counter count is less than 0x40, a reset will be generated.
- The reload counter will be reset before the counter counts to the value of the window register.

After reset, the watchdog is always disabled and it can be enabled only by setting the WWDTEN bit of WWDT\_CTRL control register.

The counter of window watchdog is in free state. When the watchdog is disabled, the counter will continue to count down. The counter must be reloaded between the value of window register and 0x40 to avoid reset.

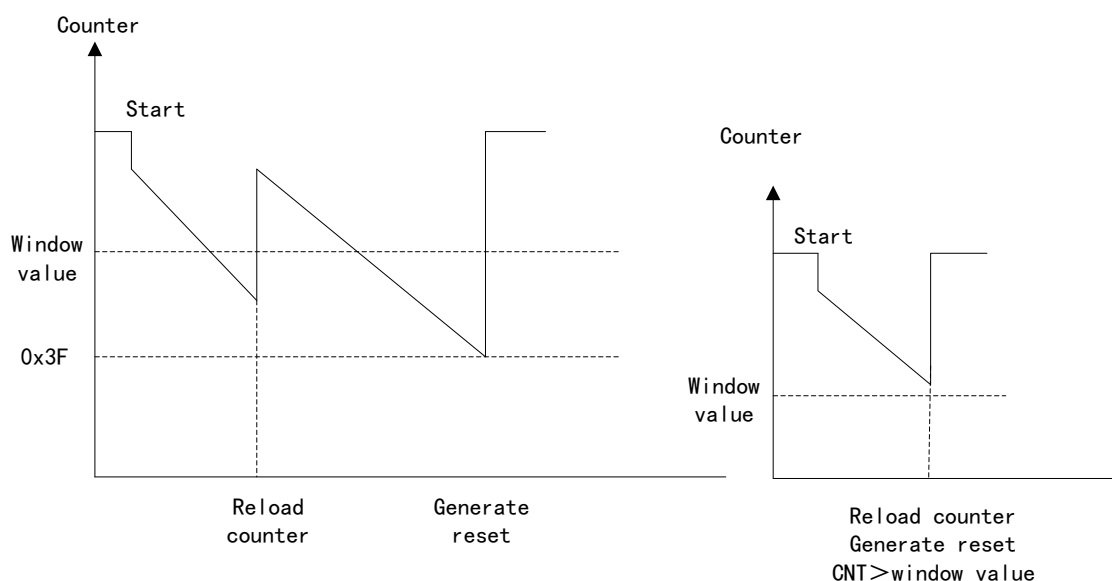
Setting the EWIE bit of the configuration register can enable the early wake-up interrupt. When the count reaches 0x40, the interrupt will be generated.

Entering the interrupt service program (ISR) can be used to prevent the window watchdog from resetting. EWIE interrupt can be cleared by writing 0 in the state register.

The windowed watchdog has a unique window feature that can effectively monitor whether the program is functioning correctly. For example: suppose a program segment runs for a time T, and the window register is set to a value slightly less than (TR - T). If the reloading of the register does not occur within

this window, it indicates a program fault. When the counter counts down to 0x3F, a reset will be triggered.

Figure 65 Window Watchdog Timing Diagram



The calculation formula of window watchdog timer timeout is as follows:

$$T_{WWDt} = T_{PCLK1} \times 2^{WTB} \times (T[5:0] + 1)$$

Wherein:

- $T_{WWDt}$ : WWDt timeout
- $T_{PCLK1}$ : Clock cycle of APB1 (in ms)

Minimum/Maximum timeout when PCLK1=36MHZ:

Table 77 Min/Max Timeout when PCLK1=36MHZ

| WTB | Min timeout value | Max timeout value |
|-----|-------------------|-------------------|
| 0   | 136.53μs          | 8.74ms            |
| 1   | 273.07μs          | 17.48ms           |
| 2   | 546.13μs          | 34.95ms           |
| 3   | 1092.27μs         | 69.91ms           |

## 18.4 IWDt register address mapping

Table 78 IWDt Register Address Mapping

| Register name | Description             | Offset address |
|---------------|-------------------------|----------------|
| IWDt_KEY      | Key register            | 0x00           |
| IWDt_PSC      | Prescaler register      | 0x04           |
| IWDt_CNTRLd   | Counter reload register | 0x08           |

| Register name | Description    | Offset address |
|---------------|----------------|----------------|
| IWDT_STS      | State register | 0x0C           |

## 18.5 IWDT register functional description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

### 18.5.1 Key register (IWDT\_KEY)

Offset address: 0x00

Reset value: 0x0000 0000 (reset in standby mode)

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | KEY      | W   | <p>Allow Access IWDT Register Key Value</p> <p>Writing 0x5555 means enabled access to IWDT_PSC and IWDT_CNTRLD registers;</p> <p>When the software writes 0xAAAA, it means to execute the reload counter, and a certain interval is required to prevent the watchdog from resetting.</p> <p>Write 0xCCCC and the watchdog will be enabled (the hardware watchdog is unrestricted by this command word).</p> <p>This register is write-only and the read-out value is 0x0000.</p> |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

### 18.5.2 Prescaler register (IWDT\_PSC)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | PSC      | R/W | <p>Prescaler Factor Configure</p> <p>Support the write protection function; when writing 0x5555 in the IWDT_KEY register, it is allowed to access the register; in the process of writing this register, only when IWDT_STS register PSCUFLG=0, can the prescaler factor be changed; in the process of reading this register, only when PSCUFLG=0, can the read-out value of PSC register be valid.</p> <p>000: PSC=4<br/> 001: PSC=8<br/> 010: PSC=16<br/> 011: PSC=32<br/> 100: PSC=64<br/> 101: PSC=128<br/> 110: PSC=256<br/> 111: PSC=256</p> |
| 31:3  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

### 18.5.3 Counter reload register (IWDT\_CNTRLD)

Offset address: 0x08

Reset value: 0x0000 0FFF (reset in standby mode)

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:0  | CNTRLD   | R/W | <p>Watchdog Counter Reload Value Setup</p> <p>It supports write protection function and defines the value loaded to the watchdog counter when 0xAAAA is written by IWDT_KEY register; in the process of writing this register, this register can be modified only when CNTUFLG=0. In the process of reading this register, when CNTUFLG=0 in IWDT_STS register, the read value is valid.</p> <p>The watchdog timeout cycle can be calculated by the reload value and clock prescaled value.</p> |
| 31:12 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

#### 18.5.4 State register (IWDT\_STS)

Offset address: 0x0C

Reset value: 0x0000 0000 (not reset in standby mode)

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                        |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PSCUFLG  | R   | <p>Watchdog Prescaler Factor Update Flag</p> <p>When the prescaler factor is updated, it is set to 1 by hardware; after the prescaler factor is updated, the bit is cleared by hardware; the prescaler factor is updated only when the PSCUFLG bit is cleared.</p>                 |
| 1     | CNTUFLG  | R   | <p>Watchdog Counter Reload Value Update Flag</p> <p>When the counter reload value is updated, it is set to 1 by hardware; after the counter reload value is updated, the bit is cleared by hardware; the counter reload value is updated only when the CNTUFLG bit is cleared.</p> |
| 31:2  | Reserved |     |                                                                                                                                                                                                                                                                                    |

### 18.6 WWDT register address mapping

Table 79 WWDT Register Address Mapping

| Register name | Description            | Offset address |
|---------------|------------------------|----------------|
| WWDT_CTRL     | Control register       | 0x00           |
| WWDT_CFG      | Configuration register | 0x04           |
| WWDT_STS      | State register         | 0x08           |

### 18.7 WWDT register functional description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

#### 18.7.1.1 Control register (WWDT\_CTRL)

Offset address: 0x00

Reset value: 0x0000 007F

| Field | Name     | R/W | Description                                                                                                                                                                                                                               |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0   | CNT      | R/W | Counter Value Setup<br>This counter is 7 bits, and CNT6 is the most significant bit<br>These bits are used to store the counter value of the watchdog.<br>When the count value decreases from 0x40 to 0x3F, WWDT reset will be generated. |
| 7     | WWDTEN   | R/S | Window Watchdog Enable<br>This bit is set to 1 by software and can be cleared by hardware only after reset. When WWDTEN=1, WWDT can generate a reset.<br>0: Disable<br>1: Enable                                                          |
| 31:8  | Reserved |     |                                                                                                                                                                                                                                           |

### 18.7.1.2 Configuration register (WWDT\_CFG)

Offset address: 0x04

Reset value: 0x0000 007F

| Field | Name     | R/W | Description                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0   | WIN      | R/W | Window Value Setup<br>This window value is 7 bits, which is used to compare with the down counter.                                                                                                              |
| 8:7   | TBPSC    | R/W | Timer Base Prescaler Factor Configure<br>Divide the frequency on the basis of PCLK1/4096<br>00: No frequency division<br>01: Two-divided frequency<br>10: Four-divided frequency<br>11: Eight-divided frequency |
| 9     | EWIEN    | R/S | Early Wakeup Interrupt Enable<br>0: No effect<br>1: When the counter value reaches 0x40, an interrupt will be generated; this interrupt is cleared by hardware after reset.                                     |
| 31:10 | Reserved |     |                                                                                                                                                                                                                 |

### 18.7.1.3 State register (WWDT\_STS)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name     | R/W   | Description                                                                                                                                                                                                                          |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | EWIFLG   | RC_W0 | Early Wakeup Interrupt Occur Flag<br>0: Not occur<br>1: When the counter value reaches 0x40, it is set to 1 by hardware; if the interrupt is not enabled, the bit will also be set to 1; it can be cleared by writing 0 by software. |
| 31:1  | Reserved |       |                                                                                                                                                                                                                                      |

## 19 Real-time Clock (RTC)

### 19.1 Full name and abbreviation description of terms

Table 80 Full name and abbreviation description of terms

| Full name in English | English abbreviation |
|----------------------|----------------------|
| Second               | SEC                  |
| Alarm                | ALR                  |
| Prescaler            | PSC                  |

### 19.2 Introduction

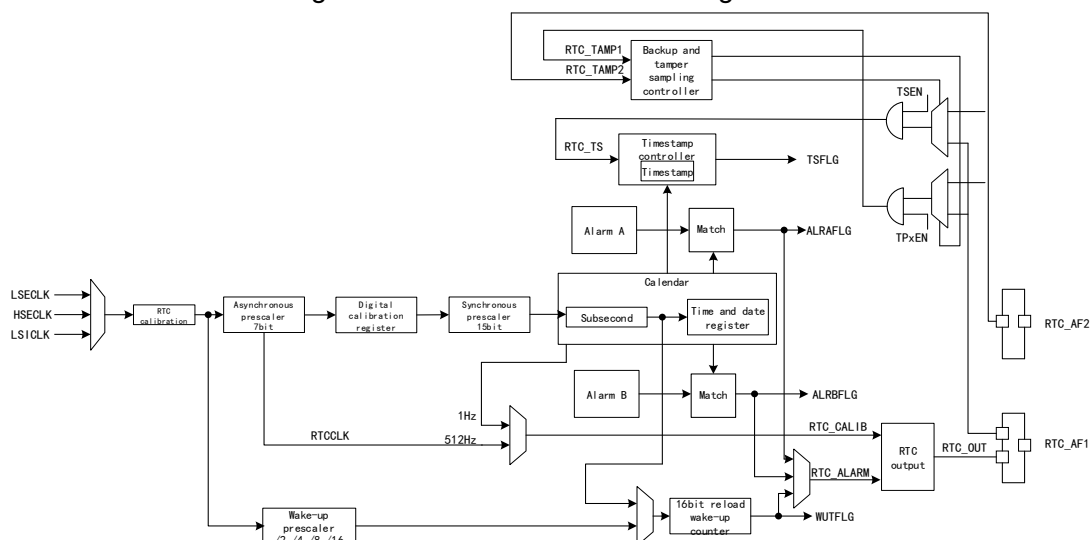
It features sub-second, time, and date registers encoded in BCD, along with corresponding alarm registers. When combined with external pins, it can implement timestamp functionality, accompanied by clock calibration and time compensation features.

### 19.3 Main characteristics

- (1) Timebase unit
- (2) Clock calibration
- (3) Subsecond, time and date
- (4) Time error compensation
- (5) Alarm (subsecond, time and date mask)
- (6) Timestamp
- (7) Tamper detection
- (8) 2 kinds of RTC outputs
- (9) Backup domain
- (10) Multiple interrupt control
- (11) Automatic wakeup of low power

### 19.4 Structure block diagram

Figure 66 RTC Structure Block Diagram



Note:

- (1) Alternate function output: RTC\_OUT is output in one of the following two forms
  - RTC\_CALIB: This output is enabled through CALOEN bit of RTC\_CTRL register, and when the frequency of LSECLK is 32.768kHz, the clock output is 512Hz or 1Hz.
  - RTC\_ALARM: This output, Alarm A, is enabled through OUTSEL bit of RTC\_CTRL register.
- (2) Alternate function input:
  - RTC\_TS: Timestamp event
  - RTC\_TAMP1: Tamper event detection 1
  - RTC\_TAMP2: Tamper event detection 2
- (3) The multiplexing function of RTC\_AF1 and RTC\_AF2 is connected to PC13 and PI8 respectively

## 19.5 Functional description

### 19.5.1 Timebase unit

## Clock source

RTC has three clock sources:

- External LSECLK crystal oscillator
- External HSECLK crystal oscillator
- Internal LSICLK

Select different clock sources by configuring the register of the clock controller CCM.

## Prescaler

When backup power supply is used, the power consumption of RTC peripherals should be as low as possible. Considering power consumption, RTC internally

adopts dual prescaler, 7-bit asynchronous prescaler APSC and 15-bit synchronous prescaler SPSC.

RTCCLK first passes through the asynchronous prescaler, and the clock after frequency division reaches the synchronous prescaler. Two prescalers can be reasonably configured to generate a 1Hz clock for date.

When the prescaler is used, it is suggested that the asynchronous prescaler should be adjusted as high as possible to reduce power consumption.

The synchronous prescaled value can also be used as the reload value of the subsecond counter.

## 19.5.2 Clock calibration

### Clock synchronization

RTC can realize clock synchronization according to external high-precision clock and the register RTC\_SHIFT. The deviation between RTC clock and external clock is detected mainly by acquiring the timestamps of subsecond time period twice. Since the synchronous prescaled value is used as the reload value of the subsecond counter, and the SFSEC bit of register RTC\_SHIFT is used in the subsecond counter, the SFSEC bit can be adjusted to finely tune the RTC clock and increase or decrease several cycles artificially.

### Reference clock

RTC has internal reference clock detection, which can be used to compensate the deviation of external LSECLK crystal oscillator. Set RCLKDEN bit to enable the reference clock detection, compare the external 50Hz or 60Hz reference clock with the internal 1Hz clock of RTC through RTC\_REFIN pin, and through this mechanism, the 1Hz clock after LSECLK frequency division is automatically compensated.

After the reference clock detection is enabled, the synchronous and asynchronous prescaler of the clock unit must be configured as the default value.

The reference clock detection cannot be used simultaneously with the clock synchronization, and it should be disabled in standby mode.

### RTC coarse digital calibration

RTC\_DCAL register can be configured as positive or negative calibration to update the date in advance or with delay, so the effective frequency can be adjusted.

### RTC precision digital calibration



RTC uses  $2^{20}$  RTCCLK as a calibration cycle by default. In addition,  $2^{19}$  and  $2^{18}$  RTCCLK can be set as a calibration cycle through the registers CALW16 and CALW8. When LSECLK is used as RTCCLK clock source, the calibration cycle of RTC is 32s, 16s, 8s.

- 16s calibration cycle; the hardware sets RECALF[0] to "0"
- 8s calibration cycle; the hardware sets RECALF[1:0] to "00"

Take 32s calibration cycle as an example, the calibration mechanism is to add or reduce some RTCCLK signals in the calibration cycle.

- When RECALF is used, RECALF RTCCLK are reduced every  $2^{20}$  RTCCLK
- When ICALFEN is used and ICALFEN=1, one RTCCLK is added every  $2^{11}$  RTCCLK
- When RECALF is used and ICALFEN,  $(512 * ICALFEN - RECALF)$  RTCCLK are added every  $2^{20}$  RTCCLK

### 19.5.3 RTC write protection

In order to prevent counting exception caused by accidental write, RTC register adopts write protection mechanism. Only when the write protection is removed, can the register with write protection function be operated.

After power-on, RTC register will enter the write protection state and the protection cannot be removed by system reset. The write protection can be removed by writing special keywords '0xCA' and '0x53' to the register RTC\_WRPROT. If the wrong keyword is written, RTC will immediately enable write protection.

### 19.5.4 Date register

RTC has subsecond, time and date shadow registers encoded by BCD, which are RTC\_SUBSEC, RTC\_TIME and RTC\_DATE respectively. The current date can be obtained by accessing the shadow register or obtained directly from the date register. The time system of 24 hours and 12 hours can be selected by TIMEFCFG bit of configuration register RTC\_CTRL.

RTC updates the shadow register every two RTCCLK cycles, and sets the flag bit RSFLG. When waking up from stop or standby mode, generally the shadow register will not be updated, which requires waiting for 1-2 RTCCLK cycles. The reset of shadow register is caused by system reset.

The shadow register is synchronized with  $f_{APB1}$ .

The way to read the date can be selected by RCMCFG bit of configuration register RTC\_CTRL.

#### **RCMCFG=0, read the date from the shadow register**

In this mode, it is recommended that  $f_{APB1}$  should be greater than  $7 * f_{RTCCLK}$ . If

$f_{APB1}$  is too small, to ensure the normal reading of date value, it is required to read the shadow register twice. If the date obtained twice is the same, the date is read successfully.

After the shadow register is updated, the flag bit RSFLG will be set. The software can read the date only after the bit RSFLG is set. Every time the date is read, the RSFLG flag should be cleared manually.

When waking up from stop or standby mode, since the shadow register is not updated, the RSFLG flag should be cleared immediately.

### **RCMCFG=1, read the date from the date register**

When  $f_{APB1}$  is less than  $7 \cdot f_{RTCCCLK}$  or the system is woken from low-power mode, it is recommended to read the date directly from the date register.

If RSFLG flag bit is not set to 1 when reading the date just at the stage of date register change, it is required to read the date twice. Therefore, it is also recommended to read the date register twice. When the read date value is the same twice, it means that the date is read successfully.

#### **19.5.5 Time compensation**

Due to seasonal changes, time compensation is sometimes needed to make it more suitable for daily needs. RTC is integrated with time compensation unit and its summer time flag. Users can choose whether to turn on time compensation according to their own needs.

By setting STCCFG bit of the register RTC\_CTRL, the summer time will increase by 1 hour; by setting WTCCFG bit of the register RTC\_CTRL, the winter time will decrease by 1. BAKP flag is used to record whether the summer time is set.

#### **19.5.6 Programmable alarm**

As a real-time clock, RTC integrates alarm function, and it runs mainly through alarm configuration register and alarm mask, in combination with date register.

Configure the alarm and alarm mask through the register RTC\_ALRMA/RTC\_ALRMAS and RTC\_ALRMB/RTC\_ALRMBSS, and the alarm mask informs RTC to pay attention to the time period of the alarm. After the alarm function is enabled, the alarm will be triggered only when the concerned time period reaches the set value. At this time, the alarm flag is set. If the alarm interrupt is enabled, the interrupt processing will be triggered.

Select "seconds" as the time period of the alarm, and only when the synchronous prescaler value is greater than 3, can the alarm operate normally.

#### **19.5.7 Timestamp**

RTC supports timestamp function and the RTC\_TS pin works together with the

timestamp register.

The timestamp polarity is detected through TSETECFG bit of the register RTC\_CTRL. When RTC\_TS pin recognizes the external timestamp edge signal, RTC will automatically latch the current date in the subsecond, time and date timestamp registers, and the timestamp flag bit TSFLG will be set to 1. If the timestamp interrupt is enabled, the timestamp interrupt processing will be triggered.

When TSFLG flag bit is set to 1, and a timestamp event occurs, the timestamp will overrun, and the flag bit TSOVRFLG will be set to 1. If a timestamp event is detected once TSFLG flag is cleared, both TSFLG and TSOVRFLG flags will be set to 1.

### **TAMPER multiplexing function**

RTC\_TAMP1 multiplexing function can be mapped to RTC\_AF1 or RTC\_AF2, and it is determined by TP1MSEL bit of RTC\_TACFG register. After TP1MSEL is modified, clear TP1EN bit to zero to avoid accidental setting of TP1FLG. Corresponding RTC\_TAMP2 pin of RTC\_TAMP2 multiplexing function.

#### **19.5.8 Backup domain**

After the main power supply  $V_{DD}$  is powered off, the backup domain register will be powered by  $V_{BAT}$  automatically. System resetting, NRST pin resetting, and resetting after the low mode is waken up will not affect the backup domain register. When  $V_{BAT}$  is powered off or tamper event occurs, the backup domain register will be reset.

The backup domain register can be used to cache user data, and can be used as a state flag to realize some function application by using the characteristics that the system reset data will remain unchanged.

#### **19.5.9 Tamper detection**

Tamper detection is a kind of data self-destruction protection device to prevent data leakage caused by tamper. Through the hardware circuit design, the tamper detection signal is sent to the tamper detection pin.

Tamper detection has multiple tamper detection pins, and each pin is enabled by a register bit separately. In order to detect real tamper events better, signal filtering can be configured, and tamper detection polarity can be configured for each pin.

### **Tamper detection polarity**

The low level/rising edge and high level/falling edge can be selected as tamper detection polarity through TPxAL bit in the register RTC\_TACFG.

## Tamper signal filter

TPSFSEL bit of the register RTC\_TACFG is used to configure the sampling frequency of tamper detection, and TPFSEL bit of RTC\_TACFG is used to configure after how many valid tamper signals are detected continuously, a tamper event can be generated.

In particular, if a tamper signal has been generated on the tamper detection pin before the tamper detection pin is enabled, an tamper event will be immediately generated on the enabled tamper detection pin.

## Tamper timestamp

At some times, in order to record the tamper detection events, RTC can latch the current tamper timestamp and this function can be enabled quickly through TPTSEN bit of the register RTC\_TACFG, not needing to enable the timestamp function additionally.

### 19.5.10 Automatic wake-up

Compared with RTC alarm, the hardware structure of the automatic wake-up is simpler, and it has no complicated configuration process of RTC alarm, so it is a good scheme to wake up the low power consumption.

There is a 16-bit self-decrement reload counter in RTC, and it is used to wake up the device automatically.

The clock of this counter is selected by WUCLKSEL bit of the register RTC\_CTRL, and by selecting different clocks, the automatic wake-up cycle can be configured from 122 $\mu$ s to 36h. First turn off the automatic wake-up, that is, clear WUTEN; when WUTWFLG flag bit is set to 1, configure WUCLKSEL bit of the RTC\_CTRL register and the reload register RTC\_AUTORLD.

When the counter decreases to 0, a wake-up event will be generated, WUTFLG flag bit will be set to 1, and before entering the next round of automatic wake-up, this flag bit must be cleared.

### 19.5.11 RTC output

RTC output transmits the internal RTC calibration clock, alarm signal, and automatic wake-up signal to the outside.

## RTC calibration clock

Calibration clock output is generally used to observe the accuracy of RTC clock source, and the observed value is used to calibrate the clock source. 512Hz and 1Hz signal output sources can be selected through CALOSEL bit of RTC\_CTRL register, and CALOEN bit of RTC\_CTRL register can enable the calibration output.

## Calibration multiplexing function output

When CALOEN bit of RTC\_CTRL register is set, RTC\_AF1 will enable the calibration multiplexing function.

## Alarm and automatic wake-up signal

When the alarm or automatic wake-up is running, these two events can be output as pulse signals. OUTSEL bit of RTC\_CTRL register is used to select the signal output source, and POLCFG bit is used to configure the output polarity.

## 19.6 Register address mapping

Table 81 RTC Register Address Mapping

| Register name | Description                                        | Offset address |
|---------------|----------------------------------------------------|----------------|
| RTC_TIME      | RTC time register                                  | 0x00           |
| RTC_DATE      | RTC date register                                  | 0x04           |
| RTC_CTRL      | RTC control register                               | 0x08           |
| RTC_STS       | RTC state register                                 | 0x0C           |
| RTC_PSC       | RTC prescaler register                             | 0x10           |
| RTC_AUTORLD   | RTC auto reload register                           | 0x14           |
| RTC_DCAL      | RTC coarse calibration register                    | 0x18           |
| RTC_ALRMA     | RTC alarm A register                               | 0x1C           |
| RTC_ALRMB     | RTC alarm B register                               | 0x20           |
| RTC_WRPROT    | RTC write protection register                      | 0x24           |
| RTC_SUBSEC    | RTC subsecond register                             | 0x28           |
| RTC_SHIFT     | RTC shift register                                 | 0x2C           |
| RTC_TSTIME    | RTC timestamp time register                        | 0x30           |
| RTC_TSDATE    | RTC timestamp date register                        | 0x34           |
| RTC_TSSUBSEC  | RTC timestamp subsecond register                   | 0x38           |
| RTC_CAL       | RTC calibration register                           | 0x3C           |
| RTC_TACFG     | RTC tamper and multiplexing configuration register | 0x40           |
| RTC_ALRMASS   | RTC alarm A subsecond register                     | 0x44           |
| RTC_ALRMBSS   | RTC alarm B subsecond register                     | 0x48           |
| RTC_BAKPx     | RTC backup register                                | 0x50-0x9C      |

## 19.7 Register functional description

### 19.7.1 RTC time register (RTC\_TIME)

Offset address: 0x00

Reset value of backup domain: 0x0000 0000

System reset: RCMCFG =0: 0x0000 0000; RCMCFG =1: 0xFFFF XXXX

RTC\_TIME is time shadow register, and this register can be written only in initialization mode to be put in write protection state.

| Field | Name     | R/W | Description                                               |
|-------|----------|-----|-----------------------------------------------------------|
| 3:0   | SECU     | R/W | Set Up the Units Digit of Seconds in BCD Format           |
| 6:4   | SECT     | R/W | Set Up the Tens Digit of Seconds in BCD Format            |
| 7     | Reserved |     |                                                           |
| 11:8  | MINU     | R/W | Set Up the Units Digit of Minutes in BCD Format           |
| 14:12 | MINT     | R/W | Set Up the Tens Digit of Minutes in BCD Format            |
| 15    | Reserved |     |                                                           |
| 19:16 | HRU      | R/W | Set Up the Units Digit of Hours in BCD Format             |
| 21:20 | HRT      | R/W | Set Up the Tens Digit of Hours in BCD Format              |
| 22    | TIMEFCFG | R/W | Time Format Configure<br>0: AM or 24-hour system<br>1: PM |
| 31:23 | Reserved |     |                                                           |

### 19.7.2 RTC date register (RTC\_DATE)

Offset address: 0x04

Reset value of backup domain: 0x0000 2101

System reset: RCMCFG =0: 0x0000 0000; RCMCFG =1: 0xFFFF XXXX

RTC\_DATE is date shadow register, and this register can be written only in initialization mode to be put in write protection state.

| Field | Name     | R/W | Description                                                                |
|-------|----------|-----|----------------------------------------------------------------------------|
| 3:0   | DAYU     | R/W | Set Up the Units Digit of Days in BCD Format                               |
| 5:4   | DAYT     | R/W | Set Up the Tens Digit of Days in BCD Format                                |
| 7:6   | Reserved |     |                                                                            |
| 11:8  | MONU     | R/W | Set Up the Units Digit of Months in BCD Format                             |
| 12    | MONT     | R/W | Set Up the Tens Digit of Months in BCD Format                              |
| 15:13 | WEEKSEL  | R/W | Week Day Units Select<br>000: Disable<br>001: Monday<br>...<br>111: Sunday |

| Field | Name     | R/W | Description                                   |
|-------|----------|-----|-----------------------------------------------|
| 19:16 | YRU      | R/W | Set Up the Units Digit of Years in BCD Format |
| 23:20 | YRT      | R/W | Set Up the Tens Digit of Years in BCD Format  |
| 31:24 | Reserved |     |                                               |

### 19.7.3 RTC control register (RTC\_CTRL)

Offset address: 0x08

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

Note:

- (1) The bits 7, 6 and 4 of this register can be written only in initialization mode.
- (2) It is not recommended to modify this register when the number of hours in the date increases, as it may mask the correct hour increment.
- (3) The written values of STCCFG and WTCCFG will take effect from the next second.
- (4) This register is under write protection.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | WUCLKSEL | R/W | Wakeup Clock Select<br>000: RTC/16<br>001: RTC/8<br>010: RTC/4<br>011: RTC/2<br>10x: clk_spre (usually 1Hz)<br>11x: clk_spre (usually 1Hz) and add 216 to WUAUTORE counter value                                                                                                                                |
| 3     | TSETECFG | R/W | Time Stamp Event Trigger Edge Configure<br>This bit indicates that RTC_TS generates a timestamp event on rising edge or falling edge.<br>0: Rising edge<br>1: Falling edge<br>This bit can be changed only when TSEN=0.                                                                                         |
| 4     | RCLKDEN  | R/W | RTC_REFIN Reference Clock Detection Enable<br>0: Disable<br>1: Enable<br>SPSC must be 0x00FF.                                                                                                                                                                                                                   |
| 5     | RCMCFG   | R/W | Read Calendar Value Mode Configure<br>0: The date value is read from the shadow register, and the shadow register is updated every two RTCCLK cycles<br>1, read the date value from the date register<br>If the clock frequency of APB1 is lower than seven times of RTCCLK frequency, RCMCFG must be set to 1. |
| 6     | TIMEFCFG | R/W | Time Format Configure<br>0: 24-hour/day format<br>1: AM/PM time format                                                                                                                                                                                                                                          |

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|---------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7     | DCALEN  | R/W | Coarse Digital Calibration Enable<br>0: Disable<br>1: Enable<br>Require APSC≥6                                                                                                                                                                                                                                                                     |
| 8     | ALRAEN  | R/W | Alarm A Function Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                 |
| 9     | ALRBEN  | R/W | Alarm B Function Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                 |
| 10    | WUTEN   | R/W | Wakeup Timer Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                     |
| 11    | TSEN    | R/W | Time Stamp Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                       |
| 12    | ALRAIEN | R/W | Alarm A Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                |
| 13    | ALRBIEN | R/W | Alarm B Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                |
| 14    | WUTIEN  | R/W | Wakeup Timer Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                           |
| 15    | TSIEN   | R/W | Time Stamp Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                             |
| 16    | STCCFG  | R/W | Summer Time Change Configure<br>The bit will always be 0 in the reading process; if this bit is set not in the initialization mode, the date time will increase by 1.<br>0: Invalid<br>1: The current time increases by 1 hour to calibrate the summer time variation                                                                              |
| 17    | WTCCFG  | R/W | Winter Time Change Configure<br>The bit will always be 0 in the reading process; if this bit is set not in the initialization mode, and HRx of RCT_TIME register is 0, this bit is invalid, and if HRx is not 0, the date time will decrease by 1.<br>0: Invalid<br>1: The current time increases by 1 hour to calibrate the winter time variation |
| 18    | BAKP    | R/W | Backup Value Setup<br>This bit indicates whether the summer time has changed and is written by the user.                                                                                                                                                                                                                                           |



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                 |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19    | CALOSEL  | R/W | Calibration Output Value Select<br>When CALOEN=1, this bit is used to select the output signal of RTC_CALIB.<br>0: 512Hz<br>1: 1Hz<br>The above frequency is valid when RTCCLK is 32.768kHz and the prescaler is at the default value (APSC=127, SPSC=255). |
| 20    | POLCFG   | R/W | Output Polarity Configure<br>This bit indicates the level state of the pin when ALRAFLG/ALRBFLG/WUTFLG bit is set to 1 (depending on OUTSEL bit).<br>0: High level<br>1: Low level                                                                          |
| 22:21 | OUTSEL   | R/W | Output Way Select<br>This bit is used to select the flag bit associated with RTC_ALARM output.<br>00: Disable<br>01: Alarm A output<br>10: Alarm B output<br>11: Wake-up output                                                                             |
| 23    | CALOEN   | R/W | Calibration Output Enable<br>This bit is used to enable RTC_CAL output.<br>0: Disable<br>1: Enable                                                                                                                                                          |
| 31:24 | Reserved |     |                                                                                                                                                                                                                                                             |

#### 19.7.4 RTC state register (RTC\_STS)

This register (except RTC\_STS[13:8] bit) is in write protection state.

Offset address: 0x0C

Reset value of backup domain: 0x0000 0007

System reset: 0xFFFF XXXX

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                           |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ALRAWFLG | R   | Alarm A Write Occur Flag<br>When ALRAEN=0 for RTC_CTRL, the value of alarm A will change and this bit will be set to 1 by hardware; this bit will be cleared by hardware in initialization mode.<br>0: The alarm A cannot be updated<br>1: The alarm A can be updated |
| 1     | ALRBWFLG | R   | Alarm B Write Occur Flag<br>When ALRBEN=0 for RTC_CTRL, the value of alarm A will change and this bit will be set to 1 by hardware; this bit will be cleared by hardware in initialization mode.<br>0: The alarm B cannot be updated<br>1: The alarm B can be updated |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | WUTWFLG  | R     | <p>Wakeup Timer Write Occur Flag</p> <p>When WUTEN=0 and the value of wake-up timer can be changed, this bit can be set by hardware.</p> <p>0: It is not allowed to update the wake-up timer configuration<br/>1: It is allowed to update the wake-up timer configuration</p>                                                                                                                                                                                                                                                         |
| 3     | SOPFLG   | R     | <p>Shift Operation Pending Occur Flag</p> <p>0: Not occur<br/>1: Occurred</p> <p>When a shift operation is generated by writing to RTC_SHIFT register, this bit will be set to 1 by hardware immediately. After corresponding shift operation is performed, this bit will be cleared by software. It is invalid to write to SOPFLG.</p>                                                                                                                                                                                               |
| 4     | INITSFLG | R     | <p>Initialization State Occur Flag</p> <p>When the "year" field in the date is not "0", this bit will be set by hardware.</p> <p>0: Not occur<br/>1: Occurred</p>                                                                                                                                                                                                                                                                                                                                                                     |
| 5     | RSFLG    | RC_W0 | <p>Registers Synchronization Occur Flag</p> <p>When the content in the date register is copied to the shadow registers (RTC_SUBSEC, RTC_TIME and RTC_DATE), this bit is set to 1 by hardware; when shifting operation is pending (SOPFLG=1) or is in the mode that the shadow register is ignored (RCMCFG=1), this bit is cleared by hardware in initialized mode; or this bit can be cleared by software.</p> <p>This bit is cleared by hardware/software in initialization mode.</p> <p>0: Not synchronized<br/>1: Synchronized</p> |
| 6     | RINITFLG | R     | <p>Register Initialization Occur Flag</p> <p>This bit is set to "1", RTC is in initialization state, and the time, date and prescaler registers can be updated.</p> <p>0: Cannot be initialized<br/>1: Initialized</p>                                                                                                                                                                                                                                                                                                                |
| 7     | INITEN   | R/W   | <p>Initialization Mode Enable</p> <p>0: Free run mode<br/>1: Initialization mode; it is used to program RTC_TIME, RTC_DATE and RTC_PSC. The counter stops counting, and after INITEN is reset, the counter will start counting from a new value.</p>                                                                                                                                                                                                                                                                                  |
| 8     | ALRAFLG  | RC_W0 | <p>Alarm A Match Occur Flag</p> <p>When RTC_TIME and RTC_DATE match the alarm A register RTC_ALRMA, this flag is set by hardware.</p> <p>This flag can be cleared by writing 0 by software.</p>                                                                                                                                                                                                                                                                                                                                       |
| 9     | ALRBFLG  | RC_W0 | <p>Alarm B Match Occur Flag</p> <p>When RTC_TIME and RTC_DATE match the alarm B register RTC_ALRMB, this flag is set by hardware.</p> <p>This flag can be cleared by writing 0 by software.</p>                                                                                                                                                                                                                                                                                                                                       |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                               |
|-------|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10    | WUTFLG   | RC_W0 | Wakeup Timer Occur Flag<br>When the auto refresh counter counts to 0, this bit will be set to 1 by hardware; it is cleared by writing 0 by software.<br>Clear this flag 1.5 RTCCLK cycles before WUTFLG is set to 1 again.                |
| 11    | TSFLG    | RC_W0 | Flag for occurrence of timestamp (Time Stamp Occur Flag)<br>When a timestamp event occurs, this flag is set to 1 by hardware; it is cleared by writing 0 by software.                                                                     |
| 12    | TSOVRFLG | RC_W0 | Time Stamp Overflow Occur Flag<br>When TSFLG=1 and a timestamp event is generated, this flag bit is set to 1 by hardware; it is cleared by writing 0 by software.<br>It is recommended to clear this bit after TSFLG flag bit is cleared. |
| 13    | TP1FLG   | RC_W0 | RTC_TP1FLG Detection Occur Flag<br>When a tamper event is detected in RTC_TP1FLG input, this flag is set to 1 by hardware, and it can be cleared by writing 0 by software.                                                                |
| 14    | TP2FLG   | RC_W0 | RTC_TP2FLG Detection Occur Flag<br>When a tamper event is detected in RTC_TP2FLG input, this flag is set to 1 by hardware, and it can be cleared by writing 0 by software.                                                                |
| 15    | Reserved |       |                                                                                                                                                                                                                                           |
| 16    | RCALPFLG | R     | Recalibration Pending Occur Flag<br>When the software writes to RTC_CAL, this bit is set to 1 automatically, and the RTC_CAL register is locked.<br>This bit will return 0 when other new calibration setting is performed.               |
| 31:17 | Reserved |       |                                                                                                                                                                                                                                           |

### 19.7.5 RTC prescaler reegister (RTC\_PSC)

Offset address: 0x10

Reset value of backup domain: 0x007F 00FF

System reset: 0xFFFF XXXX

The register can only be written in the initialization mode, and the initialization must be completed by two independent write accesses, which is in write protected state.

| Field | Name     | R/W | Description                                                                                   |
|-------|----------|-----|-----------------------------------------------------------------------------------------------|
| 14:0  | SPSC     | R/W | Synchronous Prescaler Coefficient<br>$ck\_spre\ frequency = ck\_apre\ frequency / (SPSC + 1)$ |
| 15    | Reserved |     |                                                                                               |
| 22:16 | APSC     | R/W | Asynchronous Prescaler Coefficient<br>$ck\_apre\ frequency = RTCCLK\ frequency / (APSC + 1)$  |
| 31:23 | Reserved |     |                                                                                               |

### 19.7.6 RTC auto reload register (RTC\_AUTORLD)

Offset address: 0x14

Reset value of backup domain: 0x0000 FFFF

System reset: 0XXXXX XXXX

This register can be written only when WUTEFLG of RTC\_STS is set to 1, and it is in write protection state.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | WUAUTORE | R/W | <p>Wakeup Auto-reload Value Setup</p> <p>When the wake-up counter is waken up (WUTEN=1), this flag bit will be set to 1 in each CLK_WUAUTORE cycle, and CLK_WUAUTORE cycle can be set by WUCLKSEL bit of RTC_CTRL register.</p> <p>When WUCLKSEL[2]=1, the wake-up counter will be set to 17 bits, WUCLKSEL[1] is WUAUTORE[16], and is the most critical bit reloaded to the timer.</p> <p>After WUTEN is set, CLK_WUAUTORE cycle will appear to the first assertion of WUTFLG</p> <p>Disable WUCLKSEL[2:0]=011(RTCCLK/2) from WUAUTORE[15:0] to 0x0000.</p> |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

### 19.7.7 RTC coarse calibration register (RTC\_DCAL)

Offset address: 0x18

Reset value of backup domain: 0x0000 0000

System reset: 0XXXXX XXXX

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | DCAL     | R/W | <p>Digital Calibration</p> <p>DCALCFG=0 (positive calibration)</p> <p>00000: + 0 ppm</p> <p>00001: + 4 ppm (rounded-off value)</p> <p>00010: + 8 ppm (rounded-off value)</p> <p>..</p> <p>11111: + 126 ppm (rounded-off value)</p> <p>DCALCFG=1 (negative calibration)</p> <p>00000: - 0 ppm</p> <p>00001: - 2 ppm (rounded-off value)</p> <p>00010: - 4 ppm (rounded-off value)</p> <p>..</p> <p>11111: - 63ppm (rounded-off value)</p> |
| 6:5   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 7     | DCALCFG  | R/W | <p>Digital Calibration Configure</p> <p>0: Positive calibration - increase the date update frequency</p> <p>1: Negative calibration - decrease the date update frequency</p>                                                                                                                                                                                                                                                             |
| 31:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### 19.7.8 RTC alarm A register (RTC\_ALRMA)

Offset address: 0x1C

Reset value of backup domain: 0x0000 0000

System reset: 0XXXXX XXXX

This register can be written only when ALRWFLG of RTC\_STS is set to 1 or in initialization mode, and it is in write protection state.

| Field | Name     | R/W | Description                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | SECU     | R/W | Set Up the Units Digit of Seconds in BCD Format                                                                               |
| 6:4   | SECT     | R/W | Set Up the Tens Digit of Seconds in BCD Format                                                                                |
| 7     | SECMEN   | R/W | Alarm A Seconds Mask Enable<br>0: If the "second" matches, set Alarm A<br>1: Mask the effect of the "second" value on Alarm A |
| 11:8  | MINU     | R/W | Set Up the Units Digit of Minutes in BCD Format                                                                               |
| 14:12 | MINT     | R/W | Set Up the Tens Digit of Minutes in BCD Format                                                                                |
| 15    | MINMEN   | R/W | Alarm A Minutes Mask Enable<br>0: If the "minute" matches, set Alarm A<br>1: Mask the effect of the "minute" value on Alarm A |
| 19:16 | HRU      | R/W | Set Up the Units Digit of Hours in BCD Format                                                                                 |
| 21:20 | HRT      | R/W | Set Up the Tens Digit of Hours in BCD Format                                                                                  |
| 22    | TIMEFCFG | R/W | Time Format Configure<br>0: AM or 24-hour system<br>1: PM                                                                     |
| 23    | HRMEN    | R/W | Alarm A Hours Mask Enable<br>0: If the "hour" matches, set Alarm A<br>1: Mask the effect of the "hour" value on Alarm A       |
| 27:24 | DAYU     | R/W | Set Up the Units Digit of Days in BCD Format                                                                                  |
| 29:28 | DAYT     | R/W | Set Up the Tens Digit of Days in BCD Format                                                                                   |
| 30    | WEEKSEL  | R/W | Week Day Select<br>0: DAYU means date<br>1: DAYU means the number of weeks. DAYT has no effect.                               |
| 31    | DATEMEN  | R/W | Alarm A Date Mask Enable<br>0: If the date/week matches, set Alarm A<br>1: Mask the effect of the date/week value on Alarm A  |

### 19.7.9 RTC alarm B register (RTC\_ALRMB)

Offset address: 0x20

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

This register can be written only when ALRWFLG of RTC\_STS is set to 1 or in initialization mode, and it is in write protection state.

| Field | Name   | R/W | Description                                                                                                                   |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | SECU   | R/W | Set Up the Units Digit of Seconds in BCD Format                                                                               |
| 6:4   | SECT   | R/W | Set Up the Tens Digit of Seconds in BCD Format                                                                                |
| 7     | SECMEN | R/W | Alarm B Seconds Mask Enable<br>0: If the "second" matches, set Alarm B<br>1: Mask the effect of the "second" value on Alarm B |

| Field | Name     | R/W | Description                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 11:8  | MINU     | R/W | Set Up the Units Digit of Minutes in BCD Format                                                                               |
| 14:12 | MINT     | R/W | Set Up the Tens Digit of Minutes in BCD Format                                                                                |
| 15    | MINMEN   | R/W | Alarm B Minutes Mask Enable<br>0: If the "minute" matches, set Alarm B<br>1: Mask the effect of the "minute" value on Alarm B |
| 19:16 | HRU      | R/W | Set Up the Units Digit of Hours in BCD Format                                                                                 |
| 21:20 | HRT      | R/W | Set Up the Tens Digit of Hours in BCD Format                                                                                  |
| 22    | TIMEFCFG | R/W | Time Format Configure<br>0: AM or 24-hour system<br>1: PM                                                                     |
| 23    | HRMEN    | R/W | Alarm B Hours Mask Enable<br>0: If the "hour" matches, set Alarm B<br>1: Mask the effect of the "hour" value on Alarm B       |
| 27:24 | DAYU     | R/W | Set Up the Units Digit of Days in BCD Format                                                                                  |
| 29:28 | DAYT     | R/W | Set Up the Tens Digit of Days in BCD Format                                                                                   |
| 30    | WEEKSEL  | R/W | Week Day Select<br>0: DAYU means date<br>1: DAYU means the number of weeks. DAYT has no effect.                               |
| 31    | DATEMEN  | R/W | Alarm B Date Mask Enable<br>0: If the date/week matches, set Alarm B<br>1: Mask the effect of the date/week value on Alarm B  |

#### 19.7.10 RTC write protection register (RTC\_WRPROT)

Offset address: 0x24

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                 |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------|
| 7:0   | KEY      | W   | Write Protection Key Value Setup<br>This byte is written by software; read this byte and it is always 0x00. |
| 31:8  | Reserved |     |                                                                                                             |

#### 19.7.11 RTC subsecond register (RTC\_SUBSEC)

Offset address: 0x28

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | SUBSEC | R   | Sub Second Value Setup<br>SUBSEC is the value of synchronous prescaler counter. It is determined by the following formula:<br>$\text{Subsecond value} = (\text{SPSC} - \text{SUBSEC}) / (\text{SPSC} + 1)$<br>After one shift operation is performed, SUBSEC may be greater than SPSC. The correct time/date is one second less than RTC_TIME/RTC_DATE. |

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 31:16 | Reserved |     |             |

### 19.7.12 RTC shift register (RTC\_SHIFT)

Offset address: 0x2C

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

This register is in write protection state.

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:0  | SFSEC     | W   | <p>Subtract a Fraction of a Second Setup</p> <p>This bit field can only be written; read this byte and it is always 0. Writing to this bit is invalid while an operation is being executed.</p> <p>The set SFSEC value will be added to the synchronous prescaler counter. If the counter counts down, the clock will be delayed, and the delay time is determined by the following formula:</p> $\text{Delay (seconds)} = \text{SFSEC} / (\text{SPSC} + 1)$ <p>When it takes effect at the same time with ADD1SECEN, the advance clock will be added by a fraction of a second; the specific added value is determined by the following formula:</p> $\text{Advance (seconds)} = (1 - (\text{SFSEC} / (\text{SPSC} + 1)))$ <p>Conduct write operation to this bit and RSFLG bit can be cleared. The software keeps running until RSFLG is set to 1 to ensure that the value of the shadow register is synchronized with the shift time.</p> |
| 30:15 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 31    | ADD1SECEN | W   | <p>Add One Second Enable</p> <p>0: Not added</p> <p>1: The clock/date increases by one second</p> <p>This bit can only be written; read this byte and it is always 0. Writing to this bit is invalid while an operation is being executed.</p> <p>When it takes effect at the same time with SFSEC, it can increase the value of the clock by several tenths of a second.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 19.7.13 RTC timestamp time register (RTC\_TSTIME)

Offset address: 0x30

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

This register is valid only when TSFLG of RTC\_STS is set to 1. When TSFLG bit is reset, the content of this register will be cleared.

| Field | Name     | R/W | Description                                     |
|-------|----------|-----|-------------------------------------------------|
| 3:0   | SECU     | R   | Set Up the Units Digit of Seconds in BCD Format |
| 6:4   | SECT     | R   | Set Up the Tens Digit of Seconds in BCD Format  |
| 7     | Reserved |     |                                                 |
| 11:8  | MINU     | R   | Set Up the Units Digit of Minutes in BCD Format |
| 14:12 | MINT     | R   | Set Up the Tens Digit of Minutes in BCD Format  |

| Field | Name     | R/W | Description                                               |
|-------|----------|-----|-----------------------------------------------------------|
| 15    | Reserved |     |                                                           |
| 19:16 | HRU      | R   | Set Up the Units Digit of Hours in BCD Format             |
| 21:20 | HRT      | R   | Set Up the Tens Digit of Hours in BCD Format              |
| 22    | TIMEFCFG | R   | Time Format Configure<br>0: AM or 24-hour system<br>1: PM |
| 31:23 | Reserved |     |                                                           |

#### 19.7.14 RTC timestamp date register (RTC\_TSDATE)

Offset address: 0x34

Reset value of backup domain: 0x0000 0000

System reset: 0XXXXX XXXX

This register is valid only when TSFLG bit of RTC\_STS is set to 1. When TSFLG bit is reset, this register will be cleared.

| Field | Name     | R/W | Description                                                                |
|-------|----------|-----|----------------------------------------------------------------------------|
| 3:0   | DAYU     | R   | Set Up the Units Digit of Days in BCD Format                               |
| 5:4   | DAYT     | R   | Set Up the Tens Digit of Days in BCD Format                                |
| 7:6   | Reserved |     |                                                                            |
| 11:8  | MONU     | R   | Set Up the Units Digit of Months in BCD Format                             |
| 12    | MONT     | R   | Set Up the Tens Digit of Months in BCD Format                              |
| 15:13 | WEEKSEL  | R   | Week Day Units Select<br>000: Disable<br>001: Monday<br>...<br>111: Sunday |
| 31:16 | Reserved |     |                                                                            |

#### 19.7.15 RTC timestamp subsecond register (RTC\_TSSUBSEC)

Offset address: 0x38

Reset value of backup domain: 0x0000 0000

System reset: 0XXXXX XXXX

This register is valid only when TSFLG bit of RTC\_STS register is set to 1. When TSFLG bit is reset, the content of this register will be cleared.

| Field | Name     | R/W | Description                                                                                                           |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------|
| 15:0  | SUBSEC   | R   | Sub Second Value Setup<br>When a timestamp event occurs, SUBSEC [15:0] is the value in synchronous prescaler counter. |
| 31:16 | Reserved |     |                                                                                                                       |

#### 19.7.16 RTC precision calibration register (RTC\_CAL)

Offset address: 0x3C



Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

This register is in write protection state.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:0   | RECALF   | R/W | Reduced Calibration Frequency<br>Reduced date frequency: Mask RECALF pulses within $2^{20}$ RTCCLK pulses (32sec if the output frequency is 32768 Hz) and the date frequency will be reduced (the resolution is 0.9537 ppm).<br>Increased date frequency: It takes effect at the same time with ICALFEN                                                                                                                                                        |
| 12:9  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 13    | CAL16CFG | R/W | 16 Second Calibration Cycle Period Configure<br>When CAL16CFG is set to 1, 16-second calibration cycle is used, and it cannot be set to 1 at the same time with CAL8CFG bit.<br>When CAL16CFG=1, RECALF [0] is always 0.                                                                                                                                                                                                                                       |
| 14    | CAL8CFG  | R/W | 8 Second Calibration Cycle Period Configure<br>When CAL8CFG is set to 1, 8-second calibration cycle is used, and it cannot be set to 1 at the same time with CAL16CFG bit.<br>When CAL8CFG=1, RECALF [1:0] is always 00.                                                                                                                                                                                                                                       |
| 15    | ICALFEN  | R/W | Increase Calibration Frequency Enable<br>0: RTCCLK pulse is not increased<br>1: One RTCCLK pulse is increased (the frequency increases by 488.5 ppm) every $2^{11}$ pulses<br>It takes effect at the same time with RECALF, and when the resolution is high, the date frequency will be reduced. If the input frequency is 32768Hz, the number of RTCCLK pulses added in the 32-second window is determined by the following formula:<br>(512*ICALFEN)–RECALF。 |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 19.7.17 RTC tamper and multiplexing configuration register (RTC\_TACFG)

Offset address: 0x40

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                           |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TP1EN    | R/W | RTC_TAMP1 Input Detection Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                           |
| 1     | TP1ALCFG | R/W | RTC_TAMP1 Input Active Level Configure<br>When TPFCSSEL!=00, this bit determines that RTC_TAMP1 will trigger an tamper detection event when the input maintains high/low level.<br>0: Low level<br>1: High level<br>When TPFCSSEL=00, this bit determines that RTC_TAMP1 triggers an tamper detection event when the input is on rising/falling edge. |

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |           |     | 0: Rising edge<br>1: Falling edge                                                                                                                                                                                                                                                                                                                                                                                                      |
| 2     | TPIEN     | R/W | Tamper Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                     |
| 6:3   | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7     | TPTSEN    | R/W | Tamper Detection Event Timestamp Enable<br>This bit determines whether the timestamp generated by the tamper detection event is saved<br>0: Not saved<br>1: Saved<br>This bit is still valid when TSEN=0 for RTC_CTRL register.                                                                                                                                                                                                        |
| 10:8  | TPSFSEL   | R/W | Tamper Sampling Frequency Select<br>These bits determine the sampling frequency of each input of RTC_TAMPx.<br>0x0: RTCCLK/32768<br>0x1: RTCCLK/16384<br>0x2: RTCCLK/8192<br>0x3: RTCCLK/4096<br>0x4: RTCCLK/2048<br>0x5: RTCCLK/1024<br>0x6: RTCCLK/512<br>0x7: RTCCLK/256                                                                                                                                                            |
| 12:11 | TPFCSEL   | R/W | RTC_TAMPx Filter Count Select<br>These bits determine the number of sampling times after which the tamper event is activated on specific level (TAMP*TRG).<br>TPFCSEL is valid for each input of RTC_TAMPx.<br>0x0: Activate the tamper event on the edge where RTC_TAMPx input is converted into valid level<br>0x1: Continuous sampling twice<br>0x2: Continuous sampling for four times<br>0x3: Continuous sampling for eight times |
| 14:13 | TPPRDUSEL | R/W | RTC_TAMPx Precharge Duration Select<br>These bits determine the number of RTCCLK cycles which are enabled by pull-up resistor before sampling; which is valid in each input of RTC_TAMPx.<br>0x0: 1<br>0x1: 2<br>0x2: 4<br>0x3: 8                                                                                                                                                                                                      |
| 15    | TPPUDIS   | R/W | RTC_TAMPx Pull-up Function Disable<br>This bit determines whether all RTC_TAMPx pins are precharged before sampling.<br>0: Enable (internal pull-up is enabled)<br>1: Disable                                                                                                                                                                                                                                                          |
| 16    | TP1MSEL   | R/W | RTC_TAMP1 Mapping Select<br>0: RTC_AF1 is used as RTC_TAMP1                                                                                                                                                                                                                                                                                                                                                                            |

| Field | Name     | R/W | Description                                                                                                                                                                                        |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 1: Reserved<br>The default value is 0; other values may cause abnormal mapping of RTC_TAMP1.<br>Note: When this bit is changed, TP1EN must be reset, so as to avoid unnecessary setting of TP1FLG. |
| 17    | TSMSEL   | R/W | Timestamp Mapping Select<br>0: RTC_AF1 is used as timestamp<br>1: Reserved<br>The default value is 0; other values may cause abnormal timestamp mapping.                                           |
| 18    | ALRMOT   | R/W | RTC_ALARM Output Type Configure<br>0: Open-drain output<br>1: Push-pull output                                                                                                                     |
| 31:19 | Reserved |     |                                                                                                                                                                                                    |

### 19.7.18 RTC alarm A subsecond register (RTC\_ALRMASS)

Offset address: 0x44

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

This register can be written only when ALRAEN bit of RTC\_CTRL is reset or in initialization mode, and it will be in write protection state.

This register is in write protection state.

| Field | Name     | R/W | Description                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:0  | SUBSEC   | R/W | Sub Second Value Setup<br>The subsecond value is compared with the value in the synchronous prescaler counter to determine whether to activate the alarm A, and only the bits from 0 to MASKSEL-1 are compared. |
| 23:15 | Reserved |     |                                                                                                                                                                                                                 |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27:24 | MASKSEL  | R/W | <p>Mask the Most-significant Bits Starting at This Bit Select</p> <p>0x0: Alarm A is not compared. The alarm is set when the second unit increases by 1</p> <p>0x1: When comparing with alarm A, SUBSEC[14:1] is not involved, and only SUBSEC[0] is involved</p> <p>0x2: When comparing with alarm A, SUBSEC[14:2] is not involved, and only SUBSEC[1:0] is involved</p> <p>0x3: When comparing with alarm A, SUBSEC[14:3] is not involved, and only SUBSEC[2:0] is involved</p> <p>...</p> <p>0xC: When comparing with alarm A, SUBSEC[14:12] is not involved, and only SUBSEC[11:0] is involved</p> <p>0xD: When comparing with alarm A, SUBSEC[14:13] is not involved, and only SUBSEC[12:0] is involved</p> <p>0xE: When comparing with alarm A, SUBSEC[14] is not involved, and only SUBSEC[13:0] is involved</p> <p>0xE: When comparing the alarm A, 15 SUBSEC bits all take part in, and the alarm can be activated only when all of them match.</p> <p>The synchronous counter overrun bit (Bit 15) is never compared. This bit is not 0 only after shift operation.</p> |
| 31:28 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

### 19.7.19 RTC alarm B subsecond register (RTC\_ALRMBSS)

Offset address: 0x48

Reset value of backup domain: 0x0000 0000

System reset: 0xFFFF XXXX

This register can be written only when ALRBEN bit of RTC\_CTRL is reset or in initialization mode, and it will be in write protection state.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:0  | SUBSEC   | R/W | <p>Sub Second Value Setup</p> <p>The subsecond value is compared with the value in the synchronous prescaler counter to determine whether to activate the alarm B, and only the bits from 0 to MASKSEL-1 are compared.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 23:15 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 27:24 | MASKSEL  | R/W | <p>Mask the Most-significant Bits Starting at This Bit Select</p> <p>0x0: Alarm B is not compared. The alarm is set when the second unit increases by 1</p> <p>0x1: When comparing with alarm B, SUBSEC[14:1] is not involved, and only SUBSEC[0] is involved</p> <p>0x2: When comparing with alarm B, SUBSEC[14:2] is not involved, and only SUBSEC[1:0] is involved</p> <p>3: When comparing with alarm B, SUBSEC[14:3] is not involved, and only SUBSEC[2:0] is involved</p> <p>...</p> <p>0xC: When comparing with alarm B, SUBSEC[14:12] is not involved, and only SUBSEC[11:0] is involved</p> <p>0xD: When comparing with alarm B, SUBSEC[14:13] is not involved, and only SUBSEC[12:0] is involved</p> |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | <p>0xE: When comparing with alarm B, SUBSEC[14] is not involved, and only SUBSEC[13:0] is involved</p> <p>0xE: When comparing the alarm B, 15 SUBSEC bits all take part in, and the alarm can be activated only when all of them match.</p> <p>The synchronous counter overrun bit (Bit 15) is never compared. This bit is not 0 only after shift operation.</p> |
| 31:28 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                  |

### 19.7.20 RTC backup register (RTC\_BAKPx) (x=0-19)

Offset address: 0x50-0x9C

Reset value of backup domain: 0x0000 0000

Reset value: 0xFFFF XXXX

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | BAKP | R/W | <p>Backup Value Setup</p> <p>V<sub>BAT</sub> will supply power after V<sub>DD</sub> power supply is cut off, so this bit field is unaffected by system reset; when a tamper detection event occurs or the flash memory read protection is disabled, this register will be reset, and it will remain reset as long as TP1FLG=1.</p> <p>The contents of this bit field are valid even if the device is running in low-power mode.</p> |

## 20 Universal Synchronous/Asynchronous Transceiver (USART)

### 20.1 Full name and abbreviation description of terms

Table 82 Full name and abbreviation description of terms

| Full name in English  | English abbreviation |
|-----------------------|----------------------|
| Clear to Send         | CTS                  |
| Request to Send       | RTS                  |
| Most Significant Bit  | MSB                  |
| Least Significant Bit | LSB                  |
| Guard                 | GRD                  |
| Overrun               | OVR                  |

### 20.2 Introduction

USART (universal synchronous/asynchronous transceiver) is a serial communication device that can flexibly exchange full-duplex and half-duplex data with external devices, and meets the requirements of external devices for industry standard NRZ asynchronous serial data format. USART also provides a wide range of baud rate for selection and supports multiprocessor communication.

USART not only supports standard asynchronous transceiver mode, but also supports some other serial data exchange modes, such as LIN protocol, smart card protocol, IrDA SIR ENDEC specification and hardware flow control mode.

USART also supports DMA function to realize high-speed data communication.

### 20.3 Main characteristics

- (1) Full duplex asynchronous communication
- (2) Single-line half-duplex communication
- (3) NRZ standard format
- (4) Characteristics of programmable serial port:
  - Data bit: 8 or 9 bits
  - Check bits: Even parity check, odd parity check, no check
  - Support 0.5, 1, 1.5 and 2 stop bits
- (5) Check control

- Transmit the parity bit
- Check the received data
- (6) Select speed and clock tolerance with programmable 8 or 16-time oversampling rate
- (7) Independent transmitter and receiver enable bit
- (8) Programmable baud rate generator
- (9) Multiprocessor communication:
  - If the address does not match, it will enter the mute mode
  - Wake up from mute mode through idle bus detection or address flag detection
- (10) Synchronous transmission mode
- (11) Generation and detection of LIN break frame
- (12) Support the smart card interface of ISO7816-3 standard
- (13) Support IrDA protocol
- (14) Support hardware flow control
- (15) DMA can be used for continuous communication
- (16) State flag bit:
  - Transmission detection flag: The transmit register is empty, the receive register is not empty, and transmission is completed
  - Error detection flag: Overrun error, noise error, parity error, frame error
- (17) Multiple interrupt sources:
  - The transmit register is empty
  - Transmission is completed
  - CTS changed
  - The receive register cannot be empty
  - Overload error
  - Bus idle
  - Parity error
  - LIN disconnection detection
  - Noise error
  - Overrun error
  - Frame error

## 20.4 Functional description

Table 83 USAR Pin Description

| Pin        | Type                                             | Description                                                                                                 |
|------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| USART_RX   | Input                                            | Data receiving                                                                                              |
| USART_TX   | Output<br>I/O (single-line mode/smart card mode) | Data transmission<br>It is high level by default when the transmitter is enabled and does not transmit data |
| USART_CK   | Output                                           | Clock output                                                                                                |
| USART_nRTS | Output                                           | Request to send in hardware flow control mode                                                               |
| USART_nCTS | Input                                            | Clear to send in hardware flow control mode                                                                 |
| IrDA_RDI   | Input                                            | Data input in IrDA mode                                                                                     |
| IrDA_TDO   | Output                                           | Data output in IrDA mode                                                                                    |

### 20.4.1 Single-line half-duplex communication

HDEN bit of USART\_CTRL3 register determines whether to enter the single-line half-duplex mode.

When USART enters single-line half-duplex mode:

- The CLKEN and LINMEN bit of USART\_CTRL2 register, and IREN and SCEN bits of USART\_CTRL3 register must be cleared.
- RX pin is disabled.
- TX pin should be configured as open-drain output and connected with RX pin inside the chip.
- Transmitting data and receiving data can not be carried out at the same time. The data cannot be received before they are sent. If needing to receive data, enabling receiving can be turned on only after TXCFLG bit of USART\_STS register is set to 1.
- If there is data collision on the bus, software management is needed to allocate the communication process.

### 20.4.2 Frame format

The frame format of data frame is controlled by USART\_CTRL1 register:

- DBLCFG bit controls the character length, which can be set to 8 or 9 bits.
- PCEN bit controls to enable the parity bit or not.
- PCFG bit controls the parity bit to be odd or even.

Table 84 Frame Format

| DBLCFG bit | PCEN bit | USART data frame              |
|------------|----------|-------------------------------|
| 0          | 0        | Start bit+8-bit data+stop bit |



| DBLCFG bit | PCEN bit | USART data frame                                        |
|------------|----------|---------------------------------------------------------|
| 0          | 1        | Start bit+7-bit data+odd-even parity check bit+stop bit |
| 1          | 0        | Start bit+9-bit data+stop bit                           |
| 1          | 1        | Start bit+8-bit data+odd-even parity check bit+stop bit |

### Configurable stop bit

Four different stop bits can be configured through STOPCFG bit of USART\_CTRL2 register.

- 1 stop bits: Default stop bit.
- 0.5 stop bits: Used when receiving data in smart card mode.
- 2 stop bits: Used in normal mode, single-line mode and hardware flow control mode.
- 1.5 stop bits: Used when transmitting and receiving data in smart card mode.

### Parity bit

PCFG bit of USART\_CTRL1 determines the parity check bit; when PCFG=0, it is even parity check, on the contrary, it is odd parity check.

- Even parity check: When the number of frame data and parity bit 1 is even, the even parity bit is 0; otherwise, it is 1.
- Odd parity check: When the number of frame data and parity bit 1 is even, the odd parity bit is 1; otherwise, it is 0.

## 20.4.3 Transmitter

When TXEN bit of the register USART\_CTRL1 is set, the transmit shift register will output data through TX pin and the corresponding clock pulses will be output through CK pin.

### 20.4.3.1 Character transmitting

During transmitting period of USART, the least significant bit of the data will be moved out by TX pin first. In this mode, USART\_DATA register has a buffer between the internal bus and the transmitter shift register.

A data frame is composed of the start bit, character and stop bit, so there is a low-level start bit in front of each character; then there is a high-level stop bits the number of which is configurable.

### Transmission configuration steps

- (1) Set UEN bit of USART\_CTRL1 register to enable USART.
- (2) Decide the word length by setting DBLCFG bit of USART\_CTRL1 register.

- (3) Decide the number of stop bits by setting STOPCFG bit of USART\_CTRL2 register.
- (4) If multi-buffer communication is selected, DMA should be enabled in USART\_CTRL3 register.
- (5) Set the baud rate of communication in USART\_BR register.
- (6) Enable TXEN bit in USART\_CTRL1 register, and transmit an idle frame.
- (7) Wait for TXBEFLG bit of USART\_STS register to be set to 1.
- (8) Write data to USART\_DATA register (if DMA is not enabled, repeat steps 7-8 for each byte to be sent).
- (9) Wait for TXCFLG bit of USART\_STS register to be set to 1, indicating transmission completion.

Note: TXEN bit cannot be reset during data transmission; otherwise, the data on TX pin will be destroyed, which is because if the baud rate generator stops counting, the data being transmitted will be lost.

#### 20.4.3.2 Single-byte communication

TXBEFLG bit can be cleared by writing USART\_DATA register. When the TXBEFLG bit is set by hardware, the shift register will receive the data transferred from the data transmit register, then the data will be transmitted, and the data transmit register will be cleared. The next data can be written in the data register without covering the previous data.

- (1) If TXBEIEN in USART\_CTRL1 register is set to 1, an interrupt will be generated.
- (2) If USART is in the state of transmitting data, write to the data register to save the data to the DATA register, and transfer the data to the shift register at the end of the current data transmission.
- (3) If USART is in idle state, write to the data register, put the data into the shift register, start transmitting data, and set TXBEFLG bit to 1.
- (4) When a data transmission is completed and TXBEFLG bit is set, TXCFLG bit will be set to 1; at this time if TXCIEN bit in USART\_CTRL1 register is set to 1, an interrupt will be generated.
- (5) After the last data is written in the USART\_DATA register, before entering the low-power mode or before closing the USART module, wait to set TXCFLG to 1.

#### 20.4.3.3 Break frame

The break frames are considered to receive 0 in a frame period. Setting TXBF bit of USART\_CTRL1 register can transmit a break frame, and the length of the break frame is determined by DBLCFG bit of USART\_CTRL1 register. If the

TXBF bit is set, after completion of transmission of current data, the TX line will transmit a break frame, and after completion of transmission of break frame, the TXBF bit will be reset. At the end of the break frame, the transmitter inserts one or two stop bits to respond to the start bit.

Note: If the TXBF bit is reset before transmission of the break frame starts, the break frame will not be transmitted. To transmit two consecutive break frames, the TXBF bit should be set after the stop bit of the previous disconnection symbol.

#### 20.4.3.4 Idle frame

The idle frame is regarded as a complete data frame composed entirely of 1, followed by the start bit of the next frame containing the data. Set TXEN bit of USART\_CTRL1 register to 1 and one idle frame can be set before the first data frame.

### 20.4.4 Receiver

#### 20.4.4.1 Character receiving

During receiving period of USART, RX pin will first introduce the least significant bit of the data. In this mode, USART\_DATA register has a buffer between the internal bus and the receive shift register. The data is transmitted to the buffer bit by bit. When fully receiving the data, the corresponding receive register is not empty, then the user can read USART\_DATA.

#### Receiving configuration steps

- (1) Set UEN bit of USART\_CTRL1 register to enable USART.
- (2) Decide the word length by setting DBLCFG bit of USART\_CTRL1 register.
- (3) Decide the number of stop bits by setting STOPCFG bit of USART\_CTRL2 register.
- (4) If multi-buffer communication is selected, DMA should be enabled in USART\_CTRL3 register.
- (5) Set the baud rate of communication in USART\_BR register.
- (6) Set RXEN bit of USART\_CTRL1 to enable receiving.

Note:

- (1) RXEN bit cannot be reset during data receiving period; otherwise, the bytes being received will be lost.
- (2) In the process when the receiver is receiving a data frame, if overrun error, noise error or frame error is detected, the error flag will be set to 1.
- (3) When data is transferred from the shift register to USART\_DATA register, the RXBNEFLG bit of USART\_STS will be set by hardware.

- (4) An interrupt will be generated if RXBNEIEN bit is set.
- (5) In single buffer mode, the RXBNEFLG bit can be cleared by reading USART\_DATA register by software or by writing 0.
- (6) In multi-buffer mode, after each byte is received, RXBNEFLG bit of USART\_STS register will be set to 1, and DMA will read the data register to clear it.

#### 20.4.4.2 Break frame

When the receiver receives a break frame, USART will handle it as receiving a frame error.

#### 20.4.4.3 Idle frame

When the receiver receives an idle frame, USART will handle it as receiving an ordinary data frame; if IDLEIEN bit of USART\_CTRL1 is set, an interrupt will be generated.

#### 20.4.4.4 Oversampling rate

OSMCFG bit of USART\_CTRL1 register determines the oversampling rate.

If the oversampling rate is 8 times of the baud rate, the speed is higher, but the clock tolerance is smaller. If it is 16 times, the speed is lower, but the clock tolerance is bigger.

#### 20.4.4.5 Overrun error

If the RXBNEFLG bit in the USART\_STS register is set to 1 and a new character is received simultaneously, an overflow error will occur. Data can only be transferred from the shift register to the DATA register after the RXEN is reset. After receiving a byte, the RXBNEFLG bit will be set to 1; this bit must be cleared before receiving the next data or before the previous DMA request is processed, otherwise an overflow error will occur.

##### When an overrun error occurs

- USART\_STS OVREFLG bit set to 1.
- The data in DATA register will not be lost.
- The data in the shift register received before will be overwritten, but the data received later will not be saved.
- If RXBNEIEN bit of USART\_CTRL1 is set to 1, an interrupt will be generated.
- When OVREFLG bit is set to 1, it means that the data has been lost. There are two possibilities:
  - When RXBNEFLG=1, the previous valid data is still on DATA register, and can be read.
  - When RXBNEFLG=0, there is no valid data in DATA register.
- The OVREFLG bit can be reset through read operation for USART\_STS and USART\_DATA registers.

#### 20.4.4.6 Noise error

When noise is detected in receiving process of the receiver:

- Set NE flag on the rising edge of RXBNEFLG bit of USART\_STS register.
- Invalid data is transmitted from the shift register to USART\_DATA register.

Note: 8-time oversampling ratio cannot be used in LIN, smart card and IrDA modes.

#### 20.4.4.7 Frame error

If the stop bit is not received and recognized at the expected receiving time due to excessive noise or lack of synchronization, a frame error will be detected.

When a frame error is detected in receiving process of the receiver:

- (1) Set the FEFLG bit of USART\_STS register.
- (2) Invalid data is transmitted from the shift register to USART\_DATA register.
- (3) In single byte communication, there is no interrupt, but in multi-buffer communication, an interrupt will be generated by setting the ERRIEN bit of USART\_CTRL3 register.

#### 20.4.5 Baud rate generator

The baud rate division factor (USARTDIV) is a 16-digit number consisting of 12-digit integer part and 4-digit decimal part. The relationship of Tx/Rx baud rate and the system clock:

Formula 1 Baud rate in smart card, LIN and IrDA modes

$$\text{Baud rate} = \text{PCLK} / 16 \times (\text{USARTDIV}) \quad (\text{Formula 1})$$

Formula 2 applies to the baud rate of standard USART (including SPI mode)

$$\text{Baud rate} = \text{PCLK} / (8 \times (2 - \text{OVER8}) \times \text{USARTDIV}) \quad (\text{Formula 2})$$

The system clock of USART2/3 is PCLK1, and that of USART1 is PCLK2. USART can be enabled only after the clock control unit enables the system clock.

Example 1:

If IBR = 0d20 and IBR = 0d12 (USART\_BRR = 0x14C)

The mantissa (USARTDIV) = 0d20

Decimal (USARTDIV) = 12/16 = 0.75

So USARTDIV = 0d20.75

## 20.4.6 Multi-processor communication

In multi-processor communication, multiple USARTs are connected to form a network. In this network, two devices communicate with each other, and the mute mode can be enabled for other devices not participating in the communication in order to reduce the burden of USART. In mute mode, no receive state bit will be set and all receive interrupts are disabled.

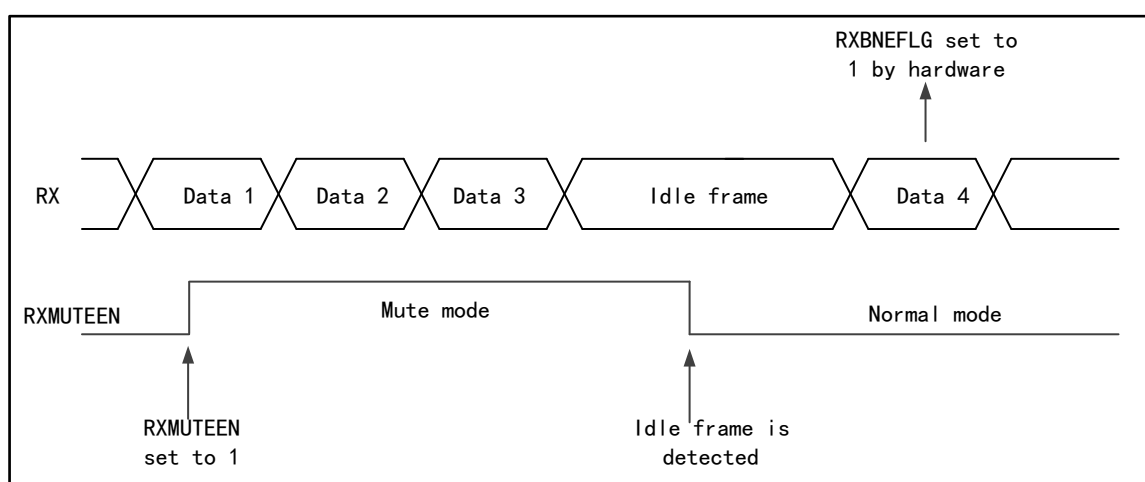
When mute mode is enabled, there are two ways to exit the mute mode:

- WUPMCFG bit is cleared and the bus is idle to exit the mute mode.
- WUPMCFG bit is set and after receiving the address flag, it can exit the mute mode.

### Idle bus detection (WUPMCFG=0)

When RXMUTEEN is set to 1, USART enters the mute mode, and it can be waken up from the mute mode when an idle frame is detected. Meanwhile, the RXMUTEEN bit will be cleared by the hardware. RXMUTEEN can also be cleared by software.

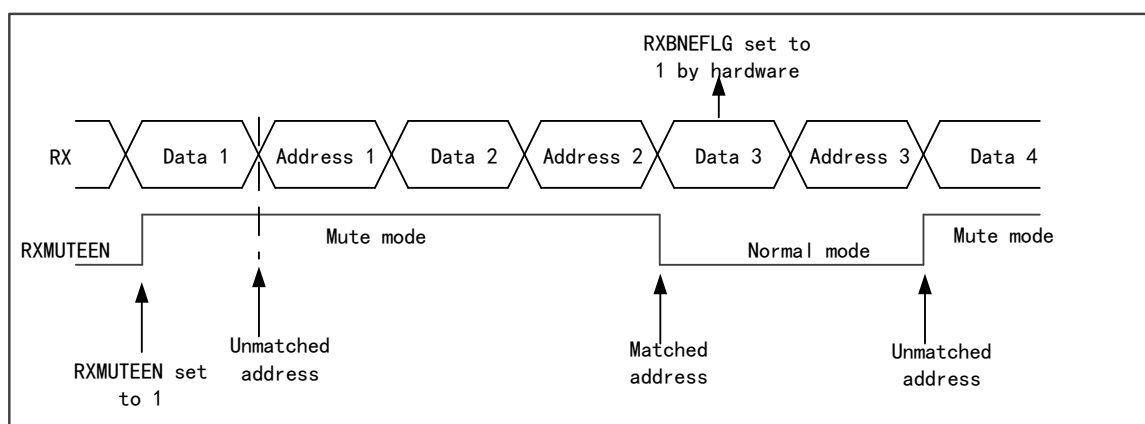
Figure 67 Idle Bus Exit Mute Mode



### Address flag detection (WUPMCFG=1)

If the address flag bit is 1, this byte is regarded as the address. The storage address of lower four bits of the address bytes will first be compared with its own address when the receiver receives the address byte. If the addresses do not match, the receiver will enter the mute mode. If the addresses match, the receiver will wake up from the mute mode and be ready to receive the next byte. If the address byte is received again after exiting the mute mode, but the address does not match its own address, the receiver will enter the mute mode again.

Figure 68 Address Flag Exit Mute Mode



## 20.4.7 Synchronous mode

The synchronous mode supports full duplex synchronous serial communication in master mode, and has one more signal line USART\_CK which can output synchronous clock than the asynchronous mode.

CLKEN bit of USART\_CTRL2 register decides whether to enter the synchronous mode.

When USART enters the synchronous mode:

- The LINMEN bit of USART\_CTRL2 register, and IREN, HDEN and SCEN bits of USART\_CTRL3 register must be cleared.
- The start bit and stop bit of data frame have no clock output.
- Whether the last data bit of data frame generates USART\_CK clock is decided by the LBCPOEN bit of USART\_CTRL2 register.
- The clock polarity of USART\_CK is decided by CPOL bit of USART\_CTRL2 register.
- The phase of USART\_CK is decided by the CPHA bit of USART\_CTRL2.
- The external CK clock cannot be activated when the bus is idle or the frame is disconnected.

Figure 69 USART Synchronous Transmission Example

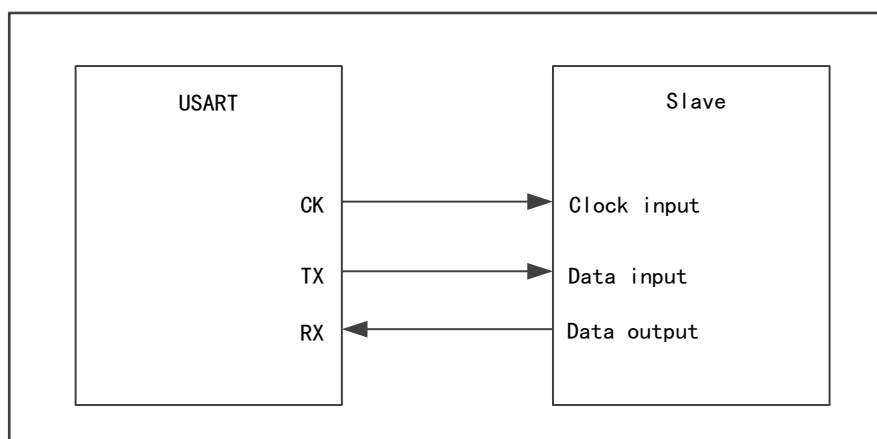


Figure 70 USART Synchronous Transmission Timing Diagram (DBLCFG=0)

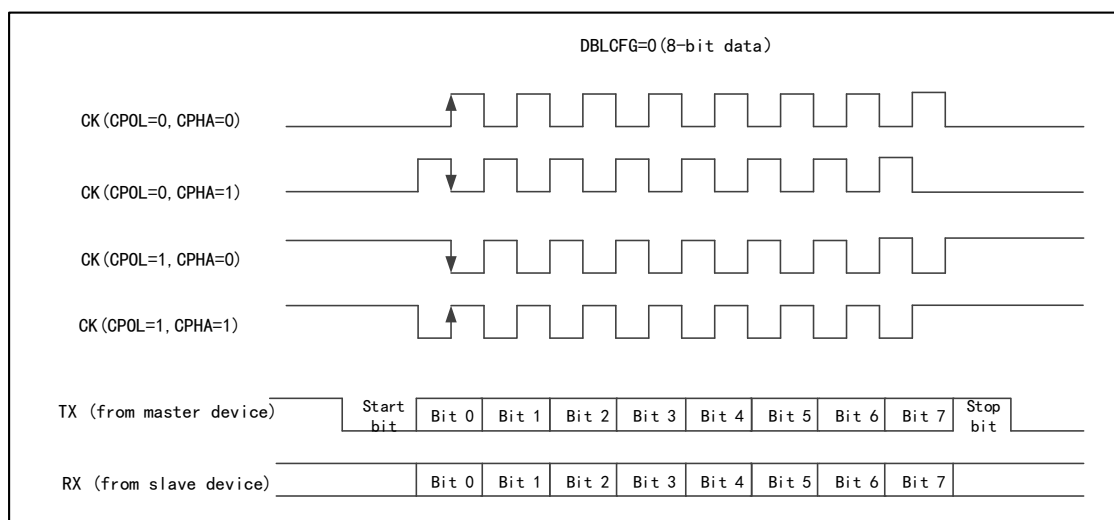
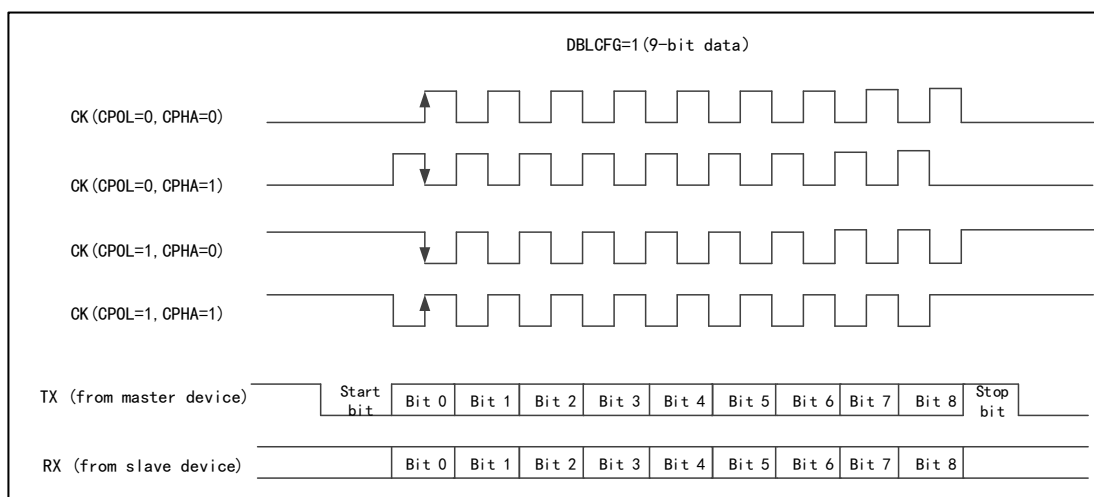


Figure 71 USART Synchronous Transmission Timing Diagram (DBLCFG=1)



## 20.4.8 LIN mode

LINMEN bit of USART\_CTRL2 register decides whether to enter LIN mode.

When entering LIN mode:

- All data frames are 8 data bits and 1 stop bit.
- The CLKEN bit and STOPCF bit of USART\_CTRL2 register and IREN bit, HDEN bit and SCEN bit of USART\_CTRL3 register need to be cleared.

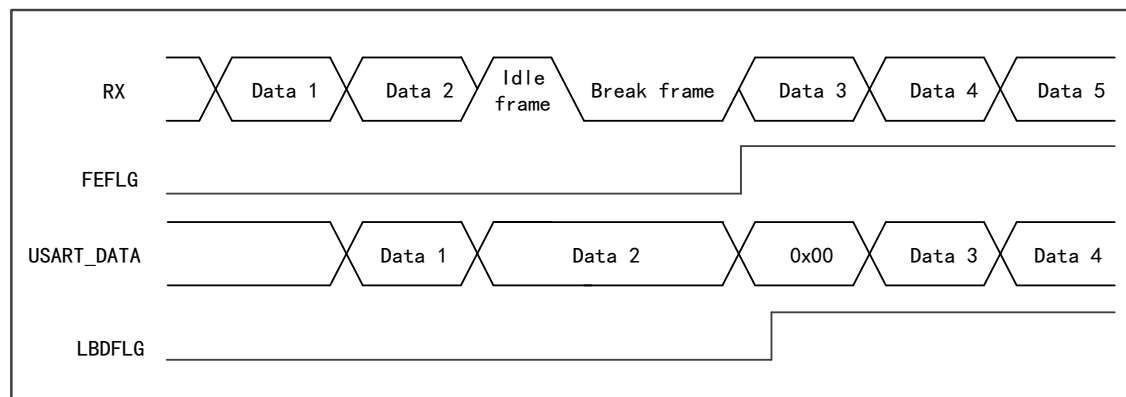
In LIN master mode, USART can generate break frame, and the detection length of break frame can be set to 10 bits and 11 bits through LBDLCFG bit of USART\_CTRL2. The break frame detection circuit is independent of USART receiver, and no matter in idle state or in data transmission state, RX pin can detect the break frame, and LBDLFLG bit of USART\_STS register is set to 1; at this time, if LBDIEN bit of USART\_CTRL2 is enabled, an interrupt will be generated.



## Detection of break frame in idle state

In idle state, if a break frame is detected on RX pin, the receiver will receive a data frame of 0 and generate FEFLG.

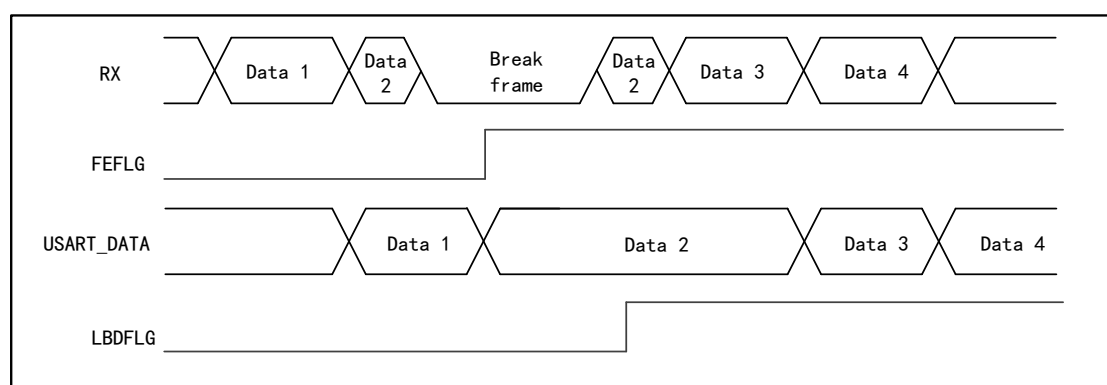
Figure 72 Break Frame Detection in Idle State



## Break frame detection in data transmission state

In the process of data transmission, if the RX pin detects the break frame, the currently transmitted data frame will generate FEFLG.

Figure 73 Break Frame Detection in Data Transmission State



## 20.4.9 Smart card mode

Smart card mode is a single-line half-duplex communication mode. The interface supports ISO7816-3 standard protocol and can control the reading and writing of smart cards that meet the standard protocol.

SCEN bit of USART\_CTRL3 register decides whether to enter the smart card mode.

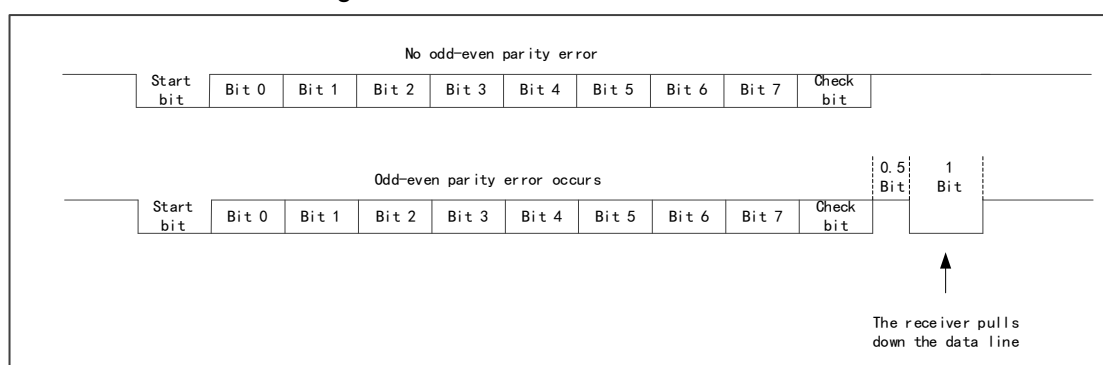
When USART enters the smart card mode:

- The LINMEN bit of USART\_CTRL2 register, and IREN and HDEN bits of USART\_CTRL3 register must be cleared.
- The data frame format is 8 data bits and 1 check bit, and 0.5 or 1.5 stop bits are used. (To avoid switching between two configurations, it

is recommended to use 1.5 stop bits when transmitting and receiving data)

- CLKEN bit of USART\_CTRL2 can be set to provide clocks for smart card.
- During the communication, when the receiver detects a parity error, in order to inform the transmitter that the data has not been received successfully, the data line will be pulled down after half a baud rate clock, and keep pulling down for one baud rate clock.
- The break frame has no meaning in smart card mode. A 00h data with frame error will be regarded as a data instead of disconnection symbol.

Figure 74 ISO7816-3 Standard Protocol



#### 20.4.10 Infrared (IrDA SIR) function mode

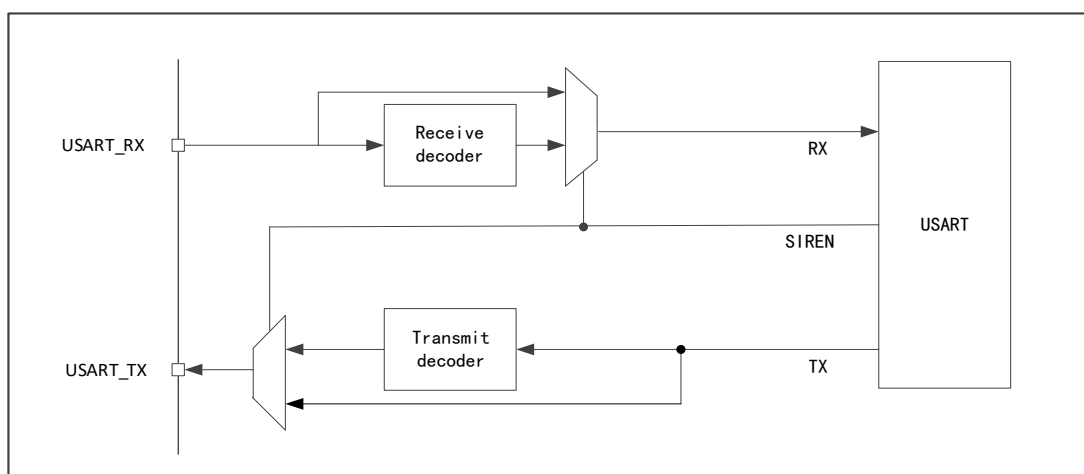
IrDA mode is a half-duplex protocol, transmitting and receiving data can not be carried out at the same time, and the delay between data transmitting and receiving should be more than 10ms.

IREN bit of USART\_CTRL3 register decides whether to enter the IrDA mode.

When USART enters the IrDA mode:

- The CLKEN bit, STOPCF bit and LINMEN bit of USART\_CTRL2 register and HDEN bit and SCEN bit of USART\_CTRL3 register must be cleared.
- The data frame uses 1 stop bit and the baud rate is less than 115200Hz.
- Using infrared pulse (RZI) indicates logic 0, so in normal mode, its pulse width is 3/16 baud rate cycles. When IrDA is in low mode, it is recommended that the pulse width be greater than three DIV frequency division clocks so as to ensure that this pulse can be detected by IrDA normally.

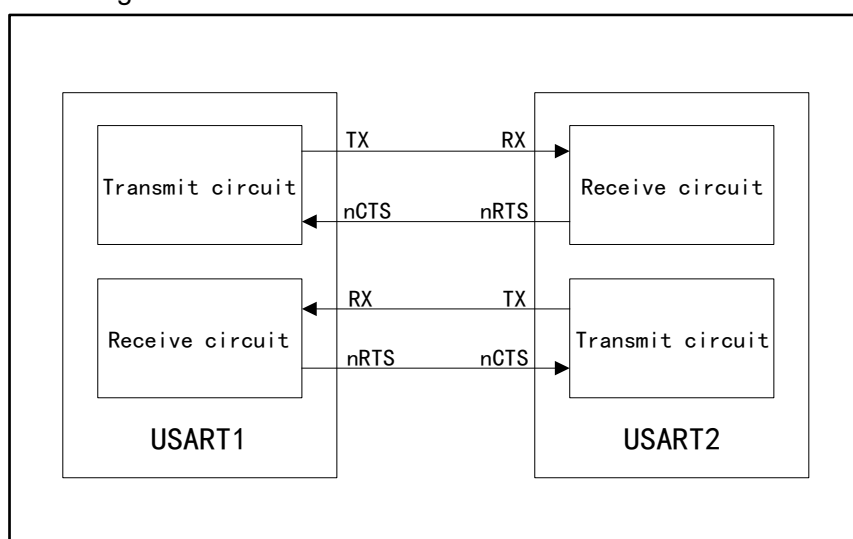
Figure 75 IrDA Mode Block Diagram



### 20.4.11 Hardware flow control

The function of hardware flow control is to control the serial data stream between two devices through nCTS pin and nRTS pin.

Figure 76 Hardware Flow Control between Two USART



#### CTS flow control

CTSEN bit of USART\_CTRL3 register determines whether CTS flow control is enabled. If CTS flow control is enabled, the transmitter will detect whether the data frame of nCTS pin can be sent. If TXBEFLG bit=0 for USART\_STS register and nCTS is pulled to low level, the data frame can be sent. If nCTS becomes high during transmission, the transmitter will stop transmitting after the current data frame is transmitted.

#### RTS flow control

RTSEN bit of USART\_CTRL3 register determines whether RTS flow control is enabled. If RTS flow control is enabled, when the receiver receives data, nRTS

will be pulled to low level. When a data frame is received, nRTS will become high to inform the transmitter to stop transmitting data frame.

#### 20.4.12 DMA multi-processor communication

USART can access the data buffer in DMA mode in order to reduce the burden of processors.

##### Transmission in DMA mode

DMATXEN bit of USART\_CTRL3 register determines whether to transmit in DMA mode. When transmitting by DMA, the data in the designated SRAM will be transmitted to the buffer by DMA.

Configuration steps of transmission by DMA:

- (1) Clear the TXCFLG bit of USART\_STS register.
- (2) Set the address of SRAM memory storing data as DMA source address.
- (3) Set the address of USART\_DATA register as DMA destination address.
- (4) Set the number of data bytes to be transmitted.
- (5) Set channel priority.
- (6) Set interrupt enable.
- (7) Enable DMA channel.
- (8) Wait for TXCFLG bit of USART\_STS register to be set to 1, indicating transmission completion.

##### Receive in DMA mode

DMARXEN bit of USART\_CTRL3 register determines whether to use DMA mode to receive; when DMA is used to receive, every time one byte is received, the received buffer data will be transmitted to the specified SRAM area by DMA.

Configuration steps of receiving by DMA:

- (1) Set the address of USART\_DATA register as DMA source address.
- (2) Set the address of SRAM memory storing data as DMA destination address.
- (3) Set the number of data bytes to be transmitted.
- (4) Set channel priority.
- (5) Set interrupt enable.
- (6) DMA channel enable.

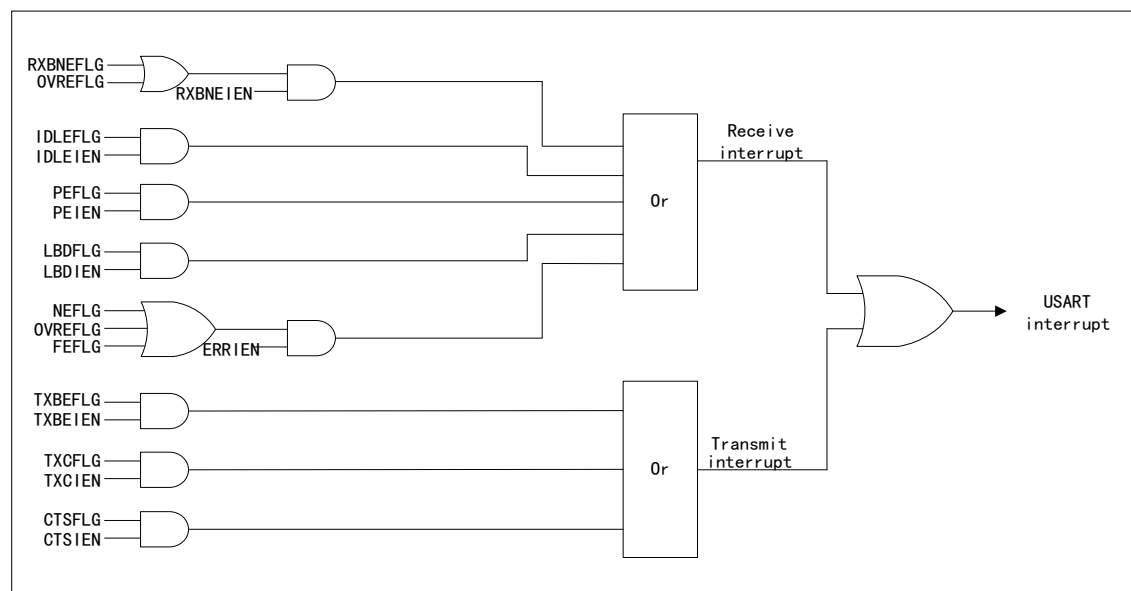
## 20.4.13 Interrupt request

Table 85 USART Interrupt Request

| Interrupt event                      |               | Event flag bit | Enable bit |
|--------------------------------------|---------------|----------------|------------|
| The receive register cannot be empty |               | RXBNEFLG       | RXBNEIEN   |
| Overload error                       |               | OVREFLG        |            |
| Line idle is detected                |               | IDLEFLG        | IDLEIEN    |
| Odd-even parity error                |               | PEFLG          | PEIEN      |
| LIN break frame flag                 |               | LBDFLG         | LBDIEN     |
| Receiving error in DMA mode          | Noise error   | NEFLG          | ERRIEN     |
|                                      | Overrun error | OVREFLG        |            |
|                                      | Frame error   | FEFLG          |            |
| Data transmit register is empty      |               | TXBEFLG        | TXBEIEN    |
| Transmission is completed            |               | TXCFLG         | TXCIEN     |
| CTS flag                             |               | CTSFLG         | CTSIEN     |

All interrupt requests of USART are connected to the same interrupt controller, and the interrupt requests have logical or relational before they are sent to the interrupt controller.

Figure 77 USART Interrupt Mapping



## 20.4.14 Comparison of USART supporting functions

Table 86 Comparison of USART Supporting Functions

| USART 模式                         | USART1 | USART2 | USART3 | UART4 | UART5 | USART6 |
|----------------------------------|--------|--------|--------|-------|-------|--------|
| Half-duplex (single-wire mode)   | √      | √      | √      | √     | √     | √      |
| Multichannel communication       | √      | √      | √      | √     | √     | √      |
| Synchronous                      | √      | √      | √      | —     | —     | √      |
| Asynchronous mode                | √      | √      | √      | √     | √     | √      |
| LIN                              | √      | √      | √      | √     | √     | √      |
| Smart card                       | √      | √      | √      | —     | —     | √      |
| IrDA                             | √      | √      | √      | √     | √     | √      |
| Hardware flow control            | √      | √      | √      | —     | —     | √      |
| Multi-buffer communication (DMA) | √      | √      | √      | √     | √     | √      |

Note: "√" means this function is supported, while "—" means that this function is not supported.

## 20.5 Register address mapping

Table 87 USART Register Address Mapping

| Register name | Description                            | Offset address |
|---------------|----------------------------------------|----------------|
| USART_STS     | State register                         | 0x00           |
| USART_DATA    | Data register                          | 0x04           |
| USART_BR      | Baud rate register                     | 0x08           |
| USART_CTRL1   | Control register 1                     | 0x0C           |
| USART_CTRL2   | Control register 2                     | 0x10           |
| USART_CTRL3   | Control register 3                     | 0x14           |
| USART_GTPSC   | Protection time and prescaler register | 0x18           |

## 20.6 Register functional description

### 20.6.1 State register (USART\_STS)

Offset address: 0x00

Reset value: 0x0000 00C0

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PEFLG    | R     | <p>Parity Error Occur Flag</p> <p>0: No error</p> <p>1: Parity error occurs</p> <p>In the receiving mode, when a parity error occurs, set to 1 by hardware;</p> <p>This bit can be cleared by software; after setting of RXBNEFLG, first read USART_STS register, and then read USART_DATA register to complete clearing.</p>                                             |
| 1     | FEFLG    | R     | <p>Frame Error Occur Flag</p> <p>0: No frame error</p> <p>1: A frame error or disconnection symbol appeared</p> <p>When there is synchronous dislocation, too much noise or disconnection symbol, set to 1 by hardware;</p> <p>This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.</p>            |
| 2     | NEFLG    | R     | <p>Noise Error Occur Flag</p> <p>0: No noise</p> <p>1: There is noise error</p> <p>When there is noise error, set to 1 by hardware;</p> <p>This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.</p>                                                                                                |
| 3     | OVREFLG  | R     | <p>Overrun Error Occur Flag</p> <p>0: No overrun error</p> <p>1: Overrun error occurred</p> <p>When the RXBNEFLG bit is set and the data in the shift register is to be transmitted to the receive register, set to 1 by hardware;</p> <p>This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.</p> |
| 4     | IDLEFLG  | R     | <p>IDLE Line Detected Flag</p> <p>0: Idle bus is not detected</p> <p>1: Idle bus is detected</p> <p>When idle bus is detected, set to 1 by hardware;</p> <p>This bit can be cleared by software; first read USART_STS register, and then read USART_DATA register to complete clearing.</p>                                                                               |
| 5     | RXBNEFLG | RC_W0 | <p>Receive Data Buffer Not Empty Flag</p> <p>0: The receive data buffer is empty</p> <p>1: The receive data buffer is not empty</p> <p>When the data register receives the data transmitted by the receive shift register, it will be set to 1 by hardware;</p> <p>This bit can be cleared by software; read USART_DATA to clear, or write 0 to this bit to clear it.</p> |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6     | TXCFLG   | RC_W0 | Transmit Data Complete Flag<br>0: Transmitting data is not completed<br>1: Transmitting data is completed<br>After the last frame of data is sent and the TXBEFLG is set, set to 1 by hardware;<br>This bit can be cleared by software; first read USART_STS register, and then write USART_DATA register to complete clearing; or this bit can be cleared by writing 0 to it. |
| 7     | TXBEFLG  | R     | Transmit Data Buffer Empty Flag<br>0: The transmit data buffer is not empty<br>1: The transmit data buffer is empty<br>When the shift register receives the data transmitted by the transmit data register, it will be set to 1 by hardware;<br>This bit can be cleared by software; write USART_DATA register to complete clearing.                                           |
| 8     | LBDFLG   | RC_W0 | LIN Break Detected Flag<br>0: LIN disconnection not detected<br>1: LIN disconnection detected<br>When LIN disconnection is detected, set to 1 by hardware;<br>This bit can be cleared by software; or cleared by writing 0 to this bit.                                                                                                                                        |
| 9     | CTSFLG   | RC_W0 | CTS Change Flag<br>0: No change on nCTS state line<br>1: There is change on nCTS state line<br>If the CTSEN bit is set, when switching to the nCTS input, set to 1 by hardware;<br>This bit can be cleared by software; or cleared by writing 0 to this bit.                                                                                                                   |
| 31:10 | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                |

### 20.6.2 Data register (USART\_DATA)

Offset address: 0x04

Reset value: 0XXXXX XXXX, X=undefined bit

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                        |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:0   | DATA     | R/W | Data Value<br>Transmit or receive the data value; read data when receiving data, and write data to the register when transmitting data.<br>When the parity bit is enabled, for 9 data bits, the 8th bit of DATA is parity bit; for 8 data bits, the 7th bit of DATA is parity bit. |
| 31:9  | Reserved |     |                                                                                                                                                                                                                                                                                    |

### 20.6.3 Baud rate register (USART\_BR)

Offset address: 0x08

Reset value: 0x0000 0000



| Field | Name      | R/W | Description                                                                                                                         |
|-------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | FBR[3:0]  | R/W | Fraction of USART Baud Rate Divider factor<br>The decimal part of USART baud rate division factor is determined by these four bits. |
| 15:4  | IBR[15:4] | R/W | Integer of USART Baud Rate Divider factor<br>The integral part of USART baud rate division factor is determined by these 12 bits.   |
| 31:16 | Reserved  |     |                                                                                                                                     |

#### 20.6.4 Control register 1 (USART\_CTRL1)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TXBF     | R/W | Transmit Break Frame<br>0: Not transmit<br>1: Will transmit<br>This bit can be set by software and cleared by hardware when the stop bit of the break frame is sent.                                                                                                                                                                                                                                                   |
| 1     | RXMUTEEN | R/W | Receive Mute Mode Enable<br>0: Normal working mode<br>1: Mute mode<br>This bit is set or cleared by software, or cleared by hardware when wake-up sequence is detected.<br>USART must receive a data before it is put in the mute mode, so that it can be detected and awakened by idle bus.<br>In the wake-up of address flag detection, if the RXBNEFLG bit is set, the RXMUTEEN bit cannot be modified by software. |
| 2     | RXEN     | R/W | Receive Enable<br>0: Disable<br>1: Enable, and start to detect the start bit on RX pin                                                                                                                                                                                                                                                                                                                                 |
| 3     | TXEN     | R/W | Transmit Enable<br>0: Disable<br>1: Enable<br>Except in smart card mode, if there is a 0 pulse on this bit at any time of transmitting data, an idle bus will be transmitted after the current data is transmitted.<br>After this bit is set, the data will be transmitted after one-bit time.                                                                                                                         |
| 4     | IDLEIEN  | R/W | IDLE Interrupt Enable<br>0: Disable<br>1: Generate an interrupt when IDLEFLG is set                                                                                                                                                                                                                                                                                                                                    |
| 5     | RXBNEIEN | R/W | Receive Buffer Not Empty Interrupt Enable<br>0: Disable<br>1: Generate an interrupt when OVREFLG or RXBNEFLG is set                                                                                                                                                                                                                                                                                                    |
| 6     | TXCIEN   | R/W | Transmit Complete Interrupt Enable<br>0: Disable<br>1: Generate an interrupt when TXCFLG is set                                                                                                                                                                                                                                                                                                                        |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7     | TXBEIEN  | R/W | Transmit Buffer Empty Interrupt Enable<br>0: Interrupt generation is disabled<br>1: Generate an interrupt when TXBEFLG is set                                                                                                                                                                                                              |
| 8     | PEIEN    | R/W | Parity Error interrupt Enable<br>0: Interrupt generation is disabled<br>1: Generate an interrupt when PEFLG is set                                                                                                                                                                                                                         |
| 9     | PCFG     | R/W | Odd/Even Parity Configure<br>0: Even parity check<br>1: Odd parity check<br>The selection will not take effect until the current transmission of bytes is completed.                                                                                                                                                                       |
| 10    | PCEN     | R/W | Parity Control Enable<br>0: Disable<br>1: Enable<br>If this bit is set, a check bit will be inserted in the most significant bit when transmitting data; when receiving data, check whether the check bit of the received data is correct.<br>The check control will not take effect until the current transmission of bytes is completed. |
| 11    | WUPMCFG  | R/W | Wakeup Method Configure<br>0: Idle bus wakeup<br>1: Address tag wakeup                                                                                                                                                                                                                                                                     |
| 12    | DBLCFG   | R/W | Data Bits Length Configure<br>0: 1 start bit, 8 data bits, n stop bits<br>1: 1 start bit, 9 data bits, n stop bits<br>This bit cannot be modified during transmission of data.                                                                                                                                                             |
| 13    | UEN      | R/W | USART Enable<br>0: USART frequency divider and output are disabled<br>1: USART module is enabled                                                                                                                                                                                                                                           |
| 14    | Reserved |     |                                                                                                                                                                                                                                                                                                                                            |
| 15    | OSMCFG   | R/W | Oversampling Mode Configure<br>0: 16-time oversampling<br>1: 8-time oversampling<br>This bit can be set only when USART is not enabled.                                                                                                                                                                                                    |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                            |

## 20.6.5 Control register 2 (USART\_CTRL2)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                              |
|-------|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | ADDR[3:0] | R/W | USART Device Node Address Setup<br>This bit is valid only in the mute mode of multiprocessor communication, and decides to enter the mute mode or wake up according to whether the detected address tags are consistent. |
| 4     | Reserved  |     |                                                                                                                                                                                                                          |

| Field | Name     | R/W | Description                                                                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5     | LBDLCFG  | R/W | LIN Break Detection Length Configure<br>0: 10 bits<br>1: 11 bits                                                                                                                                                          |
| 6     | LBDIEN   | R/W | LIN Break Detection Interrupt Enable<br>0: Disable<br>1: Generate an interrupt when LBDFLG bit is set                                                                                                                     |
| 7     | Reserved |     |                                                                                                                                                                                                                           |
| 8     | LBCPOEN  | R/W | Last Bit Clock Pulse Output Enable<br>0: Not output from CK<br>1: Output from CK<br>This bit is valid only in synchronous mode; this bit does not exist on UART4 and UART5.                                               |
| 9     | CPHA     | R/W | Clock Phase Configure<br>This bit indicates on the edge of which clock sampling is conducted.<br>0: The first<br>1: The second<br>This bit is valid only in synchronous mode; this bit does not exist on UART4 and UART5. |
| 10    | CPOL     | R/W | Clock Polarity Configure<br>The state of CK pin when USART is in idle state.<br>0: Low level<br>1: High level<br>This bit is valid only in synchronous mode; this bit does not exist on UART4 and UART5.                  |
| 11    | CLKEN    | R/W | Clock Enable (CK pin)<br>0: Disable<br>1: Enable<br>This bit does not exist on UART4 and UART5.                                                                                                                           |
| 13:12 | STOPCFG  | R/W | STOP Bit Configure<br>00: 1 stop bit<br>01: 0.5 stop bit<br>10: 2 stop bits<br>11: 1.5 stop bits                                                                                                                          |
| 14    | LINMEN   | R/W | LIN Mode Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                |
| 31:15 | Reserved |     |                                                                                                                                                                                                                           |

Note: These three bits (CPOL, CPHA and LBCPOEN) cannot be changed after transmission is enabled.

## 20.6.6 Control register 3 (USART\_CTRL3)

Offset address: 0x14

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ERRIEN   | R/W | Error interrupt Enable<br>0: Disable<br>1: Enable; when DMARXEN is set and one among FEFLG, OVREFLG or NEFLG is set, an interrupt will be generated.                                                                                                                                                                                                                                                                                                                                                                                            |
| 1     | IREN     | R/W | IrDA Function Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2     | IRLPEN   | R/W | IrDA Low-power Mode Enable<br>0: Normal mode<br>1: Low-power mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 3     | HDEN     | R/W | Half-duplex Mode Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4     | SCNACKEN | R/W | NACK Transmit Enable During Parity Error in Smartcard Function<br>0: NACK is not sent<br>1: Transmit NACK<br>This bit does not exist on UART4 and UART5.                                                                                                                                                                                                                                                                                                                                                                                        |
| 5     | SCEN     | R/W | Smartcard Function Enable<br>0: Disable<br>1: Enable<br>This bit does not exist on UART4 and UART5.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 6     | DMARXEN  | R/W | DMA Receive Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7     | DMATXEN  | R/W | DMA Transmit Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | RTSEN    | R/W | RTS Hardware Flow Control Function Enable<br>0: Disable<br>1: Enable RTS interrupt<br>RTS: Require To Send, which is output signal, indicating it has been ready to receive.<br>Request is made to receive data only when there is space in the receive buffer; when data can be received, RTS output is pulled to low level.<br>This bit does not exist on UART4 and UART5.                                                                                                                                                                    |
| 9     | CTSEN    | R/W | CTS Hardware Flow Control Function Enable<br>0: Disable<br>1: Enable<br>CTS: Clear To Send, which is input signal<br>When CTS input signal is at low level, the data can be transmitted; otherwise, the data cannot be transmitted; if CTS signal is pulled to high during data transmission, the data transmission will be stopped after this data is transmitted; if write operation is performed for the data register when CTS is high, the data will not be transmitted until CTS is valid.<br>This bit does not exist on UART4 and UART5. |

| Field | Name     | R/W | Description                                                                                                                                                         |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10    | CTSIEN   | R/W | CTS Interrupt Enable<br>0: Disable<br>1: Generate an interrupt when CTSFLG is set<br>This bit does not exist on UART4 and UART5.                                    |
| 11    | SAMCFG   | R/W | Sample Method Configure<br>0: Sampling for three times<br>1: Single sample; flag of noise detection disabled<br>This bit can be set only when USART is not enabled. |
| 31:12 | Reserved |     |                                                                                                                                                                     |

### 20.6.7 Protection time and prescaler register (USART\_GTPSC)

Offset address: 0x18

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | PSC      | R/W | Prescaler Factor Setup<br>Divide the frequency and provide clock for the system clock respectively; in different working modes, the valid bits of PSC have difference, specifically as follows:<br>In infrared low-power mode:<br>PSC[7:0] is valid.<br>00000000: Reserved<br>00000001: 1 divided frequency<br>00000010: 2 divided frequency<br>.....<br>11111111: 255 divided frequency<br>In infrared normal mode:<br>PSC can only be set to 00000001<br>In smart card mode:<br>PSC[7:5] invalid, PSC[4:0] valid<br>00000: Reserved<br>00001: 2 divided frequency<br>00010: 4 divided frequency<br>00011: 6 divided frequency<br>.....<br>11111: 62 divided frequency<br>This bit does not exist on UART4 and UART5. |
| 15:8  | GRDT     | R/W | Guard Time Value Setup<br>After transmitting data, TXCFLG can be set after the protection time; the time unit is baud clock; it can be applied to smart card mode; this bit does not exist on UART4 and UART5.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

## 21 Internal Integrated Circuit Interface (I2C)

### 21.1 Full name and abbreviation description of terms

Table 88 Full name and abbreviation description of terms

| Full name in English        | English abbreviation |
|-----------------------------|----------------------|
| Serial Data                 | SDA                  |
| Serial Clock                | SCL                  |
| System Management Bus       | SMBus                |
| Clock                       | CLK                  |
| Serial Clock High           | SCLH                 |
| Serial Clock Low            | SCLL                 |
| Address Resolution Protocol | ARP                  |
| Negative Acknowledgement    | NACK                 |
| Packet Error Checking       | PEC                  |
| Address Resolution Protocol | ARP                  |

### 21.2 Introduction

I2C is a short-distance bus communication protocol. In implementation, I2C bus is composed of two signal lines (SDA and SCL) and a ground wire. These two signal lines can be used for bidirectional transmission.

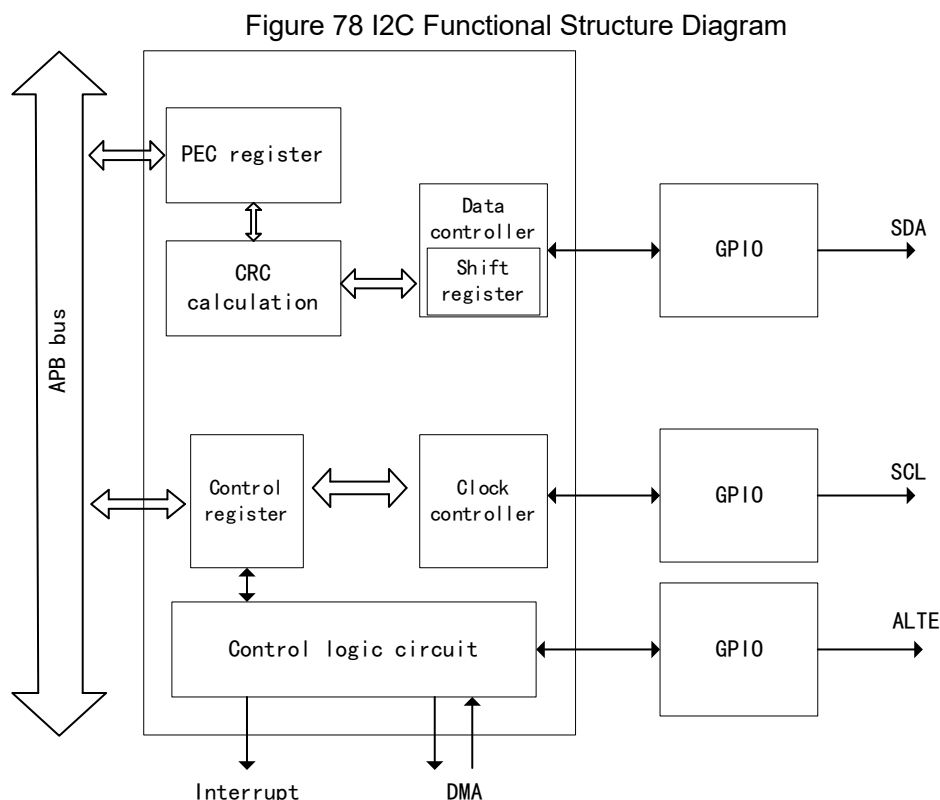
- Two signal lines, SCL clock line and SDA data line. SCL provides timing for SDA, and SDA transmits/receives data in series
- Both SCL and SDA signal lines are bidirectional
- The ground is common when the two systems use I2C bus for communication

### 21.3 Main characteristics

- (1) Multi-master function
- (2) The master can generate the clock, start bit and stop bit
- (3) Slave function
  - Programmable I2C address detection
  - Double-address mode
  - Detection stop bit
- (4) 7-bit and 10-bit addressing mode
- (5) Response to broadcast

- (6) Two communication speeds
  - Standard mode
  - Fast mode
- (7) Programmable clock extension
- (8) State flag
  - Transmitter/Receiver mode flag
  - Flag for end of byte transmission
  - Flag of busy bus
- (9) Error flag
  - Arbitration loss
  - Acknowledgment error
  - Wrong start bit or stop bit detected
- (10) Interrupt source
  - Address/Data communication succeeded
  - Error interrupt
- (11) Support DMA function
- (12) Programmable PEC
  - Final transmission in transmission mode
  - PEC error check after the last byte is received
- (13) SMBus specific function
  - Hardware PEC
  - Address resolution protocol

## 21.4 Structure block diagram



The interface can be configured to the following modes:

- Slave transmitting
- Slave receiving
- Master transmitting
- Master receiving

In the initial state of I2C interface, the working mode is slave mode. After I2C interface transmits the start signal, it will automatically switch from slave mode to master mode.

## 21.5 Functional description

Table 89 Description of Special Terms of I2C Bus

| Special terms | Description                                                                                 |
|---------------|---------------------------------------------------------------------------------------------|
| Transmitter   | Device transmitting data to the bus                                                         |
| Receiver      | Device receiving data from the bus                                                          |
| Master        | Device that initiates data transmission, generates clock signals and ends data transmission |
| Slave         | Device addressed by master                                                                  |

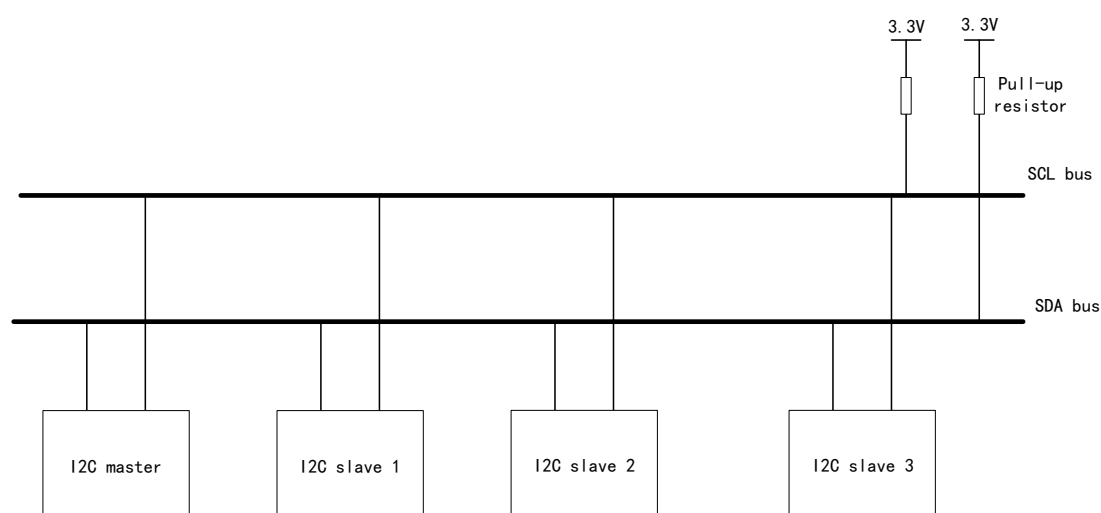


| Special terms    | Description                                                                                                                                                                |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Multiple masters | Multiple masters that control the bus at the same time without destroying information                                                                                      |
| Synchronous      | The process of synchronizing the clock signals between two or more devices                                                                                                 |
| Arbitration      | If more than one master tries to control the bus at the same time, only one master can control the bus, and the information of the controlled master will not be destroyed |

### 21.5.1 I2C physical layer

The commonly used connection modes between I2C communication devices are shown in the figure below:

Figure 79 Commonly Used I2C Communication Connection Diagram



#### Characteristics of physical layer:

- (1) Bus supporting multiple devices (signal line shared by multiple devices), which, in I2C communication bus, can connect multiple communication masters and communication slaves.
- (2) An I2C bus only uses two bus lines, namely, a bidirectional serial data line (SDA) and a serial clock line (SCL). The data line is used for data transmission, and the clock line is used for synchronous receiving and transmission of data.
- (3) Each device connected to the bus has an independent address (seven or ten bits), and the master addresses and accesses the slave device according to the address of the device.
- (4) The bus needs to connect the pull-up resistor to the power supply. When I2C bus is idle, the output is in high-impedance state. When all devices are idle, the output is in high-impedance state, and the pull-up resistor pulls the bus to high level.

- (5) Communication modes: Standard mode (up to 100KHz), fast mode (up to 400KHz).
- (6) When multiple masters use the bus at the same time, to prevent the data collision, the bus arbitration mode is adopted to determine which device occupies the bus.
- (7) Can program setup and hold time, and program the high-level time and low-level time of SCL in I2C.

## 21.5.2 I2C protocol layer

### Characteristics of protocol layer

- (1) Data is transmitted in the form of frame, and each frame is composed of 1 byte (8 bits).
- (2) In the rising edge phase of SCL, SDA needs to keep stable and SDA changes during the period when SCL is low.
- (3) In addition to data frame, I2C bus also has start signal, stop signal and acknowledge signal.
  - Start bit: During the stable high level period of SCL, a falling edge of SDA starts transmission.
  - Stop bit: During the stable high level period of SCL, a rising edge of SDA stops transmission.
  - Acknowledge bit: Used to indicate successful transmission of one byte. After the bus transmitter (regardless of the master or slave) transmits 8-bit data, SDA will release (from output to input). During the ninth clock pulse, the receiver will pull down SDA to respond to the received data.

### I2C communication reading and writing process

Figure 80 Master Writes Data to Slave

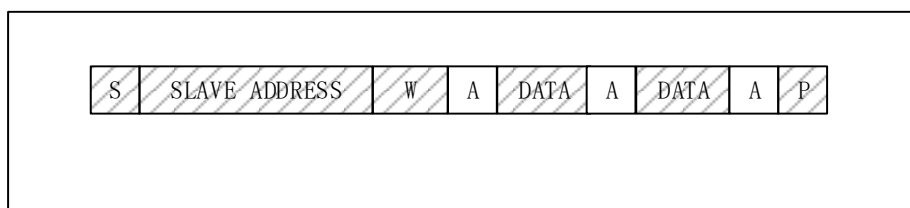
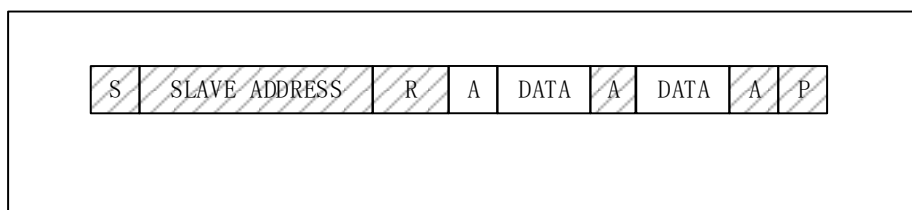


Figure 81 Master Reads Data from Slave



Remarks:

- (1) : This data is transmitted from master to slave
- (2) S: Start signal
- (3) SLAVE ADDRESS: Slave address
- (4) : This data is transmitted from slave to master
- (5) R/W: Selection bit of transmission direction
- (6) 1 means read
- (7) 0 means write
- (8) P: Stop signal

After the start signal is generated, all slaves will wait for the slave address signal sent by the master. In I2C bus, the address of each device is unique. When the address signal matches the device address, the slave will be selected, and the unselected slave will ignore the future data signal.

#### When the master direction is writing data

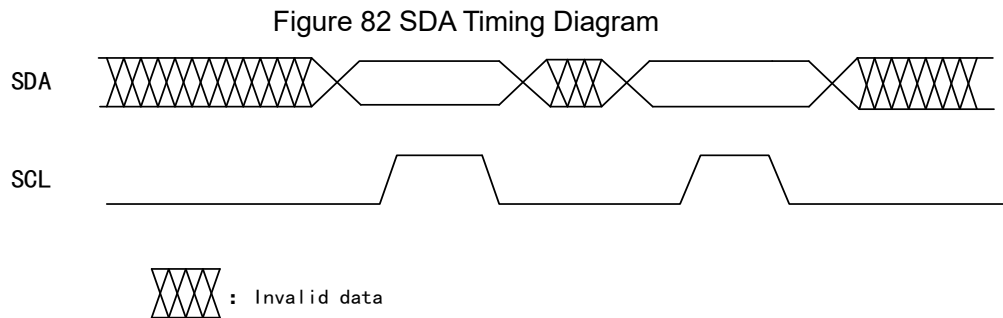
After broadcasting the address and receiving the acknowledge signal, the master will transmit data to the slave, the data length is one byte, and every time the master transmits one byte of data, it needs to wait for the answer signal transmitted by the slave. After all the bytes have been transmitted, the master will transmit a stop signal (STOP) to the slave, indicating that the transmission is completed.

#### When the master direction is reading data

After broadcasting the address and receiving the acknowledge signal, the slave will transmit the data to the master. The size of the data package is 8 bits. Every time the slave transmits one byte of data, it needs to wait for the acknowledge signal of the master. When the master wants to stop receiving data, it needs to return a non-acknowledge signal to the slave, then the slave will stop transmitting the data automatically.

### 21.5.3 Data validity

In the process of data transmission, the data on SDA line must be stable when the clock signal SCL is at high level. Only when the SCL is at the low level, can the level state of SDA be changed, and the bit transmission of each data needs a clock pulse.



### 21.5.4 Start and stop signals

All data transmission must have start signal (START) and stop signal (STOP).

Figure 83 START signal is defined as: when SCL is at high level, SDA will convert from high level to low level

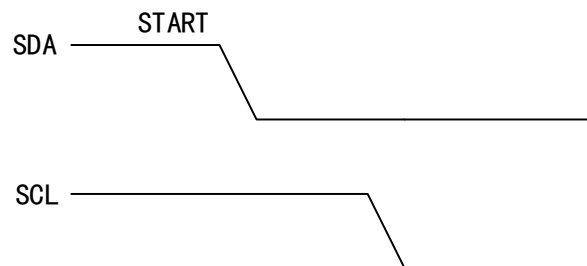
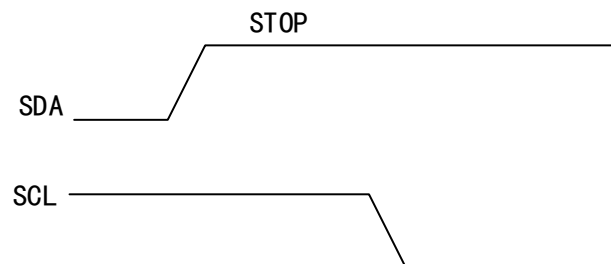


Figure 84 STOP signal is defined as: when SCL is at high level, SDA will convert from low level to high level



### 21.5.5 Arbitration

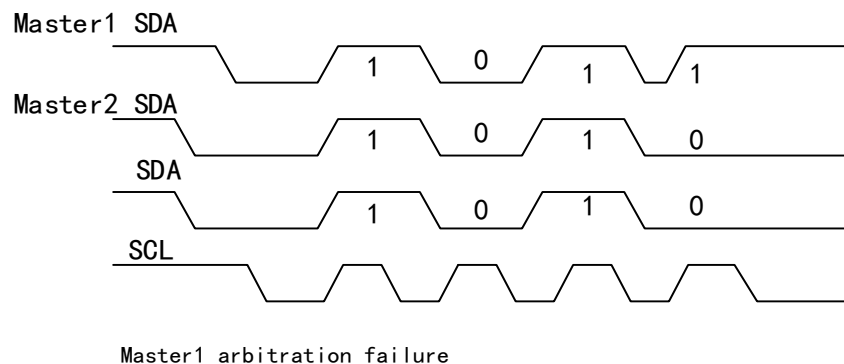
Arbitration is also used to solve the bus control conflict in case of multiple masters. The arbitration process takes place on the master and has nothing to do with the slave.

The master can start transmission only when the bus is idle. Two masters may generate an effective START signal on the bus within the shortest hold time of the START signal. In this situation, it is required that arbitration should decide

which master completes the transmission.

Arbitration is conducted by bit. During each arbitration, when SCL is high, each master will check whether the SDA level is the same as that sent by itself. The arbitration process needs to last for many bits. Theoretically, if two masters transmit exactly the same content, they can successfully transmit without arbitration failure. If one master transmits high level, but it is detected that SDA is at low level, an arbitration failure error will occur, the SDA output of the master will be disabled, and the other master will complete its own transmission.

Figure 85 SDA Timing Diagram



### 21.5.6 SMBus specific function

System management bus (SMBus) is a simple single-end double-wire bus, which can meet the requirements of lightweight communication.

SMBus is commonly used in computer motherboard, mainly for power transmission ON/OFF instructions. SMBus is the derivative bus of I2C. It is mainly used for communication of low-bandwidth devices on computer motherboard, and power-related chip.

#### Address resolution protocol

SMBus specification includes an address resolution protocol, which can realize dynamic address assignment. Dynamic recognition hardware and software enable the bus to support hot plugging, and the bus devices will be automatically identified and assigned with a unique address.

#### SMBus alarm

SMBus alert is an optional signal with an interrupt line, used to extend device control capabilities by occupying pins.

## 21.5.7 Error flag bit

Table 90 The following several error flag bits exist in I2C communication

| Error flag bit                               | Description of error flag bit                                                                                                                                                                                                                  |
|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Answer error flag bit (AEFLG)                | No answer received                                                                                                                                                                                                                             |
| Bus error flag bit (BERRFLG)                 | An external stop or start condition is detected                                                                                                                                                                                                |
| Arbitration loss flag bit (ALFLG)            | Arbitration loss is detected by the interface                                                                                                                                                                                                  |
| Overflow/Underflow error flag bit (OVRURFLG) | In slave mode, the received data is not read out, the next data has arrived, and an overrun error occurs.<br>The transmitting data clock has arrived, but the data has not been written into the DATA register, and an underflow error occurs. |
| Timeout or Tow error flag bit (TTEFLG)       | SCL is pulled down for more than a certain time                                                                                                                                                                                                |
| PEC comparison error flag bit (PECEFLG)      | CRC values are not equal                                                                                                                                                                                                                       |

## 21.5.8 Message error check (PEC)

I2C module has a PEC module, which checks the message of I2C data by CRC-8 calculator. The CRC-8 polynomial used by the calculator is:  $C(x) = X^8 + X^2 + X + 1$ .

When PECEN bit is set to 1 and PEC function is enabled, PEC module will calculate all data sent by I2C bus, including address data.

## 21.5.9 DMA mode

According to the software process of I2C, when the transmit register is empty or the receive register is full, MCU needs to write or read bytes, then we can complete the operation more quickly through the DMA function of I2C.

### DMA transmission

Set the DMAEN bit in I2C\_CTRL2 register to enable the DMA mode. When the transmit register is empty (TXBEFLG is set to 1), the data will be directly loaded from the memory area to the DATA register through DMA.

### DMA receiving

Set DMAEN in I2C\_CTRL2 register to enable DMA mode. When the receiving register is full (RXBNEFLG is set to 1), DMA will transmit DATA register data to the set storage area.

## 21.5.10 I2C interrupt

Table 91 I2C Interrupt Request

| Interrupt event                                        | Event flag bit | Interrupt control bit |
|--------------------------------------------------------|----------------|-----------------------|
| Transmitting start bit completed                       | STARTFLG       | EVIEN                 |
| Transmission completed/Address matching address signal | ADDRFLG        |                       |
| 10-bit address head segment transmission completed     | ADDR10FLG      |                       |
| Received stop signal                                   | STOPFLG        |                       |
| Data byte transmission completed                       | BTCFLG         |                       |
| Receive buffer not empty                               | RXBNEFLG       | EVIEN and BUFIEN      |
| Transmit buffer empty                                  | TXBEFLG        |                       |
| Bus error                                              | BERRFLG        | ERRIEN                |
| Arbitration loss                                       | ALFLG          |                       |
| Answer error                                           | AEFLG          |                       |
| Overrun/Underrun                                       | OVRURFLG       |                       |
| PEC error                                              | PECEFLG        |                       |
| Timeout or $T_{low}$ error                             | TTEFLG         |                       |
| SMBus alarm                                            | ALERTEN        |                       |

## 21.6 Register address mapping

Table 92 I2C Register Address Mapping

| Register name | Description                   | Offset address |
|---------------|-------------------------------|----------------|
| I2C_CTRL1     | Control register 1            | 0x00           |
| I2C_CTRL2     | Control register 2            | 0x04           |
| I2C_SADDR1    | Slave address register 1      | 0x08           |
| I2C_SADDR2    | Slave address register 2      | 0x0C           |
| I2C_DATA      | Data register                 | 0x10           |
| I2C_STS1      | State register 1              | 0x14           |
| I2C_STS2      | State register 2              | 0x18           |
| I2C_CLKCTRL   | Master clock control register | 0x1C           |
| I2C_RISEMAX   | Maximum rising time register  | 0x20           |

## 21.7 Register functional description

### 21.7.1 Control register 1 (I2C\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name       | R/W | Description                                                                                                                                                                                                                    |
|-------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | I2CEN      | R/W | I2C Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                          |
| 1     | SMBEN      | R/W | SMBus Mode Enable<br>0: I2C mode<br>1: SMBus mode                                                                                                                                                                              |
| 2     | Reserved   |     |                                                                                                                                                                                                                                |
| 3     | SMBTCFG    | R/W | SMBus Type Configure<br>0: SMBus device<br>1: SMBus master                                                                                                                                                                     |
| 4     | ARPEN      | R/W | ARP Enable<br>0: Disable<br>1: Enable<br>If SMBTCFG=0, use the default address of SMBus device<br>If SMBTCFG=1, use the primary address of SMBus                                                                               |
| 5     | PECEN      | R/W | PEC Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                          |
| 6     | SRBEN      | R/W | Slave Responds Broadcast Enable<br>0: Disable<br>1: Enable<br>Note: The broadcast address is 0x00.                                                                                                                             |
| 7     | CLKSTRECHD | R/W | Slave Mode Clock Stretching Disable<br>0: Enable<br>1: Disable<br>In slave mode, enabling extending the low-level time of the clock can avoid overrun and underrun errors.                                                     |
| 8     | START      | R/W | Start Bit Transfer<br>This bit can be set to 1 and cleared by software; when transmitting the start bit or I2CEN=0, it is cleared by hardware.<br>0: Not transmit<br>1: Transmit                                               |
| 9     | STOP       | R/W | Stop Bit Transfer<br>This bit can be set to 1 or cleared by software; when transmitting the stop bit, it is cleared by hardware; when timeout error is detected, it is set to 1 by hardware.<br>0: Not transmit<br>1: Transmit |
| 10    | ACKEN      | R/W | Acknowledge Transfer Enable<br>This bit can be set to 1 or cleared by software; when I2CEN=0, it is cleared by hardware.<br>0: Not transmit<br>1: Transmit                                                                     |



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11    | ACKPOS   | R/W | Acknowledge /PEC Position Configure<br>This bit can be set to 1 or cleared by software; when I2CEN=0, it is cleared by hardware.<br>0: When receiving current byte, whether transmitting NACK/ACK, whether PEC is in shift register<br>1: When receiving next byte, whether transmitting NACK/ACK and whether PEC is in the next byte of shift register                                                           |
| 12    | PEC      | R/W | Packet Error Check Transfer Enable<br>This bit can be set to 1 or 0 by software; after PEC, start bit or stop bit is transmitted, or when I2CEN=0, it is set to 0 by hardware.<br>0: Disable<br>1: Enable                                                                                                                                                                                                         |
| 13    | ALERTEN  | R/W | SMBus Alert Enable<br>This bit can be set to 1 or cleared by software; when I2CEN=0, it is cleared by software.<br>0: Release the SMBAlert pin to make it higher, and remind to transmit the response address header immediately after transmitting the NACK signal<br>1: Drive SMBAlert pin to make it lower, and remind to transmit the response address header immediately after transmitting the ACKEN signal |
| 14    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 15    | SWRST    | R/W | Software Configure I2C under Reset State<br>0: Not reset<br>1: Reset; before I2C reset, ensure that I2C pin is released and the bus is in idle state.                                                                                                                                                                                                                                                             |

### 21.7.2 Control register 2 (I2C\_CTRL2)

Offset address: 0x04

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0   | CLKFCFG  | R/W | I2C Clock Frequency Configure<br>The clock frequency is the clock of I2C module, which is the clock input from APB bus.<br>000000: Disable<br>000001: Disable<br>000010: 2MHz<br>...<br>111100: 60MHz<br>Greater than 111100: Disable.<br>Minimum clock frequency of I2C bus: the standard mode is 1MHz, and the fast mode is 4MHz. |
| 7:6   | Reserved |     |                                                                                                                                                                                                                                                                                                                                     |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8     | ERRIEN   | R/W | Error Interrupt Enable<br>0: Disable<br>1: When the position 1 of any of the following state register is enabled, the interrupt will be generated: SMBALTFLG, TTEFLG, PECEFLG, OVRURFLG, AEFLG, ALFLG, and STS1_BERRFLG                                                                     |
| 9     | EVIEN    | R/W | Event Interrupt Enable<br>0: Disable<br>1: When the position 1 of any of the following state registers is enabled, the interrupt will be generated: STARTFLG, ADDRFLG, ADDR10FLG, STOPFLG, BTCFLG, TXBEFLG is set to 1 and BUFIEN is set to 1, RXBNEFLG is set to 1 and BUFIEN is set to 1. |
| 10    | BUFIEN   | R/W | Buffer Interrupt Enable<br>0: Disable<br>1: Enable; when the bit of any of the following state register is set to 1, the interrupt will be generated: TXBEFLG and RXBNEFLG                                                                                                                  |
| 11    | DMAEN    | R/W | DMA Requests Enable<br>0: Disable<br>1: When TXBEFLG=1 or RXBNEFLG=1, enable DMA request                                                                                                                                                                                                    |
| 12    | LTCFG    | R/W | DMA Last Transfer Configure<br>Configure whether the EOT of the next DMA is the last transmission received, and only used for the master receiving mode.<br>0: No<br>1: Yes                                                                                                                 |
| 15:13 | Reserved |     |                                                                                                                                                                                                                                                                                             |

### 21.7.3 Slave mode address register 1 (I2C\_SADDR1)

Offset address: 0x08

Reset value: 0x0000

| Field | Name      | R/W | Description                                                                                                                                             |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ADDR[0]   | R/W | Slave Address Setup<br>When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 0 bit of the address.     |
| 7:1   | ADDR[7:1] | R/W | Slave Address Setup<br>Slave address [7:1] bit                                                                                                          |
| 9:8   | ADDR[9:8] | R/W | Slave Address Setup<br>When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the [9:8] bit of the address. |
| 14:10 | Reserved  |     |                                                                                                                                                         |
| 15    | ADDRLen   | R/W | Slave Address Length Configure<br>0: 7-bit address mode<br>1: 10-bit address mode                                                                       |

### 21.7.4 Slave address register 2 (I2C\_SADDR2)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ADDRNUM    | R/W | <p>Slave Address Number Configure</p> <p>In the slave 7-bit address mode, it can be configured to identify the single-address mode and double-address mode; only ADDR1 is identified in single-address mode; both ADDR1 and ADDR2 can be identified in double-address mode.</p> <p>Single or double address registers can be identified in 7-bit address mode, specifically as follows:</p> <p>0: Identify one address (ADDR1)</p> <p>1: Identify two addresses (ADDR1 and ADDR2)</p> |
| 7:1   | ADDR2[7:1] | R/W | <p>Slave Dual Address Mode Address Setup</p> <p>[7:1] bit of the address in double-address mode</p>                                                                                                                                                                                                                                                                                                                                                                                   |
| 15:8  | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

### 21.7.5 Data register (I2C\_DATA)

Offset address: 0x10

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                         |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | DATA     | R/W | <p>Data Register</p> <p>In I2C transmission mode, write the data to be sent to this register; in I2C receiving mode, read the received data from this register.</p> |
| 15:8  | Reserved |     |                                                                                                                                                                     |

### 21.7.6 State register 1 (I2C\_STS1)

Offset address: 0x14

Reset value: 0x0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | STARTFLG | R   | <p>Start Bit Sent Finished Flag</p> <p>0: Not transmit</p> <p>1: Transmit</p> <p>When the start bit is sent, this bit can be set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then writes the DATA register; when I2CEN=0, it can be cleared by hardware.</p>                                                                                                                                                       |
| 1     | ADDRFLG  | R   | <p>Address Transfer Complete /Receive Match Flag</p> <p>Whether the matching address is received in slave mode:</p> <p>0: Not receive</p> <p>1: Receive</p> <p>Whether finishing transmitting the address in master mode:</p> <p>0: Not completed</p> <p>1: Completed</p> <p>The bit is set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then reads STS2 register; when I2CEN=0, it can be cleared by hardware.</p> |
| 2     | BTCFLG   | R   | <p>Byte Transfer Complete Flag</p> <p>0: Not completed</p> <p>1: Completed</p>                                                                                                                                                                                                                                                                                                                                                                                    |

| Field | Name      | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |           |       | <p>When receiving data, if failing to read the data received in DATA register, and a new data is received then, set to 1 by hardware;</p> <p>When transmitting data, if the DATA register is empty, to transmit the data in the shift register, set to 1 by hardware.</p> <p>This bit can be cleared after the software first reads STS1 register, and then reads or writes the DATA register; this bit can be set to 0 by hardware by transmitting a start bit or stop bit during the transmission, or when I2CEN=0.</p>                                                                           |
| 3     | ADDR10FLG | R     | <p>10-Bit Address Header Transmit Flag</p> <p>0: Not transmit</p> <p>1: Transmit</p> <p>The bit is set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then writes the DATA register; when I2CEN=0, it can be cleared by hardware.</p>                                                                                                                                                                                                                                                                                                                   |
| 4     | STOPFLG   | R     | <p>Stop Bit Detection Flag</p> <p>0: Not detected</p> <p>1: Detected</p> <p>If ACKEN=1, after one answer, when the slave detects the stop bit on the bus, it will be set to 1 by hardware;</p> <p>This bit can be cleared after the software first reads STS1 register and then writes CTRL1 register; when I2CEN=0, it can be cleared by hardware.</p>                                                                                                                                                                                                                                             |
| 5     | Reserved  |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 6     | RXBNEFLG  | R     | <p>Receive Buffer Not Empty Flag</p> <p>0: The receive buffer is empty</p> <p>1: The receive buffer is not empty</p> <p>This bit can be set to 1 by hardware when there is data in DATA register;</p> <p>When BTCFLG is set to 1, since the data register is still full, the RXBNEFLG bit cannot be cleared by reading DATA register;</p> <p>This bit can be cleared after the software reads and writes DATA register; when I2CEN=0, it can be cleared by hardware.</p>                                                                                                                            |
| 7     | TXBEFLG   | R     | <p>Transmit Buffer Empty Flag</p> <p>0: The transmit buffer is not empty</p> <p>1: The transmit buffer is empty</p> <p>This bit can be set to 1 by hardware when the content of DATA register is empty;</p> <p>When the software writes the first data to the DATA register, it will immediately move the data to the shift register, then the data in the DATA register is empty and this bit cannot be cleared;</p> <p>This bit can be cleared after the software writes data to DATA register; after transmitting the start bit or stop bit, or when I2CEN=0, it can be cleared by hardware.</p> |
| 8     | BERRFLG   | RC_W0 | <p>Bus Error Flag</p> <p>0: No bus error</p> <p>1: Bus error occurred</p> <p>Bus error means exception of start bit or stop bit; when an error is detected, this bit can be set to 1 by hardware; this bit can be</p>                                                                                                                                                                                                                                                                                                                                                                               |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |       | cleared after the software writes 0; when I2CEN=0, it can be cleared by hardware.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9     | ALFLG    | RC_W0 | <p>Master Mode Arbitration Lost Flag</p> <p>0: No arbitration loss</p> <p>1: In case of arbitration loss, I2C interface will automatically switch back to slave mode</p> <p>"Arbitration loss in master mode" means the master loses the control of buses; this bit is set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it is cleared by hardware.</p>                                                                                                                                                                                                                                   |
| 10    | AEFLG    | RC_W0 | <p>Acknowledge Error Flag</p> <p>0: No acknowledgment error</p> <p>1: Acknowledgment error occurred</p> <p>This bit can be set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it can be cleared by hardware.</p>                                                                                                                                                                                                                                                                                                                                                                           |
| 11    | OVRURFLG | RC_W0 | <p>Overrun/Underrun Flag</p> <p>0: Not occur</p> <p>1: Occurred</p> <p>This bit can be set to 1 by hardware when CLKSTRETCHD=1 and one of the following conditions is met:</p> <p>(1) In the slave receiving mode, when the data in the DATA register is not read out, but a new data is received (this data will be lost), overrun occurs;</p> <p>(2) In the slave transmission mode, no data is written in the data register but it still needs to transmit data (the same data is sent twice), and then underrun occurs.</p> <p>This bit can be cleared by writing 0 by software; or be cleared by hardware when I2CEN=0.</p> |
| 12    | PECEFLG  | RC_W0 | <p>PEC Error in Reception Flag</p> <p>0: No PEC error: when ACKEN=1, after receiving PEC, the receiver will return ACKEN</p> <p>1: There is PEC error; regardless of the value of ACKEN, as long as PEC is received, the receiver will return NACK</p> <p>This bit can be cleared by writing 0 by software; or be cleared by hardware when I2CEN=0.</p>                                                                                                                                                                                                                                                                          |
| 13    | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 14    | TTEFLG   | RC_W0 | <p>Timeout or Tlow Error Flag</p> <p>0: No timeout error</p> <p>1: When a timeout error occurs, in slave mode, the slave is reset and the bus is released; in master mode, the hardware transmits the stop bit.</p> <p>This bit can be set to 1 by hardware when timeout error occurs in any of the following situations:</p> <p>(1) SCL maintains low level for more than 25ms;</p> <p>(2) SCL low-level extension time of the main device is more than 10ms;</p> <p>(3) SCL low-level extension time of the slave device is more than 25ms.</p>                                                                                |

| Field | Name      | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|-----------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |           |       | This bit can be cleared by writing 0 by software; or be cleared by hardware when I2CEN=0.                                                                                                                                                                                                                                                                                                                                                      |
| 15    | SMBALTFLG | RC_W0 | <p>SMBus Alert Occur Flag</p> <p>0: SMBus master mode, without alarm;<br/>SMBus slave mode, without alarm, SMBAlert pin level unchanged</p> <p>1: SMBus master mode, with an alarm generated on the pin;<br/>SMBus slave mode, receiving an alarm, causing SMBAlert pin level to become low</p> <p>This bit can be set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it can be cleared by hardware.</p> |

### 21.7.7 State register 2 (I2C\_STS2)

Offset address: 0x18

Reset value: 0x0000

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | MSFLG      | R   | <p>Master Slave Mode Flag</p> <p>0: Slave mode<br/>1: Master mode</p> <p>This bit can be set to 1 by hardware when I2C is configured as master mode;</p> <p>This bit can be cleared by hardware when one of the following conditions is met:</p> <p>(1) Stop bit is generated<br/>(2) Bus arbitration is lost<br/>(3) I2CEN=0</p>                                                                        |
| 1     | BUSBSYFLG  | R   | <p>Bus Busy Flag</p> <p>0: The bus is idle (no communication)<br/>1: The bus is busy (in the progress of communication)</p> <p>This bit can be set to 1 by hardware when SDA or SCL is at low level; cleared by hardware after the stop bit is generated.</p>                                                                                                                                            |
| 2     | TRFLG      | R   | <p>Transmitter / Receiver Mode Flag</p> <p>0: The device is in receiver mode (read)<br/>1: The device is in transmitter mode (write)</p> <p>Decide the bit value according to R/W bit;</p> <p>This bit can be cleared by hardware when one of the following conditions is met:</p> <p>(1) Stop bit is generated<br/>(2) Repeated start bit is generated<br/>(3) Bus arbitration loss<br/>(4) I2CEN=0</p> |
| 3     | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| 4     | GENCALLFLG | R   | <p>Slave Mode Received General Call Address Flag</p> <p>0: Failed to receive the broadcast address<br/>1: Received broadcast address</p> <p>This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met:</p>                                                                                                                                            |

| Field | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|-------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |             |     | (1) Stop bit is generated<br>(2) Repeated start bit is generated<br>(3) I2CEN=0                                                                                                                                                                                                                                                                                                                                                                 |
| 5     | SMBDADDRFLG | R   | SMBus Device Received Default Address Flag in Slave Mode<br>0: Failed to receive the default address<br>1: Received the default address when ARPEN=1<br>This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met:<br>(1) Stop bit is generated<br>(2) Repeated start bit is generated<br>(3) I2CEN=0                                                                                        |
| 6     | SMMHADDR    | R   | SMBus Device Received Master Header Flag in Slave Mode<br>0: Failed to receive the master head address<br>1: Received the master head address when SMBTSEL=1 and ARPEN=1<br>This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met:<br>(1) Stop bit is generated<br>(2) Repeated start bit is generated<br>(3) I2CEN=0                                                                    |
| 7     | DUALADDRFLG | R   | Flag of receiving the double-address matching in slave mode (Slave Mode Received Dual Address Match Flag)<br>0: The received address matches the content of ADDR1 register<br>1: The received address matches the content of ADDR2 register<br>This bit can be set to 1 by hardware; and be cleared by hardware when one of the following conditions is met:<br>(1) Stop bit is generated<br>(2) Repeated start bit is generated<br>(3) I2CEN=0 |
| 15:8  | PECVALUE    | R   | Save PEC value (Save Packet Error Checking Value)<br>When PECEN=1, the internal PEC value is saved in PECVALUE.                                                                                                                                                                                                                                                                                                                                 |

### 21.7.8 Master clock control register (I2C\_CLKCTRL)

Offset address: 0x1C

Reset value: 0x0000

| Field | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                |
|-------|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:0  | CLKS [11:0] | R/W | Clock Setup in Fast/Standard Master Mode<br>In I2C standard mode or SMBus mode:<br>$T_{high} = CLKS \times T_{PCLK1}$<br>$T_{low} = CLKS \times T_{PCLK1}$<br>In I2C fast mode:<br>When FDUTYCFG=0:<br>$T_{high} = CLKS \times T_{PCLK1}$<br>$T_{low} = 2 \times CLKS \times T_{PCLK1}$<br>When FDUTYCFG=1:<br>$T_{high} = 9 \times CLKS \times T_{PCLK1}$ |

| Field | Name     | R/W | Description                                                                                                                                  |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | $T_{low} = 16 \times CLKS \times T_{PCLK1}$                                                                                                  |
| 13:12 | Reserved |     |                                                                                                                                              |
| 14    | FDUTYCFG | R/W | Fast Mode Duty Cycle Configure<br>Here it is defined that the duty cycle=tlow/thigh<br>0: SCLK duty cycle is 2<br>1: SCLK duty cycle is 16/9 |
| 15    | SPEEDCFG | R/W | Master Mode Speed Configure<br>0: Standard mode<br>1: Fast mode                                                                              |

### 21.7.9 Maximum rising time register (I2C\_RISETMAX)

Offset address: 0x20

Reset value: 0x0002

| Field | Name     | R/W | Description                                                                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------|
| 5:0   | RISETMAX | R/W | Master Mode Maximum Rise Time in Fast/Standard Mode<br>The time unit is TPCLK1, and RISETMAX is the maximum rising time of SCL plus 1. |
| 15:6  | Reserved |     |                                                                                                                                        |



## 22 Serial Peripheral Interface (SPI)

### 22.1 Full name and abbreviation description of terms

Table 93 Full name and abbreviation description of terms

| Full name in English  | English abbreviation |
|-----------------------|----------------------|
| Most Significant Bit  | MSB                  |
| Least Significant Bit | LSB                  |
| Master Out Slave In   | MOSI                 |
| Master In Slave Out   | MISO                 |
| Serial Clock          | SCK                  |
| Transmit              | TX                   |
| Receive               | RX                   |
| Busy                  | BSY                  |

### 22.2 Introduction

The SPI interface can be configured to support the SPI protocol, operating in default SPI mode.

Serial Peripheral Interface (SPI) provides data transmission and reception functions based on the SPI protocol, allowing the chip to communicate with external devices in half-duplex, full-duplex, synchronous, and serial modes. It can operate in either master or slave mode.

### 22.3 Main characteristics

- (1) Master and slave operation with 3-wire full duplex synchronous transmission and reception
- (2) Simplex synchronous transmission can be achieved by two wires (the third bidirectional data line can be included/not included)
- (3) Select 8-bit or 16-bit transmission frame format
- (4) Support multiple master device mode
- (5) Support special transmission and receiving mark and can trigger interrupt
- (6) Have SPI bus busy state flag
- (7) The SPI communication rate is up to 60Mbit/s

- (8) Clock polarity and phase are programmable
- (9) Data sequence is programmable; select MSB or LSB first
- (10) Interrupt can be triggered by master mode fault, overrun and CRC error flag
- (11) Have DMA transmit and receive buffers
- (12) SPI TI mode
- (13) Calculation, transmission and verification can be conducted through hardware CRC

## 22.4 Functional description

### 22.4.1 Description of SPI signal line

Table 94 SPI Signal Line Description

| Pin name | Description                                                                                                                                                                                                                                                                                                           |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SCK      | Master device: SPI clock outputs<br>Slave device: SPI clock inputs                                                                                                                                                                                                                                                    |
| MISO     | Master device: Input the pin and receive data<br>Slave device: Output the pin and transmit data<br>Data direction: From slave device to master device                                                                                                                                                                 |
| MOSI     | Master device: Output the pin and transmit data<br>Slave device: Input the pin and receive data<br>Data direction: From master device to slave device                                                                                                                                                                 |
| NSS      | Software NSS mode: NSS pin can be used for other purposes.<br>NSS mode of master device hardware: NSS output, single master mode.<br>NSS closed output: Operation of multiple master environments is allowed.<br>NSS mode of slave device hardware: NSS signal is set to low level as chip selection signal of slave. |

### 22.4.2 Phase and polarity of clock signal

The clock polarity and clock phase are CPOL and CPHA bits of SPI\_CTRL1 register.

Clock polarity CPOL means the level signal of SCK signal line when SPI is in idle state.

- When CPOL=0, SCK signal line is in idle state and at low level
- When CPOL=1, SCK signal line is in idle state and at high level

Clock phase CPHA means the sampling moment of data:

- When CPHA=0, the signal on MOSI or MISO data line will be sampled by the "odd edge" on SCK clock line.
- When CPHA=1, the signal on MOSI or MISO data line will be sampled by the "even edge" on SCK clock line.

SPI can be divided into four modes according to the states of clock phase CPHA and clock polarity CPOL.

Table 95 Four Modes of SPI

| SPI mode | CPHA | CPOL | Sampling moment | Idle SCK clock |
|----------|------|------|-----------------|----------------|
| 0        | 0    | 0    | Odd edge        | Low level      |
| 1        | 0    | 1    | Odd edge        | High level     |
| 2        | 1    | 0    | Even edge       | Low level      |
| 3        | 1    | 1    | Even edge       | High level     |

### 22.4.3 Data frame format

Set MSB or LSB to be first by configuring LSBSEL bit in SPI\_CTRL1 register.  
Select to transmit/receive in 8/16-bit data frame format by configuring DFLSEL bit in SPI\_CTRL1 register.

### 22.4.4 NSS mode

Software NSS mode: Select to enable or disable this mode by configuring SSSEN bit of SPI\_CTRL1 register, and the internal NSS signal level is driven by ISSEL bit of SPI\_CTRL1 register.

Hardware NSS mode:

- Turn on NSS output: When SPI is in master mode, enable SSOEN bit. NSS pin will be pulled to low level and SPI will automatically enter the slave mode.
- Turn off NSS output: Operation is allowed in multiple master environments.

### 22.4.5 SPI mode

#### 22.4.5.1 SPI master mode

In master mode, generate serial clock on SCK pin.

Master mode configuration:

- Configure MSMSEL=1 in SPI\_CTRL1 register
- Select the polarity and phase by configuring CPOL and CPHA bits in SPI\_CTRL1 register
- Select 8/16-bit data frame format by configuring DFLSEL bit in SPI\_CTRL1 register
- Select LSB or MSB first by configuring LSBSEL in SPI\_CTRL1 register
- NSS configuration:
  - NSS pin works in input mode: in hardware mode, it is required to connect NSS pin to high level during the entire data frame

transmission; in software mode, it is required to set SSEN bit and ISSEL bit in SPI\_CTRL1 register

- NSS works in output mode and it is required to configure SSOEN bit of SPI\_CTRL2 register
- Configure FRFCFG bit of SPI\_CTRL2 register to select TI mode protocol for serial communication
- Enable SPI by configuring SPIEN bit in SPI\_CTRL1 register

In master mode: MOSI pin is data output, while MISO is data input.

### **TI protocol**

In slave mode, SPI interface supports TI protocol. It is controlled by FRFCFG bit of SPI\_CTRL2 register. Both clock polarity and phase position conform to TI protocol. NSS management is specific to TI protocol, not needing to configure SPI\_CTRL1 and SPI\_CTRL2 registers.

#### **22.4.5.2 SPI slave mode**

In slave mode, SCK pin receives the serial clock transmitted from the master device.

Configuration of slave mode:

- Configure MSMSEL=0 in SPI\_CTRL1 register
- Select the polarity and phase by configuring CPOL and CPHA bits in SPI\_CTRL1 register.
- Select 8/16-bit data frame format by configuring DFLSEL bit in SPI\_CTRL1 register
- Select LSB or MSB first by configuring LSBSEL in SPI\_CTRL1 register
- NSS configuration:
  - In hardware mode: NSS pin must be at low level in the whole data frame transmission process
  - In software mode: Set SSEN bit in SPI\_CTRL1 register and clear ISSEL bit (this step is not required for TI mode)
- Configure FRFCFG bit of SPI\_CTRL2 register to select TI mode protocol for serial communication
- Enable SPI by configuring SPIEN bit in SPI\_CTRL1 register

In slave mode: MOSI pin is data input, while MISO is data output.

### **TI protocol**

In slave mode, SPI interface supports TI protocol. It is controlled by FRFCFG bit of SPI\_CTRL2 register. Both clock polarity and phase position conform to TI protocol. NSS management is specific to TI protocol, not needing to configure SPI\_CTRL1 and SPI\_CTRL2 registers.

In slave mode, SPI baud rate prescaler can use any baud rate to control the moment of switching MISO pin state to high-impedance state, so it can determine this moment very flexibly. The baud rate is generally the baud rate of external master clock. The baud rate value set by BRSEL[2:0] of SPI\_CTRL1 register and the internal circuit of the chip synchronously determine the time when the MISO pin state changes to high-impedance state.

### 22.4.5.3 Half-duplex communication of SPI

#### One clock line and one bidirectional data line

- Enable this mode by setting BMEN of SPI\_CTRL1 register
- Control the data line to be input or output by setting BMOEN bit of SPI\_CTRL1 register
- SCK pin is used as clock, MOSI pin is used in master device to transmit data, and MISO pin is used in slave device to transmit data

### 22.4.6 Data transmitting and receiving process in different SPI modes

Table 96 Run Mode of SPI

| Mode                                             | Configure        | Data pin                              |
|--------------------------------------------------|------------------|---------------------------------------|
| Full duplex mode of master device                | BMEN=0, RXOMEN=0 | MOSI transmits; MISO receives         |
| Unidirectional receiving mode of master device   | BMEN=0, RXOMEN=1 | MOSI is not used; MISO receives       |
| Bidirectional transmitting mode of master device | BMEN=1, BMOEN=1  | MOSI transmits; MISO is not used      |
| Bidirectional receiving mode of master device    | BMEN=1, BMOEN=0  | MOSI is not used; MISO receives       |
| Full duplex mode of slave device                 | BMEN=0, RXOMEN=0 | MOSI receives, and MISO transmits     |
| Unidirectional receiving mode of slave device    | BMEN=0, RXOMEN=1 | MOSI receives, while MISO is not used |
| Bidirectional transmitting mode of slave device  | BMEN=1, BMOEN=1  | MOSI is not used, and MISO transmits  |
| Bidirectional receiving mode of slave device     | BMEN=1, BMOEN=0  | MOSI receives, while MISO is not used |

Figure 86 Connection in Full Duplex Mode

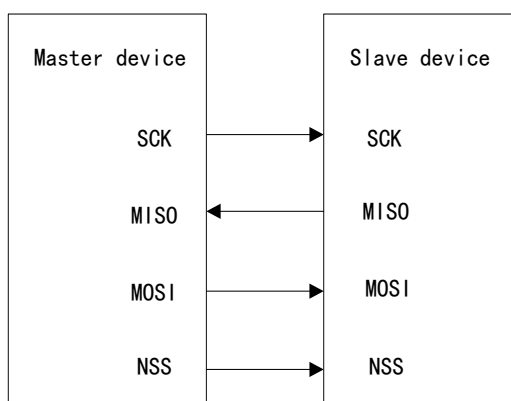


Figure 87 Connection in Half-duplex Mode (the master is used for receiving, while the slave is used for transmitting)

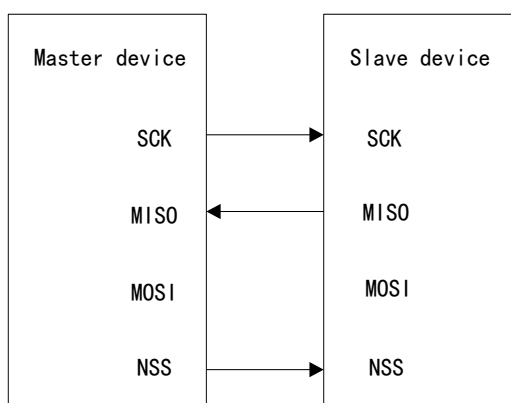


Figure 88 Connection in Half-duplex Mode (the master only transmits, while the slave receives)

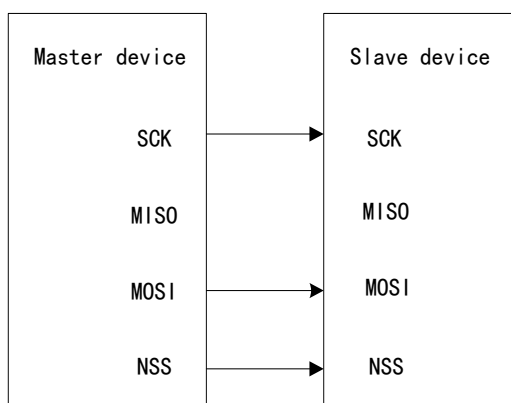
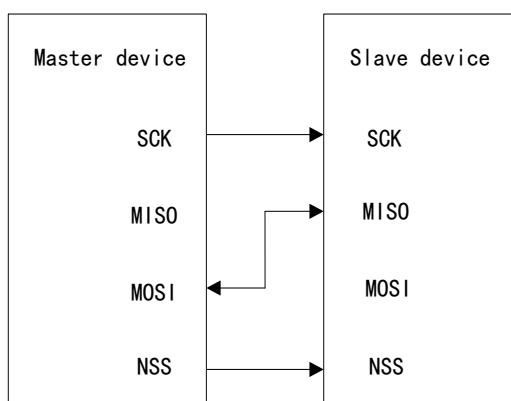


Figure 89 Bidirectional Line Connection



### 22.4.6.1 Transmitting and receiving of processed data

#### Data transmission

After the mode configuration is completed, the SPI module is enabled to remain idle.

**Master mode:** The software writes a data frame to the transmit buffer, and the transmission process starts.

**Slave mode:** The SCK signal on the SCK pin starts to jump, while the NSS pin level is low, and the transmission process starts (before starting data transmission, make sure that the data has been written to the transmit buffer in advance).

When SPI is transmitting a data frame, it will load the data frame from the data buffer to the shift register, and then start to transmit data. After one bit of data frame is sent, TXBEFLG is set to 1. If you need to continue to transmit data, the software needs to wait until TXBEFLG=1 writes data to the SPI\_DATA register. (TXBEFLG flag is set to 1 by hardware and cleared by software).

#### Data receiving

BSYFLG flag is always set to 1 in the data transmission process.

At the last edge of the sampling clock, the received data is transferred from the shift register to the receive buffer. Set the RXBNEFLG flag, and the software reads the data in data register (SPI\_DATA) to obtain the content of the receive buffer; if RXBNEIEN bit of SPI\_CTRL2 register is set, an interrupt will be generated, and after data is read, the BSYFLG flag will be automatically cleared.

### 22.4.6.2 Full duplex transmitting and receiving mode in master/slave device

#### Full duplex mode in master device

- After writing data to SPI\_DATA register (transmit buffer), data transmission starts.
- When SPI transmits the first bit of data, the data is transferred from the transmit buffer to the shift register and then transferred to the MOSI pin serially according to the sequence.
- The data received on MISO pin is serially transferred to SPI\_DATA register (receive buffer) according to the sequence.

Transmitting and receiving are synchronous.

#### **Full duplex mode under slave device**

- When the slave device receives the clock signal and the first data bit appears on the MOSI pin, data transmission starts, and the subsequent data bits will be transferred to the shift register in turn.
- When SPI transmits the first bit of data, the data is transferred from the transmit buffer to the shift register, and then transferred to the MISO pin serially according to the sequence.
- The software must ensure that the data to be sent is written before the SPI master device starts to transmit data.

Transmitting and receiving are synchronous.

#### **Full duplex transmitting and receiving process under master/slave device**

- (1) Enable SPI module: Configure SPIEN=1 of SPI\_CTRL1 register.
- (2) Write the first data to be sent to SPI\_DATA register, and the TXBEFLG flag will be cleared.
- (3) Wait until TXBEFLG flag bit is set to 1 (control by hardware), and write the second data bit to be sent.
- (4) Wait until RXBNEFLG flag bit is set to 1 (control by hardware), read the first received data in the SPI\_DATA register, at the same time, clear the RXBNEFLG flag (cleared by software). Repeat the operation, and transmit and receive data at the same time.
- (5) Wait until RXBNEFLG=1 and receive the last data.
- (6) Wait until TXBEFLG=1 and close SPI module after BSYFLG=0.

### **22.4.6.3 Bidirectional transmitting mode of master/slave device**

#### **Bidirectional transmission of master device**

- Write data to SPI\_DATA register, and the transmission starts
- The data in the transmit buffer is transferred to the shift register in parallel, and then transferred to the MOSI pin serially according to the sequence.



### **Bidirectional transmission of slave device**

- When the slave device receives the clock signal and the first data bit appears on the MISO pin, data transmission starts.
- At the same time, the data to be sent by the transmit buffer is transferred to the shift register in parallel, and then sent to the MISO pin in serial (before data transmission, make sure that the data has been written to the transmit buffer in advance).

### **Bidirectional transmission process of master/slave device**

- (1) Enable SPI module: Configure SPIEN=1 of SPI\_CTRL1 register.
- (2) Write the first data to be sent to SPI\_DATA register, and the TXBEFLG flag will be cleared.
- (3) Wait until TXBEFLG=1, write the second data, repeat the operation and transmit the subsequent data
- (4) After writing the last data, wait for TXBEFLG=1 and BSYFLG=0 and transmission is completed

#### **22.4.6.4 One-way/Two-way receiving mode under master/slave device**

- (1) Enable SPI module: Configure SPIEN=1 of SPI\_CTRL1 register.
- (2) In the master device: Generate SCK clock immediately, and continuously receive data before SPI is disabled.
- (3) Slave device: When SPI master device pulls down NSS and generates clock, receive data.
- (4) Wait until the RXBNEFLG flag is set to 1, read data through SPI\_DATA, and repeat the operation to receive data.

#### **22.4.7 CRC functions**

SPI module contains two CRC computing units, which are used for data receiving and data transmission respectively.

CRC computing unit is used to define polynomials in SPI\_CRCPOLY register.

Enable CRC computing by configuring CRCEN bit in SPI\_CTRL1 register; at the same time, reset the CRC register (SPI\_RXCRC and SPI\_TXCRC).

To obtain the CRC value of transmission calculation, after the last data is written to the transmit buffer, it is required to set CRCNXT bit of SPI\_CTRL1; indicate that the hardware transmits the CRC value after the last data is sent, and the CRCNXT bit will be cleared; at the same time, compare the values of CRC and SPI\_RXCRC, and if they do not match, it is required to set CRCEFLG bit of SPI\_STS register, and after ERRIEN bit of SPI\_CTRL2 register is set, an interrupt will occur.

Note:

- (1) If SPI is under slave device and CRC function is used, CRC computing will continue when NSS pin is at high level. For example, when the master device communicates with multiple slave devices alternately, the above situation will occur, so it is necessary to avoid faulty operation of CRC.
- (2) In the process of a slave device from being unselected (NSS is at high level) to being selected (NSS is at low level 0), it is required to clear the CRC value at both ends of the master and slave devices to keep the next CRC computing results of the master and slave devices synchronized.
- (3) When SPI is in slave mode, CRC computing can be enabled after the clock is stable.
- (4) When the SPI clock frequency is too high, the CPU operation will affect the SPI bandwidth. It is recommended to use DMA mode to avoid the reduction of SPI speed.
- (5) When the SPI clock frequency is too high, during the CRC transmission period, the CPU utilization frequency is reduced, and the function call is disabled in the CRC transmission process to avoid errors when receiving the last data and CRC.
- (6) When NSS hardware mode is used in slave mode, NSS pin should be kept low during data transmission and CRC transmission period.

### Sequence of clearing CRC values

- (1) Disable SPI (SPIEN=0)
- (2) Clear CRCEN bit
- (3) Set CRCEN bit to 1
- (4) Enable SPI (SPIEN=1)

## 22.4.8 DMA function

For high-speed data transmission, the request/response DMA mechanism in SPI improves the system efficiency and can transfer data to SPI transmit buffer promptly, and the receive buffer can read the data in time to prevent overflow.

When SPI only transmits data, it is only needed to enable DMA transmission channel; when SPI only receives data, it is only needed to enable DMA receiving channel.

DMA function of SPI mode can be enabled by configuring TXDEN and RXDEN bits of SPI\_CTRL2 register.

- When transmitting: When TXBEFLG flag bit is set to 1, issue the DMA request, DMA controller writes data to SPI\_DATA register, and then the TXBEFLG flag bit will be cleared.

- When receiving: When setting RXBNEFLG flag bit to 1, issue the DMA request, DMA controller reads data from SPI\_DATA register, and then RXBNEFLG flag bit is cleared.

By monitoring BSYFLG flag bit, confirm whether SPI communication is over after DMA has transferred all data to be sent in transmitting mode, which can avoid damaging the transmission of last data.

### **DMA function with CRC**

By the end of communication, if SPI enables both CRC operation and DMA function, transmitting and receiving of CRC bytes will be completed automatically.

At the end of data and CRC transmission, if CRCEFLG flag bit of SPI\_STS register is set to 1, it indicates that an error occurred during transmission.

### **22.4.9 Disable SPI**

After data transmission is over, end the communication by closing SPI module. In some configurations, if SPI is disabled before data transmission is completed, data transmission error may be caused. Different methods are required in different operation modes to close SPI.

#### **Maser mode/full-duplex slave mode**

- (1) Wait until RXBNEFLG flag bit is set to 1, and receive the last data
- (2) Wait until TXBEFLG flag bit is set to 1
- (3) Wait for clearing BSYFLG flag bit
- (4) Close SPI (set SPIEN=0 of SPI\_CTRL1 register)

#### **One-way transmit-only/bidirectional transmitting mode of master mode/slave mode**

After the last data is written into SPI\_DATA register:

- (1) Wait until TXBEFLG flag bit is set to 1
- (2) Wait for clearing BSYFLG flag bit
- (3) Close SPI (set SPIEN=0 of SPI\_CTRL1 register)

#### **One-way receive-only/bidirectional receiving mode of master mode/slave mode**

- (1) Wait No. n-1 RXBNEFLG flag bit is set to 1
- (2) Wait for one SPI clock cycle before SPI is disabled (set SPIEN=0 of SPI\_CTRL1 register)

- (3) Before entering the stop mode, wait until the last RXBNEFLG flag bit is set to 1

### **Receive-only/bidirectional receiving mode in slave mode**

SPI can be disabled at any time (set SPIEN=0 of SPI\_CTRL1 register) and it will be disabled when the transmission is over. If you want to enter the stop mode, wait until BSYFLG flag bit is cleared.

## **22.4.10 SPI interrupt**

### **22.4.10.1 State flag bit**

#### **Transmit buffer empty flag TXBEFLG**

TXBEFLG=1 indicates that the transmit buffer bit is empty, and the next data to be sent can be written. When the data is written to SPI\_DATA register, clear the TXBEFLG flag bit.

#### **Receive buffer non-empty flag RXBNEFLG**

RXBNEFLG=1 indicates that the receive buffer contains valid data and the data can be read through SPI\_DATA register; and the RXBNEFLG flag can be cleared.

#### **Busy flag BSYFLG**

BSYFLG flag is set and cleared by hardware, which can indicate the state of SPI communication layer. When BSYFLG=1, it indicates SPI is communicating, but in the two-line receiving mode under the master device, BSYFLG=0 during the period of receiving of data.

BSYFLG flag can be used to detect whether transmission is over to avoid damaging the last transmitted data.

BSYFLG flag bit can be used to avoid conflict when writing data in multi-master mode.

BSYFLG flag will be cleared when the transmission ends (except for continuous communication in master mode), SPI is disabled and the master mode fails.

BSYFLG=0 between data item and data item when communication is discontinuous.

When communication is continuous:

- In master mode: BSYFLG=1 in the whole transmission process
- In slave mode: BSYFLG is kept low within one SCK clock cycle between transmission of each data

Note: It is best to use TXBEFLG and RXBNEFLG flags to process the transmitting and receiving of each data item.

## 22.4.10.2 Error flag bit

### Master mode error MEFLG

MEFLG is an error flag bit. The master mode error occurs when: in hardware NSS mode, the NSS pin of the master device is pulled down; in software NSS mode, ISSEL bit is cleared; MEFLG bit is set automatically.

Influence of master mode failure: MEFLG is set to 1, and SPI interrupt is generated when ERRIEN is set; SPIEN is cleared (output stops, SPI interface is disabled); MSMSEL is cleared and the device is forced into the slave mode.

Operation of clearing the MEFLG flag bit: When MEFLG bit is set to 1, it is required to read or write SPI\_STS register, and then write to SPI\_CTRL1 register.

When MEFLG flag bit is 1, it is not allowed to set SPIEN and MSMSEL bits.

### Overrun error OVRFLG

Overrun error: After the master device transmits the data, the RXBNEFLG flag bit is still 1, which indicates that the overrun error occurred. Then OVRFLG bit is set to 1, and if the ERRIEN bit is also set, an interrupt will be generated.

After an overrun error occurs, the data in the receive buffer is not the data sent by the master device, and then the read data in SPI\_DATA register is the data not read before, while the data sent later will not be read.

OVRFLG flag can be cleared by reading SPI\_DATA register and SPI\_STS register according to the sequence.

### CRC error flag CRCEFLG

By setting CRCEN bit of SPI\_CTRL1 register, start CRC computing, CRC error flag, and check whether the received data is valid.

When the value sent by SPI\_TXCRC register does not match the value in SPI\_RXCRC register, a CRC error will be generated, and CRCEFLG flag bit in SPI\_STS register will be set to 1.

CRCEFLG can be cleared by writing 0 to CRCEFLG bit of SPI\_STS register.

### TI frame format error flag FREFLG

If SPI supports TI protocol in slave mode, TI frame format error will be detected when NSS pulse occurs during communication. When this error appears, SPI\_STS[FREFLG]=1, SPI will not be disabled, but NSS pulse will be ignored, and SPI will start new transmission when next NSS pulse arrives. As the error detection may cause the loss of two data bytes, the data may have been damaged.

FREFLAG flag will be cleared when reading SPI\_STS register. If ERRIEN=1, and a frame format error is detected, an interrupt will be generated. The continuity of data cannot be guaranteed at this time, the SPI shall be disabled and after the slave SPI is enabled again, the master will restart the communication.

Table 97 SPI Interrupt Request

| Interrupt flag | Interrupt event               | Enable control bit | Clearing method                                                |
|----------------|-------------------------------|--------------------|----------------------------------------------------------------|
| TXBEFLAG       | Transmit buffer empty flag    | TXBEIEN            | Write SPI_DATA register                                        |
| RXBNEFLAG      | Receive buffer non-empty flag | RXBNEIEN           | Read SPI_DATA register                                         |
| MEFLAG         | Master mode failure event     | ERRIEN             | Read/Write SPI_STS register, and then write SPI_CTRL1 register |
| OVRFLAG        | Overrun error                 |                    | Read SPI_DATA register, and then read SPI_STS register         |
| CRCEFLAG       | CRC error flag                |                    | Write 0 to CRCEFLAG bit                                        |
| FREFLAG        | TI frame format error         |                    | Read SPI_STS register                                          |

## 22.5 Register address mapping

Table 98 SPI Register Address Mapping

| Register name | Description                 | Offset address |
|---------------|-----------------------------|----------------|
| SPI_CTRL1     | SPI control register 1      | 0x00           |
| SPI_CTRL2     | SPI control register 2      | 0x04           |
| SPI_STS       | SPI state register          | 0x08           |
| SPI_DATA      | SPI data register           | 0x0C           |
| SPI_CRCPOLY   | SPI CRC polynomial register | 0x10           |
| SPI_RXCRC     | SPI receive CRC register    | 0x14           |
| SPI_TXCRC     | SPI transmit CRC register   | 0x18           |

## 22.6 Register functional description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

### 22.6.1 SPI control register 1 (SPI\_CTRL1)

Offset address: 0x00

Reset value: 0x0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                             |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CPHA   | R/W | <p>Clock Phase Configure</p> <p>This bit indicates on the edge of which clock to start sampling</p> <p>0: On the edge of No. 1 clock</p> <p>1: On the edge of No. 2 clock</p> <p>Note: This bit cannot be modified during communication.</p>                                            |
| 1     | CPOL   | R/W | <p>Clock Polarity Configure</p> <p>Level state maintained by SCK when SPI is in idle state.</p> <p>0: Low level</p> <p>1: High level</p> <p>Note: This bit cannot be modified during communication.</p>                                                                                 |
| 2     | MSMCFG | R/W | <p>Master/Slave Mode Configure</p> <p>0: Configure as slave mode</p> <p>1: Configure as master mode</p> <p>Note: This bit cannot be modified during communication.</p>                                                                                                                  |
| 5:3   | BRSEL  | R/W | <p>Baud Rate Divider Factor Select</p> <p>000: DIV=2</p> <p>001: DIV=4</p> <p>010: DIV=8</p> <p>011: DIV=16</p> <p>100: DIV=32</p> <p>101: DIV=64</p> <p>110: DIV=128</p> <p>111: DIV=256</p> <p>Baud rate=FPCLK/DIV</p> <p>Note: This bit cannot be modified during communication.</p> |
| 6     | SPIEN  | R/W | <p>SPI Device Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>Note: When SPI device is disabled, operate according to the process of closing SPI.</p>                                                                                                                                  |
| 7     | LSBSEL | R/W | <p>LSB First Transfer Select</p> <p>0: First transmit the most significant bit (MSB)</p> <p>1: First transmit the least significant bit (LSB)</p>                                                                                                                                       |
| 8     | ISSEL  | R/W | <p>Internal Slave Device Select</p> <p>When CTRL1_SSEN=1 (software NSS mode), select internal NSS level by configuring the bit</p> <p>0: Internal NSS is low</p> <p>1: Internal NSS is high</p>                                                                                         |
| 9     | SSEN   | R/W | <p>Software Slave Device Enable</p> <p>0: Software NSS mode is disabled, and the internal NSS level is determined by external NSS pin</p> <p>1: Software NSS mode is enabled, and the internal NSS level is determined by the ISSEL bit in the SPI_CTRL1 register.</p>                  |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                               |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10    | RXOMEN | R/W | Receive Only Mode Enable<br>0: Transmit and receive at the same time<br>1: Receive-only mode<br>RXOMEN bit and BMEN bit together determine the transmission direction in the two-line and two-way mode. In the configuration of multiple slave devices, in order to avoid data transmission collision, it is necessary to set RXOMEN bit to 1 on the slave devices that are not accessed. |
| 11    | DFLSEL | R/W | Data Frame Length Format Select<br>0: 8-bit data frame format<br>1: 16-bit data frame format<br>Note: To ensure proper operation, write to this bit only when SPI (SPIEN = "0") is disabled.                                                                                                                                                                                              |
| 12    | CRCNXT | R/W | CRC Transfer Next Enable<br>0: The next transmitted data is from transmit buffer<br>1: The next transmitted data is from CRC register<br>Note: After the last data is written to SPI_DATA register, set CRCNXT bit immediately.                                                                                                                                                           |
| 13    | CRCEN  | R/W | CRC Calculate Enable<br>0: Disable<br>1: Enable<br>CRC check function only applies to full duplex mode.<br>Note: To ensure proper operation, write to this bit only when SPI (SPIEN = "0") is disabled.                                                                                                                                                                                   |
| 14    | BMOEN  | R/W | Bidirectional Mode Output Enable<br>0: Disable, namely, receive-only mode<br>1: Enable, namely, transmit-only mode<br>When BMEN=1, that is in single-line bidirectional mode, this bit decides the transmission direction.                                                                                                                                                                |
| 15    | BMEN   | R/W | Bidirectional Mode Enable<br>0: Double-line unidirectional mode<br>1: Single-line bidirectional mode<br>Single-line two-way transmission: the transmission between MOSI pin of data master and MISO pin of slave.                                                                                                                                                                         |

## 22.6.2 SPI control register 2 (SPI\_CTRL2)

Offset address: 0x04

Reset value: 0x0000

| Field | Name  | R/W | Description                                                                                                                  |
|-------|-------|-----|------------------------------------------------------------------------------------------------------------------------------|
| 0     | RXDEN | R/W | Receive Buffer DMA Enable<br>When RXDEN=1, once RXBNEFLG flag is set, DMA request will be issued.<br>0: Disable<br>1: Enable |



| Field | Name     | R/W | Description                                                                                                                                                                          |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | TXDEN    | R/W | Transmit Buffer DMA Enable<br>When this bit is set, once TXBEFLG flag is set, DMA request will be issued.<br>0: Disable<br>1: Enable                                                 |
| 2     | SSOEN    | R/W | SS Output Enable<br>SS output in master mode<br>0: SS output is disabled, and it can work in multi-master mode.<br>1: SS output is enabled, and it cannot work in multi-master mode. |
| 3     | Reserved |     |                                                                                                                                                                                      |
| 4     | FRFCFG   | R/W | Frame Format Configure<br>0: SPI Motorola mode<br>1: SPI TI mode                                                                                                                     |
| 5     | ERRIEN   | R/W | Error interrupt Enable<br>0: Disable<br>1: Enable<br>When an error occurs, ERRIEN bit controls whether to generate the interrupt.                                                    |
| 6     | RXBNEIEN | R/W | Receive Buffer Not Empty Interrupt Enable<br>0: Disable<br>1: Allowed<br>When RXBNEFLG flag bit is set to 1, an interrupt request will be generated.                                 |
| 7     | TXBEIEN  | R/W | Transmit Buffer Empty Interrupt Enable<br>0: Disable<br>1: Enable<br>When TXBEFLG flag bit is set to 1, an interrupt request will be generated.                                      |
| 15:8  | Reserved |     |                                                                                                                                                                                      |

### 22.6.3 SPI state register (SPI\_STS)

Offset address: 0x08

Reset value: 0x0002

| Field | Name     | R/W | Description                                               |
|-------|----------|-----|-----------------------------------------------------------|
| 0     | RXBNEFLG | R   | Receive Buffer Not Empty Flag<br>0: Empty<br>1: Not empty |
| 1     | TXBEFLG  | R   | Transmit Buffer Empty Flag<br>0: Not empty<br>1: Empty    |
| 3:2   | Reserved |     |                                                           |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                    |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4     | CRCEFLG  | RC_W0 | CRC Error Occur Flag<br>This bit indicates whether the received CRC value matches the value of RXCRC register<br>0: Match<br>1: Not match<br>This bit is set by hardware, can be cleared by writing 0 to this bit by software. |
| 5     | MEFLG    | R     | Mode Error Occur Flag<br>0: Not occur<br>1: Occurred<br>This bit is set by hardware.                                                                                                                                           |
| 6     | OVRFLG   | R     | Overflow Occur Flag<br>0: Not occur<br>1: Occurred<br>This bit is set by hardware.                                                                                                                                             |
| 7     | BSYFLG   | R     | SPI Busy Flag<br>0: SPI is idle<br>1: SPI is communicating<br>It is set or cleared by hardware.                                                                                                                                |
| 8     | FREFLG   | R     | Frame Format Error Flag<br>0: Not occur<br>1: Occurred<br>Note: This flag is used when working in TI slave mode. This bit is set to 1 by hardware and cleared to 0 when reading SPI_STS register.                              |
| 15:9  | Reserved |       |                                                                                                                                                                                                                                |

#### 22.6.4 SPI data register (SPI\_DATA)

Offset address: 0x0C

Reset value: 0x0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | DATA | R/W | Transmit Receive Data register<br>When writing this register, the data will be written to the transmit buffer; when reading this register, the data in receive buffer will be read.<br>The size of the buffer is consistent with the length of the data frame, that is, for 8-bit data, only DATA[7:0] is used when transmitting and receiving data, and DATA[15:8] is invalid; for 16-bit data, DATA[15:0] will be used when transmitting and receiving data. |

#### 22.6.5 SPI CRC polynomial register (SPI\_CRCPOLY)

Offset address: 0x10

Reset value: 0x0007

| Field | Name    | R/W | Description                                                                                                                                 |
|-------|---------|-----|---------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | CRCPOLY | R/W | CRC Polynomial Value Setup<br>This register contains CRC polynomial of CRC computing, which can be modified, and the reset value is 0x0007. |

## 22.6.6 SPI receive CRC register (SPI\_RXCRC)

Offset address: 0x14

Reset value: 0x0000

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | RXCRC | R   | <p>Receive Data CRC Value</p> <p>The CRC data of receive data calculated by hardware are stored in this register; the bits and the length of data frames are consistent, that is, if the received data are 8 bits, the CRC computing is made based on CRC8; if the received data are 16 bits, the CRC computing is made based on CRC16.</p> <p>When CRCEN is set, the hardware clears the register.</p> <p>Note: When BSYFLG bit is set to 1, the value of reading RXCRC register may be wrong.</p> |

## 22.6.7 SPI transmit CRC register (SPI\_TXCRC)

Offset address: 0x18

Reset value: 0x0000

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | TXCRC | R   | <p>Transmit Data CRC Value</p> <p>The CRC data of sent data calculated by hardware are stored in this register; the bits and the length of data frames are consistent, that is, if the sent data are 8 bits, the CRC computing is based on CRC8; if the sent data is are 16 bits, the CRC computing is based on CRC16.</p> <p>When CRCEN is set, the hardware clears the register.</p> <p>Note: When BSYFLG bit is set to 1, the value of reading RXCRC register may be wrong.</p> |

## 23 Quad Serial Peripheral Interface (QSPI)

### 23.1 Full name and abbreviation description of terms

Table 99 Full name and abbreviation description of terms

| Full name in English                                | English abbreviation |
|-----------------------------------------------------|----------------------|
| Quad Serial Peripheral Interface                    | QSPI                 |
| Electrically Erasable Programmable Read-Only Memory | EEPROM               |

### 23.2 Introduction

QSPI is a serial data bus interface consisting of a clock (SCLK), chip select signal (CS), and four data lines (IO[0:3]). It connects to external SPI Flash storage media using single, dual, or quad lines. The interface supports four modes: transmit and receive, transmit only, receive only, and EEPROM read. The modes are controlled by software.

### 23.3 Main characteristics

- (1) Programmable clock polarity and clock phase
- (2) Integrated FIFO for transmission and reception, with a depth of 8 and a data width of 32 bits
- (3) Support four transmission modes, enabling data frame sizes ranging from 4 bits to 32 bits
- (4) Support hardware or software to control chip select signals
- (5) In four-wire transmission mode, support clock delay extension
- (6) Support variable command length, address length, wait cycles, and data frame size
- (7) Programmable delay for sampling time during serial data reception, enabling higher serial data bit sampling rates

### 23.4 Functional description

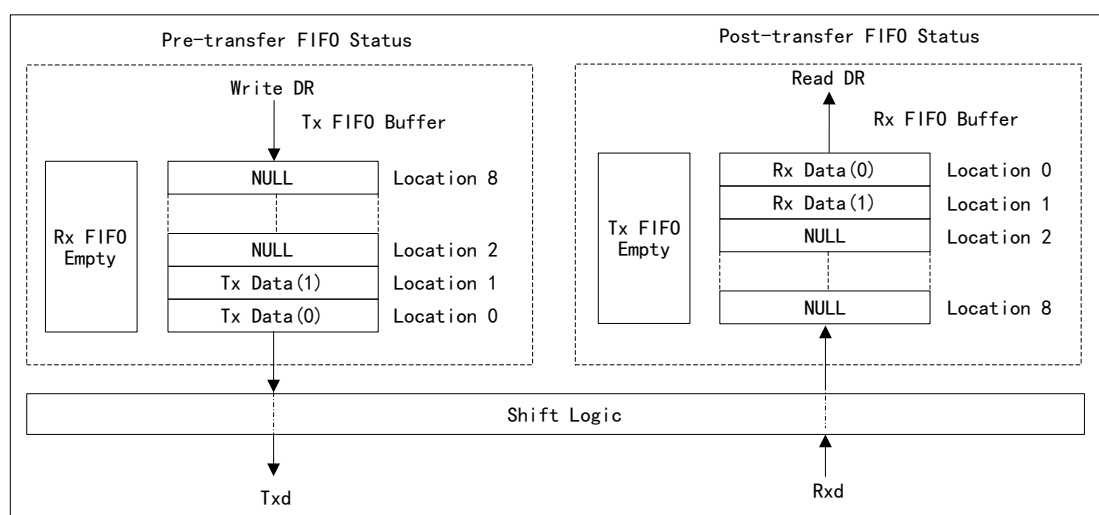
#### 23.4.1 Transfer modes

This section discusses the operation of the QSPI in different modes during serial bus data transfer. The transmission mode (TXMODE) is determined by the control register 1 (QSPI\_CTRL1) through the TXMODE bits.

#### Transmit and Receive

When TXMODE = 2'b00, both transmit and receive logic are enabled. Transmission begins when data is written into the transmit FIFO and the number of data units exceeds the transmit threshold (TFTH) in the QSPI\_TFTL register. Serial data is sent to the transmit data line and reaches the target device. Meanwhile, data on the receive data line is transferred from the receive shift register into the receive FIFO.

Figure 90 QSPI Transfer FIFO Status in the Transmit and Receive States

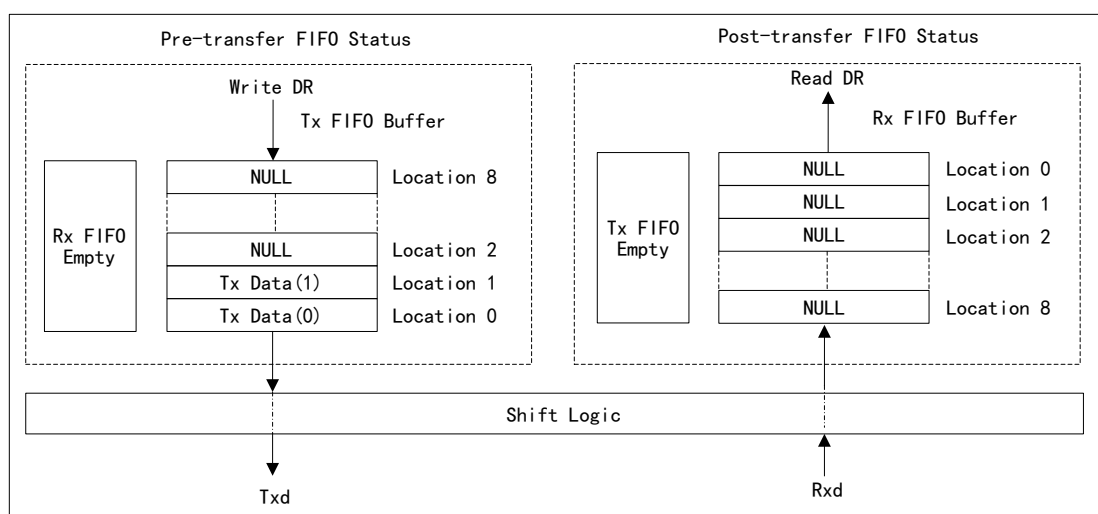


### Transmit-only

When TXMODE = 2'b01, only the transmission logic unit is active. The reception logic unit is inactive. When data is written into the transmit FIFO and the number of data exceeds the FIFO transmission threshold (TFTH in the QSPI\_TFTL register), the transfer begins. The data is then serially sent out through the transmission data line to the target device. Data on the receive data line will be ignored. As a result, no data will be stored in the receive FIFO.

The following images show the FIFO levels before the start of serial transmission and after the transmission is completed. In this example, two data frames are transmitted from QSPI to an external serial device in a continuous transfer mode.

Figure 91 QSPI Transfer FIFO Status in the Transmit State

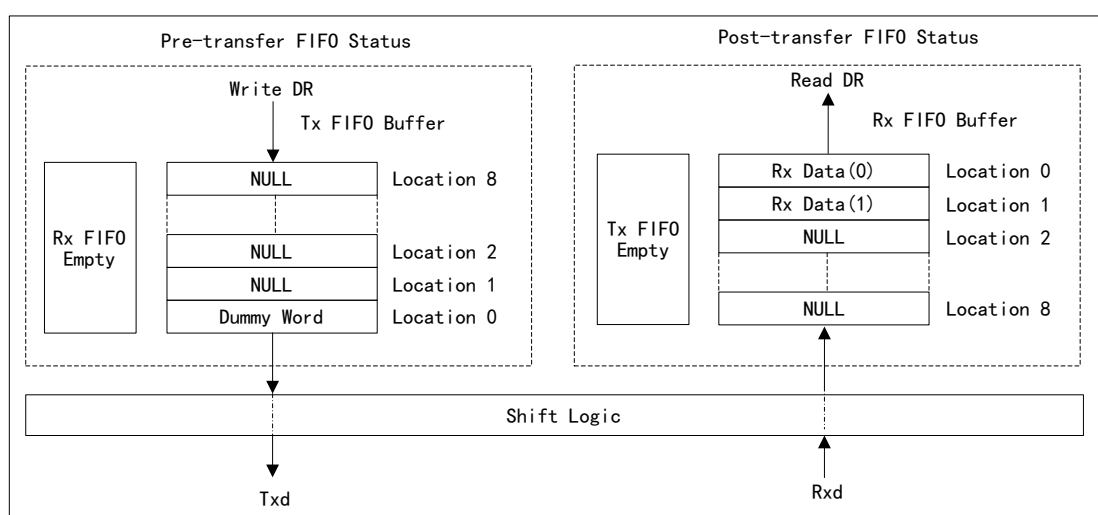


### Receive-only

When TXMODE = 2'b10, only the reception logic unit is active, and the transmission logic unit is inactive. No data will be sent. Data on the receive data line will be transferred from the receive shift register to the receive FIFO. To start a transfer, an invalid data needs to be written into the transmit FIFO.

The following images show the FIFO levels before the start of serial transmission and after the transmission is completed. In this example, QSPI continuously receives two data frames from an external serial device.

Figure 92 QSPI Transfer FIFO Status in the Receive Mode



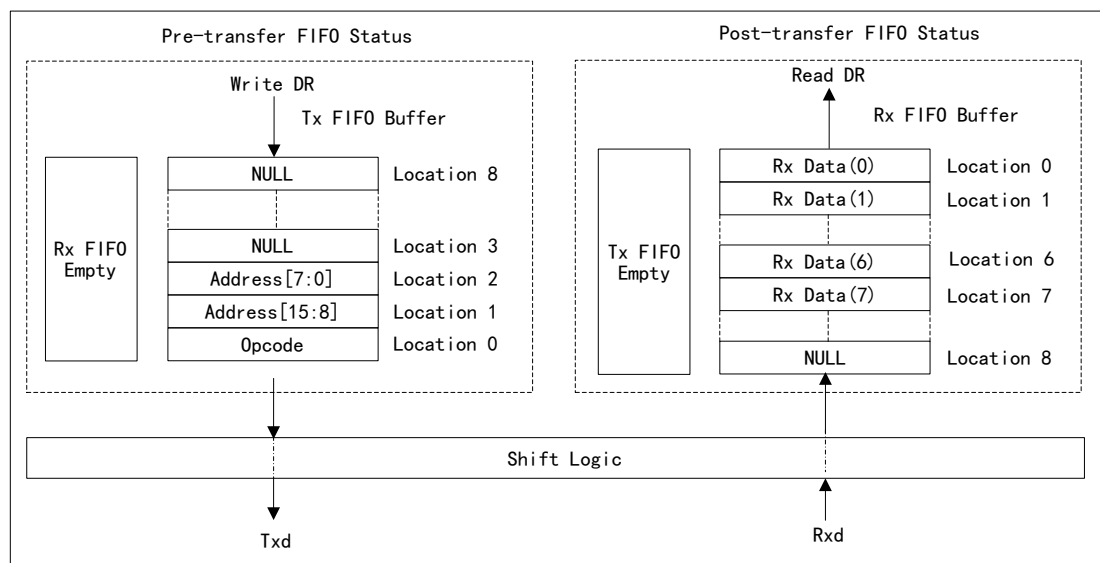
### EEPROM Read

When TXMODE = 2'b11, the transmitted data is used to send commands/addresses to the corresponding external device. Typically, three data frames are required (8-bit command code, 8-bit high address, 8-bit low

address). During the data transmission process, the reception logic unit will not capture any data on the receive data line until the transmit FIFO is empty. That is, when the transmission FIFO is empty, the reception logic unit becomes active and starts receiving data until the number of received data frames in QSPI matches the value of the NDF field in the QSPI\_CTRL2 register plus one.

The following images show the FIFO levels before the start of serial transfer and after the transfer is completed. In this example, QSPI continuously receives two data frames from an external serial device.

Figure 93 FIFO Status in EEPROM Read Transfer Mode



### 23.4.2 Data transfer

Data transfer is initiated by an external master device. After entering the transmit FIFO, the number of valid data exceeds the threshold set by the TFTH field in the QSPI\_TFTL register, and an external slave device is selected. During data transmission, the register status is set to the BUSY flag. A new external transfer can only be attempted after the BUSY flag is cleared.

### 23.4.3 Clock ratio

#### Clock Ratio Descriptions

QSPI operates in an oversampling architecture. For the host mode of operation, the peripheral device clock (sclk\_out) period is a multiple of the core clock (qspi\_clk).

When the QSPI macro unit is configured as a master device, the maximum frequency of the bit rate clock (sclk\_out) is half of the qspi\_clk frequency. This allows the shift control logic to capture data on one edge of sclk\_out and derive data on the opposite edge.

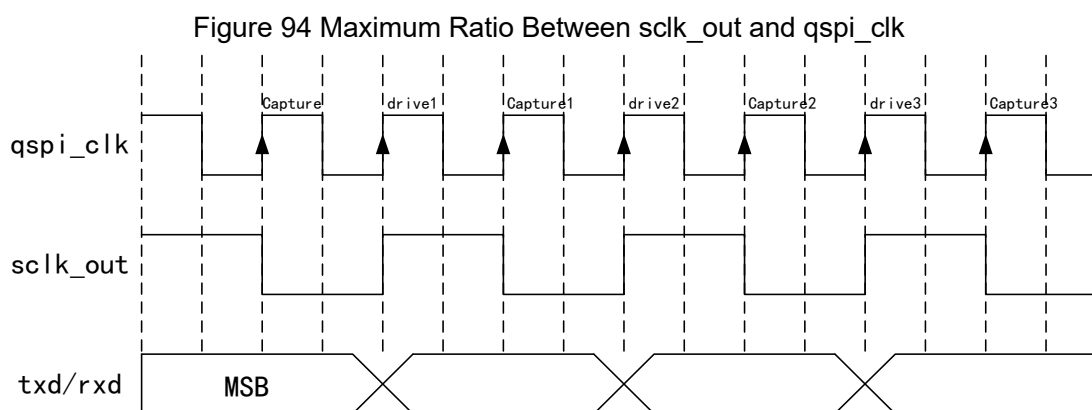
The sclk\_out frequency can be calculated using the following formula:

$$F_{\text{sclk\_out}} = F_{\text{qspi\_clk}} / \text{SCKDIV}$$

Note:

- (1) SCKDIV is a programmable register that ranges between 0 and 65534. If SCKDIV = 0, sclk\_out is disabled.
- (2) sclk\_out line only toggles during active data transfers. During other times, it remains in an inactive state.

The diagram below illustrates the maximum ratio between sclk\_out and qspi\_clk.



### Maximum Frequency Ratio Overview

The frequency ratio rule between (sclk\_out / sclk\_in) bit rate and QSPI peripheral device clock (qspi\_clk) is summarized as follows:

$$F_{\text{qspi\_clk}} \geq 2 \times (\text{maximum } F_{\text{sclk\_out}})$$

#### 23.4.4 Receive and Transmit FIFO buffer

The FIFO buffers used by QSPI are internal D-type flip-flops. According to the serial protocol, a serial transfer (data frame) length ranges from 4 to 32 bits, so the length of both the transmit FIFO and receive FIFO buffers is fixed at 32 bits. Data frames smaller than 32 bits must be right-aligned when written into the transmit FIFO. The shift control logic automatically adjusts the received data in the receive FIFO to be right-aligned. The QSPI\_TFTL register determines the FIFO threshold level at which an interrupt is generated.

When the AHB issues a read command to the QSPI\_DATA register, data will be popped from the receive FIFO. A FIFO full interrupt request (qspi\_rxf\_intr) is triggered when the number of FIFO entries is greater than or equal to the threshold plus one. The threshold set by the programmable register QSPI\_RFTL determines the FIFO entry level at which this interrupt is generated.

The threshold allows the processor to be notified when the FIFO is about to empty. When the receive shift logic attempts to transfer data to a nearly full receive FIFO, a receive FIFO overflow interrupt occurs. In this case, the new



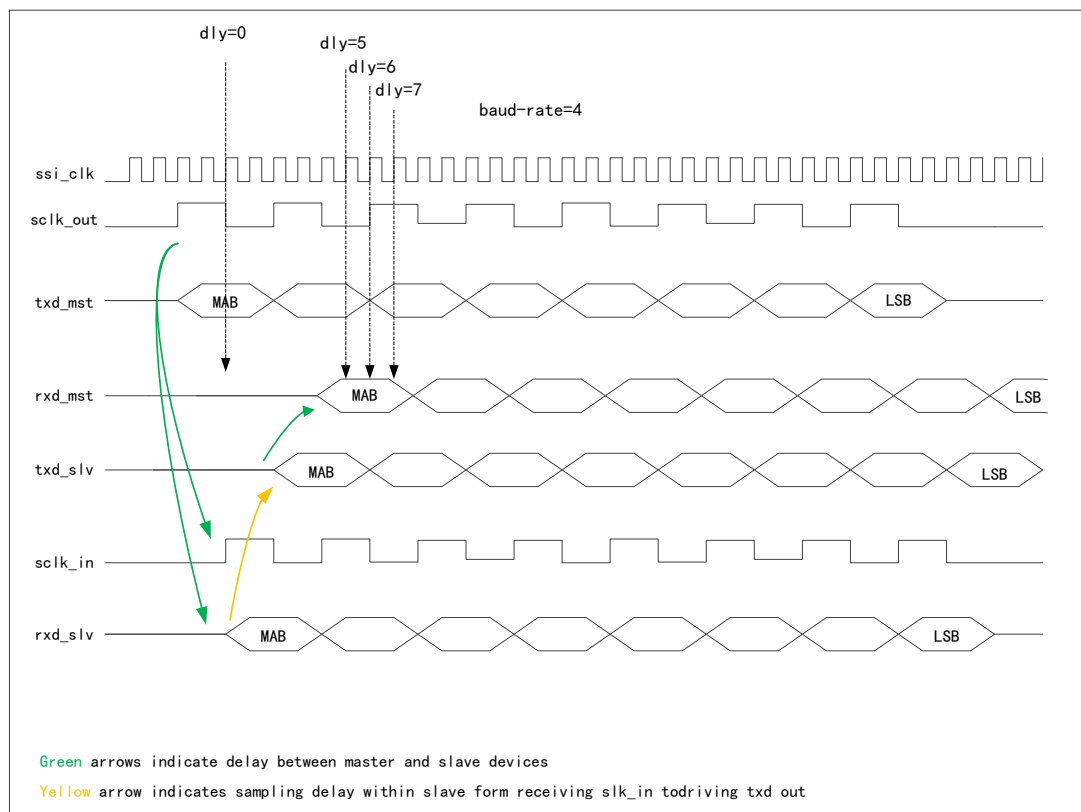
received data will be lost. Conversely, attempting to read data from an empty receive FIFO will generate a receive FIFO underflow interrupt, warning the processor that the data read is invalid.

### 23.4.5 Receive Data (RXD) Sampling Delay

When QSPI is configured as a master, additional logic can be incorporated into the design to delay the default sampling time of the received data signal. This extra logic helps improve the maximum achievable frequency of the serial bus.

The delay along the round-trip path between the `sclk_out` signal issued by the master and the RXD signal issued by the slave can be considered as the timing of the received signal. From the master's perspective, this delay means that the signal has already left the normal sampling window. The following diagram illustrates this situation:

Figure 95 Description of Receive Data (RXD) Sampling Delay



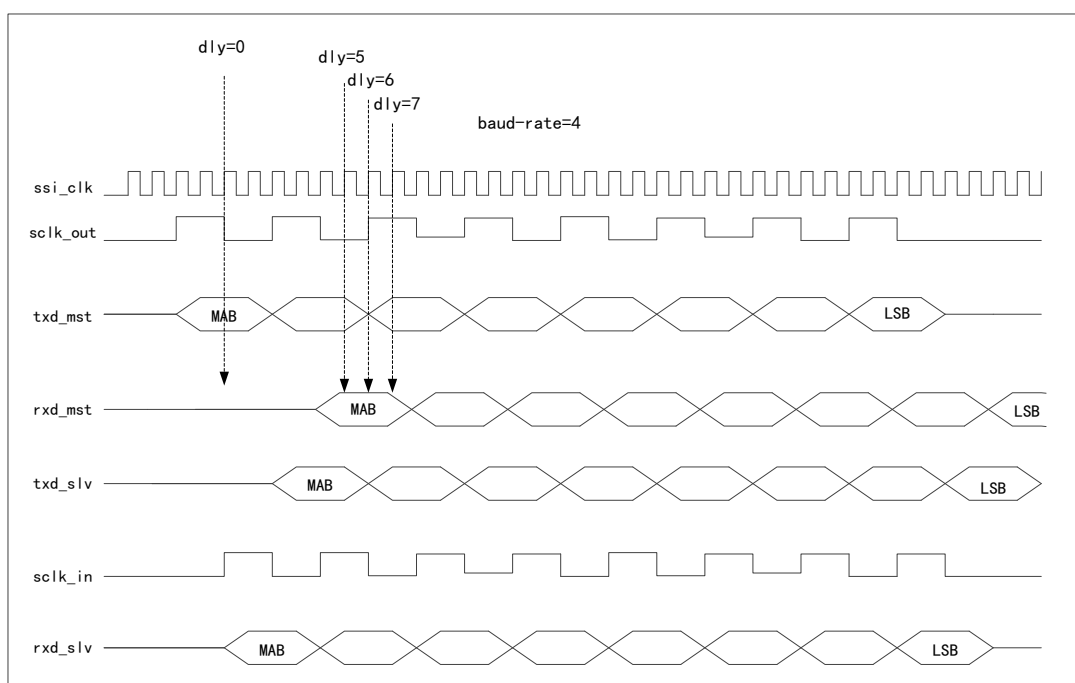
The slave uses the master's `sclk_out` signal as a gate to obtain the data mapping of the RXD signal onto the serial bus. The delay in routing and sampling the `sclk_out` signal from the slave device means that, before the master samples the RXD signal, the RXD bit has not yet stabilized to the correct value.

The following diagram illustrates how routing delay of the RXD signal can produce incorrect RXD values at the default sampling time of the master port.

Without receive sample delay logic, increasing the transfer baud rate would be necessary to ensure that the sampling time of the received data signal remains within the valid range, which would result in a decrease in the serial interface frequency.

When the RXD sample delay logic is included, the delay value can be dynamically adjusted so that the sampling time of the RXD signal shifts from the default to a number of qspi\_clk cycles. The RXD sample delay logic can be configured to collect RXD signal samples on both the positive and negative edges of the qspi\_clk. This approach increases the number of sampling points within one sclk\_out cycle and helps meet timing requirements at higher frequencies. QSPI adjusts the sampling points of the RXD signal using the QSPI\_RSD register.

Figure 96 Using QSPI to Collect RXD Signal Samples



## 23.4.6 QSPI interrupt

### qspi\_txe\_intr

This interrupt is set when the transmit FIFO is equal to or less than its threshold. The threshold that triggers the interrupt is determined by the programmable register QSPI\_RFTL. When data is written into the transmit FIFO buffer, the interrupt is cleared by hardware as the FIFO level exceeds the threshold.

### qspi\_txo\_intr

This interrupt is set when an AHB access attempts to write to a transmit FIFO that is completely full. Once set, data written from the AHB is ignored. The

interrupt remains set until the transmit FIFO overflow interrupt clear register (QSPI\_TFOIC) is read.

#### **qspi\_rxf\_intr**

This interrupt is set when the receive FIFO is equal to or greater than its threshold plus one. It is necessary to read the receive FIFO buffer within the interrupt to prevent overflow. The threshold that triggers the interrupt is determined by the programmable register QSPI\_RFTL. When data is read from the receive FIFO buffer, the interrupt is cleared by hardware as the FIFO level falls below the threshold.

#### **qspi\_rxo\_intr**

This interrupt is set when the receive logic attempts to place data into a receive FIFO that is already full. Once set, new received data is ignored. The interrupt remains set until the receive FIFO overflow interrupt clear register (QSPI\_RFOIC) is read.

#### **qspi\_rxu\_intr**

This interrupt is set when an AHB access attempts to read from an empty receive FIFO. Once set, reads from the receive FIFO return zero. The interrupt remains set until the receive FIFO underflow interrupt clear register (QSPI\_RFUIC) is read.

### **23.4.7 Enhanced SPI mode write operation**

QSPI write operations can be divided into three parts: instruction phase, address phase, and data phase.

The following register fields are used for a write operation:

- The FRF bit in QSPI\_CTRL1 specifies the format of the frame transmission.
- The INSLEN bit in QSPI\_CTRL3 specifies the length of the instruction.
- The ADDRLEN bit in QSPI\_CTRL3 specifies the address length.
- The DFS bit in QSPI\_CTRL1 specifies the data length.

A write transfer will only start when both the instruction and address have been written into the data register. To initiate a Quad write operation, the FRF bits in QSPI\_CTRL1 must be set to 10, which sets the transfer type. For each write instruction, data is transferred in the format specified by the FRF bits in QSPI\_CTRL1.

The following cases may occur for enhanced SPI mode write operations:

- Case A: Both instruction and address are transmitted in standard SPI format.

- Case B: Instruction is transmitted in standard SPI format, address in enhanced SPI format.
- Case C: Both instruction and address are transmitted in enhanced SPI format.

### Enhanced SPI Mode Read Operation

QSPI read operations can be divided into four phases: instruction phase, address phase, wait cycles, and data phase.

The wait cycles can be programmed via the WAITCYC field in QSPI\_CTRL3. The wait cycles are used to lock and switch the slave's mode from input to output, varying depending on the device. For a read operation, QSPI sends the instruction and control data at once, then waits to receive the number of data frames specified by the NDF field in QSPI\_CTRL2 before disabling the slave select signal. To initiate a Quad read operation, the FRF bits in QSPI\_CTRL1 are set to 00/01/10 respectively, which sets the transfer type. Each read instruction's data is transferred in the format specified by the FRF bits in QSPI\_CTRL1.

The following four cases may occur for enhanced SPI mode read operations:

- Case A: Both instruction and address are transmitted in standard SPI format.
- Case B: Instruction is transmitted in standard SPI format, address in enhanced SPI format.
- Case C: Both instruction and address are transmitted in enhanced SPI format.
- Case D: No instruction or address transmission during read.

### Clock Stretching Function

During data transfers between QSPI and an external SPI device, software might not guarantee timely transmission. This can cause underflow errors if the transmit FIFO is empty when QSPI attempts to send data because no valid data is available. On the receive side, overflow errors can happen if the receive FIFO is full and new incoming data cannot be properly received. To avoid such issues, software must abandon the current transfer and restart it.

To address this, QSPI provides a clock stretching function. If the transmit FIFO becomes empty before the end of a transmission, QSPI will halt the clock signal until enough data (above the transmit FIFO threshold TFTH) is available in the FIFO. Then QSPI resumes the clock and continues the transfer. If the receive FIFO is full before the end of a reception, QSPI stops the clock until data is read from the receive FIFO (below the receive FIFO threshold QSPI\_RFTL).

The clock stretching function can be enabled or disabled by setting bit 30 of the QSPI\_CTRL3 register. If enabled, the length of the data frame for the current

transfer must be written into the QSPI\_CTRL2 register.

### 23.4.8 DMA Function

The request/response DMA mechanism in QSPI facilitates high-speed data transfers and improves system efficiency.

By configuring the RDMAEN and TDMAEN bits in the QSPI\_DMACTRL register, the DMA function of QSPI can be enabled.

- During transmission: A DMA transmit data request is generated when the valid data level in the transmit FIFO level register QSPI\_TFL is equal to or below the value set by the DMATDL bit.
- During reception: A DMA receive data request is generated when the valid data level in the receive FIFO level register QSPI\_RFL is equal to or above the value set by the DMARDL bit.

### 23.4.9 XIP Function

#### 23.4.9.1 Overview of XIP mode

QSPI supports eXecute In Place (XIP) mode. In this mode, QSPI acts as a memory-mapped interface for SPI memory, allowing code to be executed directly from the SPI memory without first copying the code.

#### 23.4.9.2 XIP operation configuration process

XIP operations are supported only in dual- and quad-SPI modes. Typically, an XIP operation includes instruction phase, address phase, and data phase. Whether the instruction phase is included depends on the characteristics of the Flash memory.

When the Flash supports the instruction phase, the configuration process for XIP transfer is as follows:

- (1) Configure external access memory space and data endianness in the QSPI\_SWITCH register.
- (2) Set frame format value, transfer mode, and data frame size in the QSPI\_CTRL1 register.
- (3) Set clock division in the QSPI\_BR register.
- (4) In the QSPI\_CTRL3 register, configure address length, wait cycles, etc.
- (5) Write instruction opcodes in the XIP\_INCR\_INST and XIP\_WRAP\_INST registers.
- (6) Set XIP prefetch, transfer type, wait cycles, instruction length, instruction and address transfer types, and instruction enable in the XIP\_CTRL register.
- (7) Configure slave enable in the XIP\_SER register.

- (8) Enable XIP in the XIP\_EN register.

When the Flash does not support the instruction phase, the configuration process is as follows:

- (1) Configure external access memory space and data endianness in the QSPI\_SWITCH register.
- (2) Set frame format value, transfer mode, and data frame size in the QSPI\_CTRL1 register.
- (3) Set clock division in the QSPI\_BR register.
- (4) In the QSPI\_CTRL3 register, configure address length, wait cycles, etc.
- (5) Set XIP prefetch, transfer type, wait cycles, and address transfer type in the XIP\_CTRL register.
- (6) Configure slave enable in the XIP\_SER register.
- (7) Enable XIP in the XIP\_EN register.

Note: The maximum address length is 32 bits.

### 23.4.9.3 XIP and Non-XIP

XIP and non-XIP operations are mutually exclusive. When starting a new XIP or non-XIP transfer, two transfers must be arranged sequentially.

A non-XIP (read or write) transaction can be initiated during an ongoing XIP transfer. Only one transaction can be performed on the serial interface at a time. QSPI handles transactions based on a first-come, first-served principle. This means if a non-XIP transfer is already in progress on the SPI interface, the XIP transfer request will wait until the current transfer is completed, and vice versa.

Both XIP and non-XIP operations have their own dedicated registers for transfer configuration.

### 23.4.9.4 Continuous and non-continuous XIP transfers

QSPI supports both continuous and non-continuous transfer modes.

When XIP is in continuous transfer mode, the corresponding instructions (depending on Flash characteristics), address (the base address for continuous data transfer), and so on, need to be configured. After sending the instruction and address to the external Flash, QSPI continuously reads data starting from the base address. The instruction and address are sent only once; subsequent data transfers are incremented reads from the base address.

When XIP is in non-continuous transfer mode, each data read requires sending a full instruction (depending on Flash characteristics) and address, followed by the corresponding data read transfer.

Compared to continuous transfer, non-continuous XIP transfer adds a complete

instruction and address transmission for each read, increasing system latency.

Continuous XIP mode can be enabled by setting the CONT\_XFER\_EN bit in the XIP\_CTRL register to 1.

QSPI exits continuous mode under any of the following conditions:

- A non-XIP command is received on the XIP interface (effectively driving the xip\_en enable signal to 0).
- When the CPU points to a non-continuous address, the slave select is canceled, and QSPI initiates a new XIP request.

#### 23.4.9.5 Data Prefetch in XIP Operation

QSPI supports data prefetch in XIP mode, where the controller prefetches a continuous burst of data during the current XIP transaction. If the next transaction request is for a continuous address, data can be read directly from the RX FIFO without waiting to send new addresses and data to the device, improving overall system performance.

If a new XIP request arrives after the prefetch is complete, a new XIP operation starts, clearing the prefetched data from the previous request and beginning a new transfer and XIP prefetch.

If XIP continuous mode and prefetch are enabled, data is prefetched from the slave device, and the chip select pin remains active. During continuous requests, data is read from the RX FIFO, and QSPI will prefetch data for continuous addresses. This process continues until a non-continuous address is received or a non-XIP request is detected. In such cases, prefetched data is cleared from the FIFO, and a new transfer starts.

## 23.5 Register address mapping

Table 100 QSPI Register Address Mapping

| Register name | Description                            | Offset address |
|---------------|----------------------------------------|----------------|
| QSPI_CTRL1    | Control register 1                     | 0x0            |
| QSPI_CTRL2    | Control register 2                     | 0x4            |
| QSPI_SSIEN    | Enable register                        | 0x8            |
| QSPI_SLAEN    | Slave enable register                  | 0x10           |
| QSPI_BR       | Baud rate register                     | 0x14           |
| QSPI_TFTL     | Transmit FIFO threshold level register | 0x18           |
| QSPI_RFTL     | Receive FIFO threshold level register  | 0x1C           |
| QSPI_TFL      | Transmit FIFO level register           | 0x20           |

| Register name | Description                                     | Offset address |
|---------------|-------------------------------------------------|----------------|
| QSPI_RFL      | Receive FIFO level register                     | 0x24           |
| QSPI_STS      | Status register                                 | 0x28           |
| QSPI_INTEN    | Interrupt enable register                       | 0x2C           |
| QSPI_ISTS     | Interrupt status register                       | 0x30           |
| QSPI_RIS      | Raw interrupt status register                   | 0x34           |
| QSPI_TFOIC    | Transmit FIFO overflow interrupt clear register | 0x38           |
| QSPI_RFOIC    | Receive FIFO overflow interrupt clear register  | 0x3C           |
| QSPI_RFUIC    | Receive FIFO underflow interrupt clear register | 0x40           |
| QSPI_ICF      | Interrupt clear register                        | 0x48           |
| QSPI_DMACTRL  | DMA control register                            | 0x4C           |
| QSPI_DMATDL   | DMA transmit data level register                | 0x50           |
| QSPI_DMARDL   | DMA receive data level register                 | 0x54           |
| QSPI_DATA     | Data register                                   | 0x60           |
| QSPI_RSD      | RX sample delay register                        | 0xF0           |
| QSPI_CTRL3    | Control register 3                              | 0xF4           |
| XIP_INCR_INST | XIP INCR transfer opcode register               | 0x100          |
| XIP_WRAP_INST | XIP WRAP transfer opcode register               | 0x104          |
| XIP_CTRL      | XIP control register                            | 0x108          |
| XIP_SER       | Slave enable register                           | 0x10C          |
| QSPI_SWITCH   | QSPI switch register                            | 0x200          |
| XIP_EN        | XIP enable register                             | 0x204          |

## 23.6 Register functional description

### 23.6.1 Control register1 (QSPI\_CTRL1)

Offset address: 0x00

Reset value: 0x0000 4007

This register controls the transmission of serial data. When QSPI is enabled, this register cannot be written. QSPI is started or disabled by writing to the QSPI\_CTRL2 register.



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | DFS      | RW  | <p>Data Frame Size</p> <p>Select the data frame length. When the data frame size is programmed to be less than 32 bits, the received data is automatically right-aligned by the reception logic and zero-padded at the high bits in the receive FIFO. Right adjustment of the transmission data must be performed before writing to the transmission FIFO. The transmission logic ignores the unused high bits when transmitting data.</p> <p>If SPI_FRF =01, then the DFS value must be a multiple of 2.</p> <p>If SPI_FRF =10, then the DFS value must be a multiple of 4.</p> <p>0x0 (DFS_01_BIT): Reserved</p> <p>0x1 (DFS_02_BIT): Reserved</p> <p>0x2 (DFS_03_BIT): Reserved</p> <p>0x3 (DFS_04_BIT): 04-bit serial data transfer</p> <p>0x4 (DFS_05_BIT): 05-bit serial data transfer</p> <p>0x5 (DFS_06_BIT): 06-bit serial data transfer</p> <p>0x6 (DFS_07_BIT): 07-bit serial data transfer</p> <p>0x7 (DFS_08_BIT): 08-bit serial data transfer</p> <p>0x8 (DFS_09_BIT): 09-bit serial data transfer</p> <p>0x9 (DFS_10_BIT): 10-bit serial data transfer</p> <p>0xA (DFS_11_BIT): 11-bit serial data transfer</p> <p>0xB (DFS_12_BIT): 12-bit serial data transfer</p> <p>0xC (DFS_13_BIT): 13-bit serial data transfer</p> <p>0xD (DFS_14_BIT): 14-bit serial data transfer</p> <p>0xE (DFS_15_BIT): 15-bit serial data transfer</p> <p>0xF (DFS_16_BIT): 16-bit serial data transfer</p> <p>0x10 (DFS_17_BIT): 17-bit serial data transfer</p> <p>0x11 (DFS_18_BIT): 18-bit serial data transfer</p> <p>0x12 (DFS_19_BIT): 19-bit serial data transfer</p> <p>0x13 (DFS_20_BIT): 20-bit serial data transfer</p> <p>0x14 (DFS_21_BIT): 21-bit serial data transfer</p> <p>0x15 (DFS_22_BIT): 22-bit serial data transfer</p> <p>0x16 (DFS_23_BIT): 23-bit serial data transfer</p> <p>0x17 (DFS_24_BIT): 24-bit serial data transfer</p> <p>0x18 (DFS_25_BIT): 25-bit serial data transfer</p> <p>0x19 (DFS_26_BIT): 26-bit serial data transfer</p> <p>0x1A (DFS_27_BIT): 27-bit serial data transfer</p> <p>0x1B (DFS_28_BIT): 28-bit serial data transfer</p> <p>0x1C (DFS_29_BIT): 29-bit serial data transfer</p> <p>0x1D (DFS_30_BIT): 30-bit serial data transfer</p> <p>0x1E (DFS_31_BIT): 31-bit serial data transfer</p> <p>0x1F (DFS_32_BIT): 32-bit serial data transfer</p> |
| 9:5   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | TXMODE   | R/W | <p>Transfer Mode</p> <p>Select the transmission mode for serial communication. This field does not affect the repetition of transmission. It only indicates whether the received or transmitted data is valid.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | <p>In transmit-only mode, data received from external devices is invalid and is not stored in the receive FIFO memory.</p> <p>In receive-only mode, transmitted data is invalid. After the first write to the transmit FIFO, the same data word is retransmitted during the transfer.</p> <p>In both transmit and receive mode, both transmitted and received data are valid. Data received from external devices is stored in the receive FIFO memory.</p> <p>0x0 (TX_AND_RX): Transmit and receive, not applicable to enhanced SPI operation mode</p> <p>0x1 (TX_ONLY): Transmit-only mode, or writing in enhanced SPI operation mode</p> <p>0x2 (RX_ONLY): Receive-only mode, or reading in enhanced SPI operation mode</p> <p>0x3 (EEPROM_READ): EEPROM read mode, not applicable to enhanced SPI operation mode</p> |
| 13:12 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 14    | SSTEN    | R/W | <p>Chip Select Reversal Enable</p> <p>When operating in standard SPI mode with clock phase (SCPH) set to 0, this register controls the chip select signal line between data frames.</p> <p>0: The chip select signal line does not invert between consecutive frames.</p> <p>1: The chip select signal line will invert between consecutive frames; when the chip select line is high, the CLK signal will be at its default level.</p>                                                                                                                                                                                                                                                                                                                                                                                  |
| 21:15 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 23:22 | FRF      | R/W | <p>Frame Format</p> <p>Select the data frame format for sending/receiving data.</p> <p>00 (SPI_STANDARD): Standard SPI mode</p> <p>01 (SPI_DUAL): Dual SPI mode</p> <p>10 (SPI_QUAD): Quad SPI mode</p> <p>11: Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 31:24 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### 23.6.2 Control register2 (QSPI\_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | NDF      | R/W | <p>Data Frame Number</p> <p>When TXMODE=10 or TXMODE=11, this register field sets the number of data frames for QSPI continuous reception. QSPI continues to receive serial data until the number of received data frames equals the value of this register plus one, allowing a maximum of 64KB of data to be received in continuous transfer.</p> |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                     |

### 23.6.3 Enable register (QSPI\_SSIEN)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                        |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | EN       | R/W | QSPI Enable<br>Enable or disable all QSPI operations. When disabled, all serial transmissions are halted immediately. When the device is disabled, the transmit and receive FIFO buffers are cleared. When enabled, programming of certain QSPI control registers is not possible. |
| 31:1  | Reserved |     |                                                                                                                                                                                                                                                                                    |

### 23.6.4 Slave enable register (QSPI\_SLAEN)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                               |
|-------|----------|-----|-------------------------------------------|
| 0     | SLAEN    | R/W | Slave Enable<br>0: Disabled<br>1: Enabled |
| 31:1  | Reserved |     |                                           |

### 23.6.5 Baud rate register (QSPI\_BR)

Offset address: 0x14

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | CLKDIV   | R/W | Clock Divider<br>The LSB of this field is always set to 0 and is unaffected by write operations, ensuring that an even number is stored in this register. If this value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out output is determined by the following equation:<br>$F_{sclk\_out} = F_{qspi\_clk} / SCKDIV$<br>SCKDIV can be any even number between 2 and 65534.<br>For example:<br>When $F_{qspi\_clk} = 3.6864\text{MHz}$ and $SCKDIV = 2$ , then<br>$F_{sclk\_out} = 3.6864 / 2 = 1.8432\text{MHz}$ |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

### 23.6.6 Transmit FIFO threshold level register (QSPI\_TFTL)

Offset address: 0x18

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | TFT      | R/W | <p>Transmit FIFO Threshold</p> <p>Controls the trigger level (or lower) for interrupt generation by the transmit FIFO controller.</p> <p>The FIFO depth can be set within the range of 8 to 256, and the size of this register corresponds to the number of address bits required to access the FIFO.</p> <p>If an attempt is made to set this value to a number greater than or equal to the FIFO depth, this field will not be written and will remain at its current value.</p> <p>An interrupt is triggered when the number of entries in the transmit FIFO is less than or equal to this value.</p> |
| 15:3  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 18:16 | TFTH     | R/W | <p>Transfer Start FIFO Level</p> <p>Used to control the entry level of the transmit FIFO, at which transmission will begin on the serial line. This register can be used to ensure that there is sufficient data in the transmit FIFO before starting a write operation on the serial line. These fields are only valid in master operation mode.</p>                                                                                                                                                                                                                                                    |
| 31:19 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### 23.6.7 Receive FIFO threshold level register (QSPI\_RFTL)

Offset address: 0x1C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | RFT      | R/W | <p>Receive FIFO Threshold</p> <p>Controls the trigger level (or higher) for interrupt generation by the receive FIFO controller.</p> <p>The FIFO depth can be set within the range of 8 to 256, and the size of this register corresponds to the number of address bits required to access the FIFO.</p> <p>If an attempt is made to set this value to a number greater than the FIFO depth, this field will not be written and will remain at its current value.</p> <p>An interrupt is triggered when the number of entries in the receive FIFO is greater than or equal to this value plus one.</p> |
| 31:3  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 23.6.8 Transmit FIFO level register (QSPI\_TFL)

Offset address: 0x20

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                       |
|-------|----------|-----|---------------------------------------------------------------------------------------------------|
| 3:0   | TFL      | R   | <p>Transmit FIFO Level</p> <p>Contains the number of valid data entries in the transmit FIFO.</p> |
| 31:4  | Reserved |     |                                                                                                   |

### 23.6.9 Receive FIFO level register (QSPI\_RFL)

Offset address: 0x24

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                          |
|-------|----------|-----|--------------------------------------------------------------------------------------|
| 3:0   | RFL      | R   | Receive FIFO Level<br>Contains the number of valid data entries in the receive FIFO. |
| 31:4  | Reserved |     |                                                                                      |

### 23.6.10 Status register (QSPI\_STS)

Offset address: 0x28

Reset value: 0x0000 0006

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                  |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | BUSYF    | R   | SSI Busy Flag<br>When set, indicates that serial transfer is in progress; when cleared, indicates that QSPI is idle or disabled.<br>1: QSPI is actively transmitting data<br>0: QSPI is in idle or disabled state                                                            |
| 1     | TFNF     | R   | Transmit FIFO Not Full Flag<br>The bit is set when the transmit FIFO contains one or more empty bits. It is cleared when the FIFO is full.<br>1: Transmit FIFO is not full<br>0: Transmit FIFO is full                                                                       |
| 2     | TFEF     | R   | Transmit FIFO Empty Flag<br>The bit is set when the transmit FIFO is completely empty. It is cleared when the transmit FIFO contains one or more valid entries. This bit field does not generate an interrupt.<br>1: Transmit FIFO is empty<br>0: Transmit FIFO is not empty |
| 3     | RFNEF    | R   | Receive FIFO Not Empty Flag<br>The bit is set when the receive FIFO contains one or more entries. It is cleared when the receive FIFO is empty. Software can poll this bit to fully clear the receive FIFO.<br>1: Receive FIFO is not empty<br>0: Receive FIFO is empty      |
| 4     | RFFF     | R   | Receive FIFO Full Flag<br>The bit is set when the receive FIFO is completely full. It is cleared when the receive FIFO contains one or more empty bits.<br>1: Receive FIFO is full<br>0: Receive FIFO is not full                                                            |
| 31:5  | Reserved |     |                                                                                                                                                                                                                                                                              |

### 23.6.11 Interrupt enable register (QSPI\_INTEN)

Offset address: 0x2C

Reset value: 0x0000 007F

| Field | Name     | R/W | Description                                                                                                          |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------|
| 0     | TFEIE    | R/W | Transmit FIFO Interrupt Enable<br>0: qspi_txe_intr interrupt is masked<br>1: qspi_txe_intr interrupt enable          |
| 1     | TFOIE    | R/W | Transmit FIFO Overflow Interrupt Enable<br>0: qspi_txo_intr interrupt is masked<br>1: qspi_txo_intr interrupt enable |
| 2     | RFUIE    | R/W | Receive FIFO Underflow Interrupt Enable<br>0: qspi_rxu_intr interrupt is masked<br>1: qspi_rxu_intr interrupt enable |
| 3     | RFOIE    | R/W | Receive FIFO Overflow Interrupt Enable<br>0: qspi_rxo_intr interrupt is masked<br>1: qspi_rxo_intr interrupt enable  |
| 4     | RFFIE    | R/W | Receive FIFO Full Interrupt Enable<br>0: qspi_rxf_intr interrupt is masked<br>1: qspi_rxf_intr interrupt enable      |
| 31:5  | Reserved |     |                                                                                                                      |

### 23.6.12 Interrupt status register (QSPI\_ISTS)

Offset address: 0x30

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                 |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TFEIF    | R   | Transmit FIFO Empty Interrupt Status<br>0: When qspi_txe_intr is masked, the interrupt is not activated.<br>1: When qspi_txe_intr is masked, the interrupt is activated.    |
| 1     | TFOIF    | R   | Transmit FIFO Overflow Interrupt Status<br>0: When qspi_txo_intr is masked, the interrupt is not activated.<br>1: When qspi_txo_intr is masked, the interrupt is activated. |
| 2     | RFUIF    | R   | Receive FIFO Underflow Interrupt Status<br>0: qspi_rxu_intr is masked, the interrupt is not activated.<br>1: qspi_rxu_intr is masked, the interrupt is activated.           |
| 3     | RFOIF    | R   | Receive FIFO Overflow Interrupt Status<br>0: qspi_rxo_intr is masked, the interrupt is not activated.<br>1: qspi_rxo_intr is masked, the interrupt is activated.            |
| 4     | RFFIF    | R   | Receive FIFO Full Interrupt Status<br>0: qspi_rxf_intr is masked, the interrupt is not activated.<br>1: qspi_rxf_intr is masked, the interrupt is activated.                |
| 31:5  | Reserved |     |                                                                                                                                                                             |

### 23.6.13 Raw interrupt status register (QSPI\_RIS)

Offset address: 0x34

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                       |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TFEIF    | R   | Transmit FIFO Empty Raw Interrupt Status<br>0: qspi_txe_intr is not activated before masking.<br>1: qspi_txe_intr is activated before masking.    |
| 1     | TFOIF    | R   | Transmit FIFO Overflow Raw Interrupt Status<br>0: qspi_txo_intr is not activated before masking.<br>1: qspi_txo_intr is activated before masking. |
| 2     | RFUIF    | R   | Receive FIFO Underflow Raw Interrupt Status<br>0: qspi_rxu_intr is not activated before masking.<br>1: qspi_rxu_intr is activated before masking. |
| 3     | RXOIR    | R   | Receive FIFO Overflow Raw Interrupt Status<br>0: qspi_rxo_intr is not activated before masking.<br>1: qspi_rxo_intr is activated before masking.  |
| 4     | RXFIR    | R   | Receive FIFO Full Raw Interrupt Status<br>0: qspi_rxf_intr is not activated after masking.<br>1: qspi_rxf_intr is activated after masking.        |
| 31:5  | Reserved |     |                                                                                                                                                   |

#### 23.6.14 Transmit FIFO overflow interrupt clear register (QSPI\_TFOIC)

Offset address: 0x38

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TFOIC    | R   | Transmit FIFO Overflow Interrupt Clear<br>Reflects the interrupt status.<br>Reading from this register clears the qspi_txo_intr interrupt; writing has no effect. |
| 31:1  | Reserved |     |                                                                                                                                                                   |

#### 23.6.15 Receive FIFO overflow interrupt clear register (QSPI\_RFOIC)

Offset address: 0x3C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                      |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | RFOIC    | R   | Receive FIFO Overflow Interrupt Clear<br>Reflects the interrupt status.<br>Reading from this register clears the qspi_rxo_intr interrupt; writing has no effect. |
| 31:1  | Reserved |     |                                                                                                                                                                  |

#### 23.6.16 Receive FIFO underflow interrupt clear register (QSPI\_RFUIC)

Offset address: 0x40

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | RFUIC    | R   | Receive FIFO Underflow Interrupt Clear<br>Reflects the interrupt status.<br>Reading from this register clears the qspi_rxu_intr interrupt; writing has no effect. |
| 31:1  | Reserved |     |                                                                                                                                                                   |

### 23.6.17 Interrupt clear register (QSPI\_ICF)

Offset address: 0x48

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                       |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ICF      | R   | Interrupt Clear<br>If any of the following interrupts are active, the set bit in this register will be set.<br>Reading this register clears the qspi_txo_intr, qspi_rxu_intr, qspi_rxo_intr, and qspi_mst_intr interrupts; writing has no effect. |
| 31:1  | Reserved |     |                                                                                                                                                                                                                                                   |

### 23.6.18 DMA control register (QSPI\_DMACTRL)

Offset address: 0x4C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                      |
|-------|----------|-----|--------------------------------------------------|
| 0     | RDMAEN   | R/W | Receive DMA Enable<br>0: Disabled<br>1: Enabled  |
| 1     | TDMAEN   | R/W | Transmit DMA Enable<br>0: Disabled<br>1: Enabled |
| 31:2  | Reserved |     |                                                  |

### 23.6.19 DMA transmit data level register (QSPI\_DMATDL)

Offset address: 0x50

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | DMATDL   | R/W | Data Level Transmit<br>When the valid data in the transmit FIFO is equal to or less than the DMATDL configuration value, a DMA transmit data request is generated, effective when TDMAEN=1.<br>The configuration range is from 0 to 7. |
| 31:3  | Reserved |     |                                                                                                                                                                                                                                        |

### 23.6.20 DMA receive data level register (QSPI\_DMARDL)

Offset address: 0x54

Reset value: 0x0000 0000



| Field | Name     | R/W | Description                                                                                                                                                                                                                                               |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | DMARDL   | R/W | Data Level Receive<br>When the valid data in the receive FIFO is equal to or greater than the DMATDL configuration value + 1, a DMA receive data request is generated. When RDMAEN=1, dma_rx_req is generated.<br>The configuration range is from 0 to 7. |
| 31:3  | Reserved |     |                                                                                                                                                                                                                                                           |

### 23.6.21 Data register (QSPI\_DATA)

Offset address: 0x60

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                        |
|-------|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | DATA | R/W | Data<br>When writing to this register, data must be right-aligned; reading data will be automatically right-aligned.<br>Read = Receive FIFO buffer<br>Write = Transmit FIFO buffer |

### 23.6.22 RX sample delay register (QSPI\_RSD)

Offset address: 0xF0

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                               |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | RSD      | R/W | Receive Data (RXD) Sampling Delay<br>Used to delay the sampling of the RXD input port.<br>Each value represents a single qspi_clk delay on the RXD sample.                                                                                                |
| 15:8  | Reserved |     |                                                                                                                                                                                                                                                           |
| 16    | RSE      | R/W | Receive Data (RXD) Sampling Edge<br>Used to determine the sampling edge of the RXD signal with qspi_clk.<br>Set this bit to 1, and then the input data will be sampled on the falling edge of qspi_clk; otherwise, it will be sampled on the rising edge. |
| 31:17 | Reserved |     |                                                                                                                                                                                                                                                           |

### 23.6.23 Control register3 (QSPI\_CTRL3)

Offset address: 0xF4

Reset value: 0x0000 0200

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | IAT        | R/W | <p>Transmit Format Address and Instruction</p> <p>Determines whether QSPI transmits commands/addresses in standard SPI mode or in the SPI mode selected by the CTRL0[SPI_FRF] field.</p> <p>00 (TT0): Send commands and addresses in standard SPI mode</p> <p>01 (TT1): Send commands in standard SPI mode and addresses under the mode specified by QSPI_CTRL1[SPI_FRF]</p> <p>10 (TT2): Send commands and addresses under the mode specified by SPI_FRF</p> <p>11 (TT3): Reserved</p>                                                                                                                                                                                                                                                                                                                                                               |
| 5:2   | ADDRLEN    | R/W | <p>Transmitted Address Length</p> <p>Transfer can only begin after these bits have been programmed into the FIFO.</p> <p>0x0 (ADDR_L0): No address</p> <p>0x1 (ADDR_L4): 4-bit address length</p> <p>0x2 (ADDR_L8): 8-bit address length</p> <p>0x3 (ADDR_L12): 12-bit address length</p> <p>0x4 (ADDR_L16): 16-bit address length</p> <p>0x5 (ADDR_L20): 20-bit address length</p> <p>0x6 (ADDR_L24): 24-bit address length</p> <p>0x7 (ADDR_L28): 28-bit address length</p> <p>0x8 (ADDR_L32): 32-bit address length</p> <p>0x9 (ADDR_L36): 36-bit address length</p> <p>0xA (ADDR_L40): 40-bit address length</p> <p>0xB (ADDR_L44): 44-bit address length</p> <p>0xC (ADDR_L48): 48-bit address length</p> <p>0xD (ADDR_L52): 52-bit address length</p> <p>0xE (ADDR_L56): 56-bit address length</p> <p>0xF (ADDR_L60): 60-bit address length</p> |
| 7:6   | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 9:8   | INSLEN     | R/W | <p>Instruction Length in Four-wire Mode</p> <p>00 (INST_L0): No instruction</p> <p>01 (INST_L4): 4-bit instruction</p> <p>10 (INST_L8): 8-bit instruction</p> <p>11 (INST_L16): 16-bit instruction</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 10    | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15:11 | WAITCYC    | R/W | <p>Wait Cycles</p> <p>In four-wire mode, the number of clock cycles that need to wait before sending/receiving data.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 18:16 | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 19    | XIP_DFS_HC | R   | <p>XIP Transmit Data Frame Size</p> <p>0: invalid</p> <p>1: The size of the XIP data transfer frame is fixed to the value programmed in QSPI_CTRL1[DFS].</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

| Field | Name                  | R/W | Description                                                                                                                                                                                                                                                                                       |
|-------|-----------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20    | XIP_INST_EN           | R   | XIP Instruction Enable<br>0: XIP transfer does not have an instruction phase<br>1: XIP transfer will have an instruction phase                                                                                                                                                                    |
| 21    | SSIC_XIP_CONT_XFER_EN | R   | Enable Continuous Transmission in XIP Mode<br>0: Continuous transfer mode in XIP is disabled<br>1: Continuous transfer mode in XIP is enabled; QSPI will remain in the selected device state until a non-XIP transfer is detected                                                                 |
| 28:22 | Reserved              |     |                                                                                                                                                                                                                                                                                                   |
| 29    | XIP_PREFETCH_EN       | R   | Enable Prefetch Function in XIP Mode<br>0: Pre-fetch feature in XIP transfer is disabled<br>1: Pre-fetch feature in XIP transfer is enabled. QSPI will prefetch data frames from the next consecutive position. If the next XIP request is not continuous, the prefetched data will be discarded. |
| 30    | CSEN                  | R/W | Clock Stretch Enable<br>SPI transfer capability. If writing, the FIFO becomes empty, and QSPI will extend the clock until there is enough data in the FIFO to continue transmission. If reading, the receive FIFO becomes full, and QSPI will stop the clock until data is read from the FIFO.    |
| 31    | Reserved              |     |                                                                                                                                                                                                                                                                                                   |

#### 23.6.24 XIP INCR transfer opcode register (XIP\_INCR\_INST)

Offset address: 0x100

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                               |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | INCR_INST | R/W | XIP INCR Transfer Operation Code<br>When XIP_CTRL[XIP_INST_EN] is set to 1, QSPI sends the instruction opcode for all XIP request INCR type transfers. The instruction length is determined by the XIP_CTRL[INST_L] bits. |
| 31:16 | Reserved  |     |                                                                                                                                                                                                                           |

#### 23.6.25 XIP WRAP transfer opcode register (XIP\_WRAP\_INST)

Offset address: 0x104

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                               |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | WRAP_INST | R/W | XIP WRAP Transfer Operation Code<br>When XIP_CTRL[XIP_INST_EN] is set to 1, QSPI sends the instruction opcode for all XIP request WRAP type transfers. The instruction length is determined by the XIP_CTRL[INST_L] bits. |
| 31:16 | Reserved  |     |                                                                                                                                                                                                                           |

### 23.6.26 XIP control register (XIP\_CTRL)

Offset address: 0x108

Reset value: 0x0800 0401

| Field | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | FRF            | R/W | <p>Frame Format</p> <p>Select the data frame format for transmitting/receiving data.</p> <p>0x0 (RSVD): Reserved</p> <p>0x1 (SPI_DUAL): Dual SPI mode</p> <p>0x2 (SPI_QUAD): Quad SPI mode</p> <p>0x3: Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 3:2   | TRANS_TY<br>PE | R/W | <p>Transmission Format of Address and Instruction</p> <p>Select whether QSPI transmits instructions/addresses in standard SPI mode or in the SPI mode specified by the QSPI_CTRL1[FRF] field.</p> <p>0x0 (TT0): Instructions and addresses will be sent in standard SPI mode.</p> <p>0x1 (TT1): Instructions will be sent in standard SPI mode, and addresses will be sent in the mode specified by XIP_CTRL[FRF].</p> <p>0x2 (TT2): Instructions and addresses will be sent in the mode specified by XIP_CTRL[FRF].</p> <p>0x3 (TT3): Reserved.</p>                                                                                                                                                                                                  |
| 7:4   | ADDR_L         | R/W | <p>Address Length</p> <p>0x0 (ADDR_L0): No address</p> <p>0x1 (ADDR_L4): 4-bit address length</p> <p>0x2 (ADDR_L8): 8-bit address length</p> <p>0x3 (ADDR_L12): 12-bit address length</p> <p>0x4 (ADDR_L16): 16-bit address length</p> <p>0x5 (ADDR_L20): 20-bit address length</p> <p>0x6 (ADDR_L24): 24-bit address length</p> <p>0x7 (ADDR_L28): 28-bit address length</p> <p>0x8 (ADDR_L32): 32-bit address length</p> <p>0x9 (ADDR_L36): 36-bit address length</p> <p>0xA (ADDR_L40): 40-bit address length</p> <p>0xB (ADDR_L44): 44-bit address length</p> <p>0xC (ADDR_L48): 48-bit address length</p> <p>0xD (ADDR_L52): 52-bit address length</p> <p>0xE (ADDR_L56): 56-bit address length</p> <p>0xF (ADDR_L60): 60-bit address length</p> |
| 8     | Reserved       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 10:9  | INST_L         | R/W | <p>Instruction Length in Dual/Four-wire Mode</p> <p>0x0 (INST_L0): No instruction</p> <p>0x1 (INST_L4): 4-bit instruction length</p> <p>0x2 (INST_L8): 8-bit instruction length</p> <p>0x3 (INST_L16): 16-bit instruction length</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 12:11 | Reserved       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

| Field | Name            | R/W | Description                                                                                                                                                                                                                                                                                      |
|-------|-----------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17:13 | WAIT_CYCLES     | R/W | Wait Cycles<br>In dual/four-wire XIP transfer mode, the number of clock cycles to wait before sending/receiving data.                                                                                                                                                                            |
| 18    | DFS_HC          | R/W | XIP Transmission Data Frame Size<br>0: Invalid<br>1: The size of the XIP transfer data frame is fixed to the value programmed in QSPI_CTRL1[DFS].<br>Note: When configuring XIP transfer, this bit is set to 1 by default.                                                                       |
| 21:19 | Reserved        |     |                                                                                                                                                                                                                                                                                                  |
| 22    | INST_EN         | R/W | XIP Instruction Enable<br>0: XIP transfer does not include an instruction phase.<br>1: XIP transfer will include an instruction phase.                                                                                                                                                           |
| 23    | CONT_XFER_EN    | R/W | Enable XIP Mode Continuous Transmission<br>0: Continuous transfer mode in XIP is not enabled.<br>1: Continuous transfer mode in XIP is enabled, and QSPI will keep the slave device selected until a non-XIP transfer is detected.                                                               |
| 28:24 | Reserved        |     |                                                                                                                                                                                                                                                                                                  |
| 29    | XIP_PREFETCH_EN | R/W | Enable Prefetch in XIP Mode<br>0: Prefetch function in XIP transfer is not enabled.<br>1: Prefetch function in XIP transfer is enabled, and QSPI will prefetch data frames from the next consecutive location. If the next XIP request is not continuous, the prefetched data will be discarded. |
| 31:30 | Reserved        |     |                                                                                                                                                                                                                                                                                                  |

### 23.6.27 Slave enable register (XIP\_SER)

Offset address: 0x10C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                |
|-------|----------|-----|------------------------------------------------------------|
| 0     | SER      | R/W | Slave Select Enable Flag<br>0: Not selected<br>1: Selected |
| 31:1  | Reserved |     |                                                            |

### 23.6.28 QSPI switch register (QSPI\_SWITCH)

Offset address: 0x200

Reset value: 0x0000 0000

| Field | Name   | R/W | Description                                                                                                                                |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | SWITCH | R/W | Switch PC CARD/QSPI to Access External Memory Space<br>0: PC CARD can access 0x90000000~9FFFFFFF<br>1: QSPI can access 0x90000000~9FFFFFFF |

| Field | Name             | R/W | Description                                                  |
|-------|------------------|-----|--------------------------------------------------------------|
| 1     | LITTLE<br>ENDIAN | R/W | Little Endian<br>0: Big-endian read<br>1: Little-endian read |
| 31:2  | Reserved         |     |                                                              |

### 23.6.29 XIP enable register (XIP\_EN)

Offset address: 0x204

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------|
| 0     | XIP_EN   | R/W | XIP Enable<br>0: XIP transfer mode is not enabled.<br>1: XIP transfer mode is enabled. |
| 31:1  | Reserved |     |                                                                                        |

## 24 Controller Area Network (CAN)

### 24.1 Full name and abbreviation description of terms

Table 101 Full name and abbreviation description of terms

| Full name in English     | English abbreviation |
|--------------------------|----------------------|
| First Input First Output | FIFO                 |
| Request                  | REQ                  |

### 24.2 Introduction

CAN is abbreviation of Controller Area Network, and is serial communication protocol of ISO international standardization and supports CAN Protocol 2.0A and 2.0B. In CAN protocol, the transmitter transmits the message to all receivers in the form of broadcast. When the node receives the message, it will go through the filter group and decide whether the message is needed according to the identifier. This design saves the CPU resource.

### 24.3 Main characteristics

- (1) Support CAN protocol 2.0A and 2.0B
- (2) The maximum baud rate of communication is 1Mbit/s
- (3) Transmission function
  - There are three transmitting mailboxes
  - The priority of transmitting message can be configured
  - Record the transmission time
- (4) Receiving function
  - Have two receive FIFO with three depth levels
  - Have 28 filter groups
  - Record the receiving time

### 24.4 Functional description

#### 24.4.1 Characteristics of CAN physical layer

There can be multiple communication nodes on the CAN bus, each node consists of a CAN controller and a transceiver. The controller and transceiver are connected through CAN\_TX and CAN\_RX to transmit logic signals; the transceiver and bus are connected through CAN\_High and CAN\_Low to transmit differential signals.

## 24.4.2 Message structure

Figure 97 Standard Data Frame

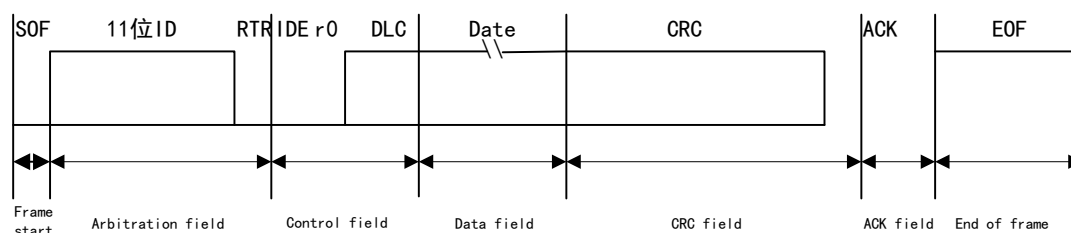
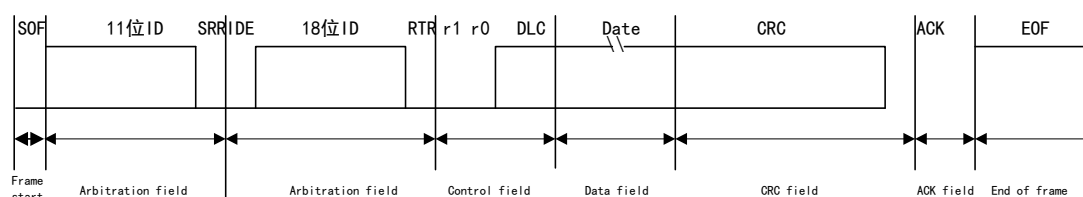


Figure 98 Extended Data Frame



Note:

- (1) Frame start: used to inform each node that there will be data for transmission.
- (2) Arbitration segment: It is used to decide which message can be transmitted when multiple messages are transmitted. Main content of this segment is ID information, the ID in standard format is 11 bits, and the ID in extended format is 29 bits.
- (3) Control segment: The main content of this segment is data length code (DLC), which is used to indicate how many bytes the data segment has in the message. The data segment has up to 8 bytes.
- (4) Data segment: Include the data information to be sent by the node.
- (5) CRC segment: CRC check code is used to ensure correct transmission of the messages.
- (6) ACK segment: This segment includes ACK slot bit and ACK delimiter bit. The transmitting node in ACK slot transmits recessive bits, while the receiving node transmits the dominant bit in this bit to acknowledge.
- (7) Frame end: Seven recessive bits sent by the transmitting nodes are used to indicate the end.

## 24.4.3 Working Mode

CAN has three main working modes: initialization mode, normal mode and sleep mode.

### 24.4.3.1 Initialization mode

Set the INITREQ bit of the configuration register CAN\_MCTRL to 1 to request to enter the initialization mode; clear the INITFLG bit to confirm entering the initialization mode.

Clear the INITREQ bit of the configuration register CAN\_MCTRL to request to exit the initialization mode; clear the INITFLG bit to confirm exiting the



initialization mode.

Message receiving and transmitting is disabled in initialization mode.

#### 24.4.3.2 Normal mode

Clear the INITREQ bit of the configuration register CAN\_MCTRL through software to request to enter the normal mode from the initialization mode; wait for the hardware to clear the INITFLG bit to enter the normal mode.

Message receiving and transmitting is allowed in normal mode.

#### 24.4.3.3 Sleep mode

Set the SLEEPREQ bit of the configuration register CAN\_MCTRL to 1 to request to enter the sleep mode.

The clock of CAN stops work in sleep mode, the software can normally access the mailbox register, and the CAN is in low-power state.

### 24.4.4 Communication mode

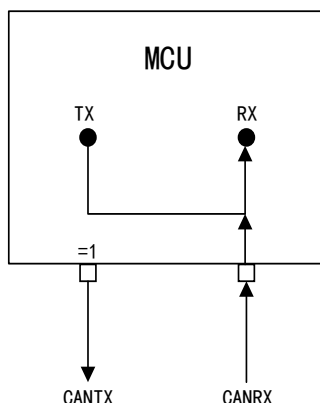
There are four communication modes: silent mode, loopback mode, silent loopback mode and normal mode. Different communication modes can be selected only in initialization mode.

#### 24.4.4.1 Silent mode

Set the SILMEN bit of the configuration register CAN\_BITTIM to 1 and select the silent mode.

In this mode, only recessive bit (logic 1) can be sent to the bus, while the dominant bit (logic 0) cannot be sent, and the data can be received from the bus.

Figure 99 CAN Works in Silent Mode

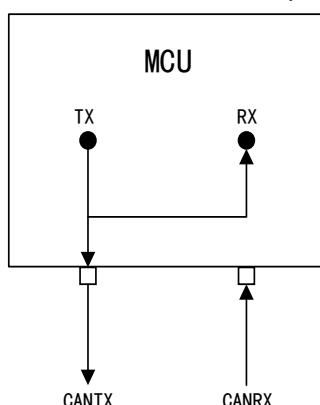


#### 24.4.4.2 Loopback mode

Set the LBKMEN bit of the configuration register CAN\_BITTIM to 1 and select the loopback mode.

In this mode, the sent data are directly transmitted to the input end for receiving, the data are not received from the bus, and all data can be sent to the bus.

Figure 100 CAN Works in Loopback Mode

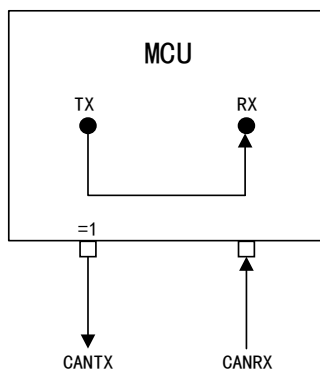


#### 24.4.4.3 Loopback silent mode

Set the LBKMEN and SILMEN bits of the configuration register CAN\_BITTIM to 1 and select the loopback silent mode.

In this mode, the sent data are directly transmitted to the input end for receiving, and the data are not received from the bus; only recessive bit (logic 1) can be sent to the bus, while the dominant bit (logic 0) cannot be sent.

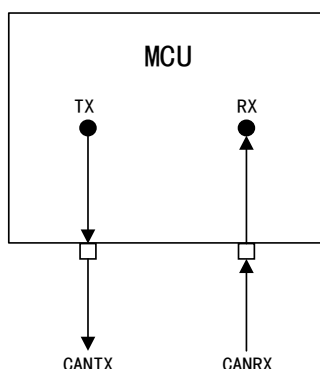
Figure 101 CAN Works in Silent Loopback Mode



#### 24.4.4.4 Normal mode

In this mode, data can be sent to the bus and be received from the bus.

Figure 102 CAN Works in Normal Mode



## 24.4.5 Data transmission

### 24.4.5.1 Conversion of transmitting mailbox state

Conversion process of transmitting mailbox state:

- (1) First select an empty mailbox to set, submit the transmitting request to the CAN bus controller by setting the TXMREQ bit of the configuration register CAN\_TXMIDx to 1, and then the mailbox immediately enters the registration state.
- (2) When multiple mailboxes are in the registered state, conduct priority scheduling. When a mailbox has the highest priority, it will enter the predetermined state.
- (3) When the message in the transmitting mailbox is sent to the bus, it will enter the transmitting state.
- (4) After the message is sent successfully, the mailbox will become idle again.

### 24.4.5.2 Transmitting priority

When multiple messages are waiting for transmitting, determine the transmitting sequence through the TXFPCFG bit of the configuration register CAN\_MCTRL:

- When the TXFPCFG bit is set to 0, the priority is determined by the message identifier, the identifier is the lowest, the priority is the highest, the identifier is equal, and the message with small mailbox number will be sent first
- When the TXFPCFG bit is set to 1, the priority will be determined by the sequence of transmitting request

### 24.4.5.3 Abort

Transmit the abort request by setting the ABREQFLG bit of the configuration register CAN\_TXSTS to 1.

If the mailbox is in registered or predetermined state, stop transmitting the request immediately; if the mailbox is in the transmitting state, there are two conditions: one is that the mailbox is successfully sent, the mailbox becomes empty. In such case, the TXSUSFLG bit of the CAN\_TXSTS register is set to 1

by hardware; the other is that the mailbox fails to transmit, the mailbox becomes predetermined and the transmitting request is aborted.

#### 24.4.5.4 Automatic retransmission is disabled

Generally, in time triggered communication mode, automatic retransmission should be disabled.

In the mode that the automatic retransmission is disabled, the message is sent only once, and no matter what the result is (success, error or arbitration loss), the hardware will not transmit the message again automatically.

When the transmitting process is finished, set the REQCFG bit of the CAN\_TXSTS register to 1, and the transmitting result will be on the TXSUSFLG, ARBLSTFLG and TXERRFLG bits.

#### 24.4.6 Data receiving

##### 24.4.6.1 Receive FIFO

CAN has two receive FIFOs, each FIFO has three mailboxes, the FMNUM[1:0] bit of the register CAN\_RXF reflects the number of messages currently stored; set the RFOM bit to 1 to release the output mailbox of receive FIFO; FFULLFLG is the full state flag bit; FOVRFLG is overrun state flag bit.

##### 24.4.6.2 Receive FIFO state conversion

At the beginning FIFO is in empty state, and after receiving the message, it will become registered.

When FIFO is in registered state and three mailboxes are full, after receiving next effective message, it will enter the overrun state, and there are two situations for loss of messages in overrun state:

- If FIFO lock function is disabled, the finally received message will be covered by new message
- If FIFO lock function is enabled, the newly received message will be discarded

#### 24.4.7 Filtering mechanism

Function of the filter: The receiving node decides whether the message is needed according to the message identifier, and only the required message will be received after filtering. CAN controller has 28 filter groups.

##### 24.4.7.1 Bit width

Each group of filters can configure two kinds of bit width.

Figure 103 One 32-bit Filter

|         |                    |                    |                   |                  |            |               |             |   |
|---------|--------------------|--------------------|-------------------|------------------|------------|---------------|-------------|---|
| ID      | CAN_FiBANK1[31:24] | CAN_FiBANK1[23:16] | CAN_FiBANK1[15:8] | CAN_FiBANK1[7:0] |            |               |             |   |
| Mapping | STDID[10:3]        | STDID[2:0]         | EXTID[17:13]      | EXTID[12:5]      | EXTID[4:0] | IDTYP<br>ESEL | TXRFR<br>EQ | 0 |

Figure 104 Two 16-bit Filters

| ID      | CAN_FiBANK1 [15:8] |  | CAN_FiBANK1 [7:0] |          |            |               | CAN_FiBANK2 [15:8] |  | CAN_FiBANK2 [7:0] |          |            |               |
|---------|--------------------|--|-------------------|----------|------------|---------------|--------------------|--|-------------------|----------|------------|---------------|
| Mapping | STDID [10:3]       |  | STDID [2:0]       | TXRF REQ | IDTYP ESEL | EXTID [17:15] | STDID [12:5]       |  | STDID [2:0]       | TXRF REQ | IDTYP ESEL | EXTID [17:15] |

## 24.4.7.2 Filtering mode

### Mask bit mode

In this mode, it is only required to use some bits of the message identifier as a list to form the mask, and the message ID should be the same as the mask, and then the message can be received

Table 102 Mask Bit Mode Example

|             |   |   |   |   |   |   |   |   |       |
|-------------|---|---|---|---|---|---|---|---|-------|
| ID          | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | ..... |
| Mask        | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | ..... |
| Screened ID | 1 | X | 1 | 1 | 0 | X | X | 0 | ..... |

### Identifier list mode

In this mode, each bit of the message ID needs to be the same as the filter identifier, and then the message can be received.

Table 103 Identifier List Mode Example

|             |   |   |   |   |   |   |   |   |   |
|-------------|---|---|---|---|---|---|---|---|---|
| ID          | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| ID          | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| Screened ID | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

## 24.4.7.3 Filter priority

The priority rules are as follows:

- The priority of the filter with bid width of 32 bits is higher than that with bid width of 16 bits
- Under the condition of the same bit width, the priority of the identifier list mode is higher than that of mask bit mode
- Under the condition of the same bit width and mode, the priority of the small filtering number is high

## 24.4.8 Bit timing and baud rate

### 24.4.8.1 Bit timing

The CAN peripheral bit timing of APM32 contains three segments: synchronization segment (SYNC\_SEG), time segment 1 (BS1) and time segment 2 (BS2), and the sampling points are at the junction of BS1 and BS2 segments.

- Synchronization segment (SYNC\_SEG): This bit occupies one time cell
- Time segment 1 (BS1): This segment occupies one to 16 time cells, and it contains PROP\_SEG and PHASE\_SEG1 in CAN standard
- Time segment 2 (BS2): This segment occupies one to eight time cells, and it represents PHASE\_SEG2 in CAN standard

### 24.4.8.2 Calculation of baud rate

Time of BS1 segment:  $Ts1 = Tq * (TIMSEG1[3:0] + 1)$

Time of BS2 segment:  $Ts2 = Tq * (TIMSEG2[2:0] + 1)$

Time of one data bit:  $T1bit = 1Tq + Ts1 + Ts2$

Baud rate =  $1 / T1bit$

$Tq = (BRPSC + 1) * TPCLK$

## 24.4.9 Error management

Transmit the error counter through the TXERRCNT bit of the configuration register CAN\_ERRSTS and receive the error counter through the RXERRCNT bit of the register CAN\_ERRSTS to reflect the error management of CAN bus.

Control the generation of interrupt in error state through the ERRIEN bit of the configuration register CAN\_INTEN.

### 24.4.9.1 Bus-line recovery

When the TXERRCNT of the CAN error state register is greater than 255, the CAN bus controller will enter the bus-line state, then the BOFLG bit of the register CAN\_ERRSTS is set to 1, and in this state, the CAN bus controller cannot receive and transmit messages.

Decide the bus-line recovery mode through the ALBOFFM bit of the configuration register CAN\_MCTRL:

- If the ALBOFFM bit is set to 1, once the hardware detects 11 continuous recessive bits for 128 times, it will exit the bus-line state automatically;
- If the ALBOFFM bit is set to 0, after the software requests to enter and then exit the initialization mode, it will exit the bus-line state.

## 24.4.10 Interrupt

### Events generating transmitting interrupt:

- The hardware sets REQCFLG0 bit of the register CAN\_TXSTS to 1, and the transmitting mailbox 0 becomes idle
- The hardware sets REQCFLG1 bit of the register CAN\_TXSTS to 1, and the transmitting mailbox 1 becomes idle
- The hardware sets REQCFLG2 bit of the register CAN\_TXSTS to 1, and the transmitting mailbox 2 becomes idle

### Events generating FIFO0 interrupt:

- Set the FMNUM0[1:0] bit of the register CAN\_RXF0 to a number rather than 0 by the hardware, and FIFO0 will receive a new message
- Set the FFULLFLG0 bit of the register CAN\_RXF0 to 1 by the hardware, and FIFO0 will be full
- Set the FOVRFLG0 bit of the register CAN\_RXF0 to 1 by the hardware and FIFO0 will overrun

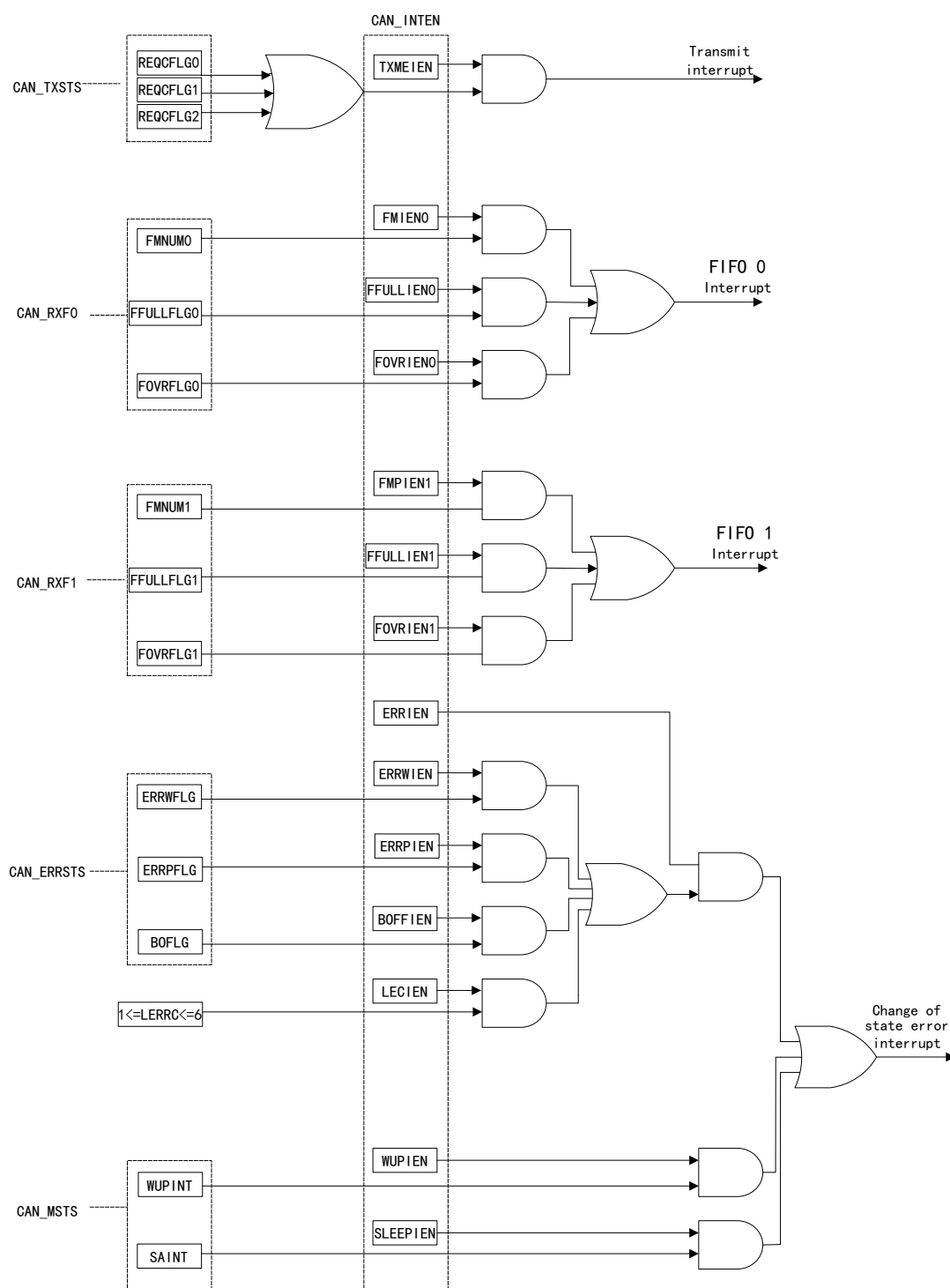
### Events generating FIFO1 interrupt:

- Set the FMNUM1[1:0] bit of the register CAN\_RXF1 to a number rather than 0 by the hardware, and FIFO1 will receive a new message
- Set the FFULLFLG1 bit of the register CAN\_RXF1 to 1 by the hardware, and FIFO1 will be full
- Set the FOVRFLG1 bit of the register CAN\_RXF1 to 1 by the hardware and FIFO1 will overrun

### Events generating state change and error interrupt:

- Set the SLEEPEN bit of the register CAN\_INTEN to 1 by the hardware and it will enter the sleep mode
- Set the WUPIEN bit of the register CAN\_INTEN to 1 by the hardware and interrupt enable will be woken up
- Set the ERRWFLG bit of the register CAN\_ERRSTS to 1 by the hardware, and it means that the number of errors has reached the threshold
- Set the ERRPFLG bit of the register CAN\_ERRSTS to 1 by the hardware, and it means that the number of errors has reached the threshold of passive error
- Set the LERRC[2:0] bit of the register CAN\_ERRSTS by the hardware, and it indicates the condition of last error

Figure 105 Event Flag and Interrupt Generation



## 24.5 Register address mapping

CAN1 base address: 0x4000\_6400

CAN2 base address: 0x4000\_6800

Note: Except base address, the register and offset addresses of CAN1 and CAN2 are exactly the same.



Table 104 CAN Register Address Mapping

| Register name | Description                                  | Offset address      |
|---------------|----------------------------------------------|---------------------|
| CAN_MCTRL     | CAN main control register                    | 0x00                |
| CAN_MSTS      | CAN main state register                      | 0x04                |
| CAN_TXSTS     | CAN transmit state register                  | 0x08                |
| CAN_RXF0      | CAN receive FIFO 0 register                  | 0x0C                |
| CAN_RXF1      | CAN receive FIFO 1 register                  | 0x10                |
| CAN_INTEN     | CAN interrupt enable register                | 0x14                |
| CAN_ERRSTS    | CAN error state register                     | 0x18                |
| CAN_BITTIM    | CAN bit timing register                      | 0x1C                |
| CAN_TXMIDx    | Transmitting mailbox identifier register     | 0x180, 0x190, 0x1A0 |
| CAN_TXDLENx   | Transmitting mailbox data length register    | 0x184, 0x194, 0x1A4 |
| CAN_TXMDLx    | Transmitting mailbox low-byte data register  | 0x188, 0x198, 0x1A8 |
| CAN_TXMDHx    | Transmitting mailbox high-byte data register | 0x18C, 0x19C, 0x1AC |
| CAN_RXMIDx    | Receive FIFO mailbox identifier register     | 0x1B0, 0x1C0        |
| CAN_RXDLENx   | Receive FIFO mailbox data length register    | 0x1B4, 0x1C4        |
| CAN_RXMDLx    | Receive FIFO mailbox low-byte data register  | 0x1B8, 0x1C8        |
| CAN_RXMDHx    | Receive FIFO mailbox high-byte data register | 0x1BC, 0x1CC        |
| CAN_FCTRL     | CAN filter control register                  | 0x200               |
| CAN_FMCFG     | CAN filter mode register                     | 0x204               |
| CAN_FSCFG     | CAN filter bit width configuration register  | 0x20C               |
| CAN_FFASS     | CAN filter FIFO association register         | 0x214               |
| CAN_FACT      | CAN filter activation register               | 0x21C               |
| CAN_FiBANKx   | Register x of CAN filter group i             | 0x240...0x31C       |

## 24.6 Register functional description

### 24.6.1 CAN control and state register

#### 24.6.1.1 CAN main control register (CAN\_MCTRL)

Offset address: 0x00

Reset value: 0x0001 0002

| Field | Name    | R/W | Description                                                                                                                                                      |
|-------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | INITREQ | R/W | Request to Enter Initialization Mode<br>0: Enter the normal work mode from the initialization mode<br>1: Enter the initialization mode from the normal work mode |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | SLEEPREQ | R/W | Request to Enter Sleep Mode<br>0: Exit the sleep mode<br>1: Request to enter the sleep mode.<br>If the AWUPCFG bit is set to 1, when the RX signal detects CAN message, this bit will be cleared by hardware; after reset, reset this bit to 1; after reset, it will enter the sleep mode.                                                                                                                                                                                   |
| 2     | TXFPCFG  | R/W | Transmit FIFO Priority Configure<br>This bit is used to determine which parameters determine the transmission priority when multiple messages are waiting for transmission.<br>0: Determined by the message identifier<br>1: Determined by the sequence of transmission request                                                                                                                                                                                              |
| 3     | RXFLOCK  | R/W | Receive FIFO Locked Mode Configure<br>This bit is used to determine whether FIFO is locked when receiving overrun, and how to deal with the next received message when the message of the receive FIFO has not been read out.<br>0: Unlocked; If the message of the receive FIFO is not read out, the next received message will cover the original message<br>1: Locked; when the message of the received FIFO is not read out, the next received message will be discarded |
| 4     | ARTXMD   | R/W | Automatic Retransmission Message Disable<br>0: Automatic retransmission is enabled, and the message will be retransmitted automatically until it is sent successfully<br>1: Automatic retransmission is disabled and the message is sent only once                                                                                                                                                                                                                           |
| 5     | AWUPCFG  | R/W | Automatic Wakeup Mode Configure<br>0: Software wakes up the sleep mode by clearing the SLEEPREQ bit of the CAN_MCTRL register<br>1: Hardware wakes up the sleep mode by detecting CAN message                                                                                                                                                                                                                                                                                |
| 6     | ALBOFFM  | R/W | Automatic Leaving Bus-Off Status Condition Management<br>0: After the software resets the INITREQ bit of the CAN_MCTRL register to 1 and then clears it, when the hardware detects 11 continuous recessive bits for 128 times, it will exit from the bus-line state<br>1: When the hardware detects 11 continuous recessive bits for 128 times, it will exit from the bus-line state automatically                                                                           |
| 14:7  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 15    | SWRST    | R/S | Software Reset CAN<br>0: Work normally<br>1: CAN is reset by force, and after reset, CAN enters the sleep mode; the hardware will clear this bit automatically                                                                                                                                                                                                                                                                                                               |
| 16    | DBGFRZE  | R/W | Debug Freeze<br>0: Invalid<br>1: During debugging, CAN cannot receive/transmit, but it still can read and write and control the receive FIFO normally                                                                                                                                                                                                                                                                                                                        |
| 31:17 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

#### 24.6.1.2 CAN main state register (CAN\_MSTS)

Offset address: 0x04

Reset value: 0x0000 0C02

| Field | Name      | R/W   | Description                                                                                                                                                                                                                                                                                                                  |
|-------|-----------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | INITFLG   | R     | Being Initialization Mode Flag<br>This bit is set to 1 or cleared by hardware.<br>1: Exit the initialization mode<br>1: Being in the initialization mode; this bit is confirmation for initialization request bit of the CAN_MCTRL register.                                                                                 |
| 1     | SLEEPFLG  | R     | Being Sleep Mode Flag<br>This bit is set to 1 or cleared by hardware<br>0: Exit the sleep mode<br>1: Being in the sleep mode; this bit is confirmation for sleep moderequest bit of the CAN_MCTRL register.                                                                                                                  |
| 2     | ERRIFLG   | RC_W1 | Error Interrupt Occur Flag<br>This bit is set to 1 by hardware and written to 1 and cleared by software.<br>0: Not occur<br>1: Occurred                                                                                                                                                                                      |
| 3     | WUIFLG    | RC_W1 | Wakeup Interrupt Occur Flag<br>When entering the sleep mode and detecting SOP wake-up, the bit is set to 1 by hardware; it is written to 1 and cleared by software.<br>0: Failed to wake up from the sleep mode<br>1: Woke up from the sleep mode                                                                            |
| 4     | SLEEIFLG  | RC_W1 | Being Sleep Mode Interrupt Flag<br>When entering the sleep mode, this bit is set to 1 by hardware and corresponding interrupt will be triggered; when exiting the sleep mode, this bit is cleared by hardware and is written as 1 and cleared by software.<br>0: Failed to enter the sleep mode<br>1: Entered the sleep mode |
| 7:5   | Reserved  |       |                                                                                                                                                                                                                                                                                                                              |
| 8     | TXMFLG    | R     | Being Transmit Mode Flag<br>0: CAN is not in transmission mode<br>1: CAN is in transmission mode                                                                                                                                                                                                                             |
| 9     | RXMFLG    | R     | Being Receive Mode Flag<br>0: CAN is not in receiving mode<br>1: CAN is in receiving mode                                                                                                                                                                                                                                    |
| 10    | LSAMVALUE | R     | CAN Rx Pin Last Sample Value                                                                                                                                                                                                                                                                                                 |
| 11    | RXSIGL    | R     | CAN Rx Pin Signal Level                                                                                                                                                                                                                                                                                                      |
| 31:12 | Reserved  |       |                                                                                                                                                                                                                                                                                                                              |

#### 24.6.1.3 CAN transmitting state register (CAN\_TXSTS)

Offset address: 0x08

Reset value: 0x1C00 0000

| Field | Name       | R/W   | Description                                                                                                                                                                                                                                                                                                                                   |
|-------|------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | REQCFLG0   | RC_W1 | <p>Mailbox 0 Request Completed Flag</p> <p>When the last transmission or abortion request of the mailbox 0 is completed, this bit is set to 1 by hardware; when receiving the transmission request, this bit is cleared by hardware; it is written to 1 or cleared by software.</p> <p>0: Being transmitted<br/>1: Transmission completed</p> |
| 1     | TXSUSFLG0  | RC_W1 | <p>Mailbox 0 Transmission Success Flag</p> <p>When mailbox 0 attempts to transmit successfully, this bit is set to 1 by hardware; and written to 1 and cleared by software.</p> <p>0: Last transmission attempt failed<br/>1: Last transmission attempt succeeded</p>                                                                         |
| 2     | ARBLSTFLG0 | RC_W1 | <p>Mailbox 0 Arbitration Lost Flag</p> <p>When the mailbox 0 loses arbitration, this bit is set to 1 by hardware; and written to 1 and cleared by software.</p> <p>0: Meaningless<br/>1: Lost</p>                                                                                                                                             |
| 3     | TXERRFLG0  | RC_W1 | <p>Mailbox 0 Transmission Error Flag</p> <p>When mailbox 0 fails to transmit, this bit is set to 1 by hardware; and written to 1 and cleared by software.</p> <p>0: Meaningless<br/>1: Failed to transmit</p>                                                                                                                                 |
| 6:4   | Reserved   |       |                                                                                                                                                                                                                                                                                                                                               |
| 7     | ABREQFLG0  | R/S   | <p>Mailbox 0 Abort Request Flag</p> <p>If there is no message waiting for Transmitting in mailbox 0, this bit is ineffective.</p> <p>0: The transmitting message of mailbox 0 is cleared, and this bit is cleared by hardware<br/>1: Set this bit to 1 to abort the transmission request of mailbox 0</p>                                     |
| 8     | REQCFLG1   | RC_W1 | <p>Mailbox 1 Request Completed Flag</p> <p>When the last request of mailbox 1 is sent or aborted, this bit is set to 1 by hardware; When receiving the transmission request, this bit is cleared by hardware, and written to 1 and cleared by software.</p> <p>0: Being transmitted<br/>1: Transmission completed</p>                         |
| 9     | TXSUSFLG1  | RC_W1 | <p>Mailbox 1 Transmission Success Flag</p> <p>When mailbox 1 attempts to transmit successfully, this bit is set to 1 by hardware; and written to 1 and cleared by software.</p> <p>0: Last transmission attempt failed<br/>1: Last transmission attempt succeeded</p>                                                                         |
| 10    | ARBLSTFLG1 | RC_W1 | <p>Mailbox 1 Arbitration Lost Flag</p> <p>When the mailbox 1 loses arbitration, this bit is set to 1 by hardware; and written to 1 and cleared by software.</p> <p>0: Meaningless<br/>1: Lost</p>                                                                                                                                             |

| Field | Name       | R/W   | Description                                                                                                                                                                                                                                                                                                                   |
|-------|------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11    | TXERRFLG1  | RC_W1 | Mailbox 1 Transmission Error Flag<br>When mailbox 1 fails to transmit, this bit is set to 1 by hardware; and written to 1 and cleared by software.<br>0: Meaningless<br>1: Failed to transmit                                                                                                                                 |
| 14:12 | Reserved   |       |                                                                                                                                                                                                                                                                                                                               |
| 15    | ABREQFLG1  | R/S   | Mailbox 1 Abort Request Flag<br>If there is no message waiting for transmitting in mailbox 1, this bit is ineffective.<br>0: The transmitting message of mailbox 1 is cleared, and this bit is cleared by hardware<br>1: Set this bit to 1 to abort the transmission request of mailbox 1                                     |
| 16    | REQCFLG2   | RC_W1 | Mailbox 2 Request Completed Flag<br>When the last transmission or abortion request of the mailbox 2 is completed, this bit is set to 1 by hardware; when receiving the transmission request, this bit is cleared by hardware; it is written to 1 or cleared by software.<br>0: Being transmitted<br>1: Transmission completed |
| 17    | TXSUSFLG2  | RC_W1 | Mailbox 2 Transmission Success Flag<br>When mailbox 2 attempts to transmit successfully, this bit is set to 1 by hardware; and written to 1 and cleared by software.<br>0: Last transmission attempt failed<br>1: Last transmission attempt succeeded                                                                         |
| 18    | ARBLSTFLG2 | RC_W1 | Mailbox 2 Arbitration Lost Flag<br>When the mailbox 2 loses arbitration, this bit is set to 1 by hardware; and written to 1 and cleared by software.<br>0: Meaningless<br>1: Lost                                                                                                                                             |
| 19    | TXERRFLG2  | RC_W1 | Mailbox 2 Transmission Error Flag<br>When mailbox 2 fails to transmit, this bit is set to 1 by hardware; and written to 1 and cleared by software.<br>0: Meaningless<br>1: Failed to transmit                                                                                                                                 |
| 22:20 | Reserved   |       |                                                                                                                                                                                                                                                                                                                               |
| 23    | ABREQFLG2  | R/S   | Mailbox 2 Abort Request Flag<br>If there is no message waiting for transmitting in mailbox 2, this bit is ineffective.<br>0: The transmitting message of mailbox 2 is cleared, and this bit is cleared by hardware<br>1: Set this bit to 1 to abort the transmission request of mailbox 2                                     |
| 25:24 | EMNUM[1:0] | R     | Empty Mailbox Number<br>This bit is applicable when there is empty mailbox. When all the Transmitting mailboxes are empty, it means the number of the transmitting mailbox with the lowest priority; when the mailbox is not empty but not all empty, it means the number of next mailbox to be sent.                         |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                    |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26    | TXMEFLG0 | R   | Transmit Mailbox 0 Empty Flag<br>When the Transmitting mailbox 0 is empty, this bit is set to 1 by hardware.<br>0: There is message to be sent in mailbox 0<br>1: There is no message to be sent in mailbox 0                                  |
| 27    | TXMEFLG1 | R   | Transmit Mailbox 1 Empty Flag<br>When the Transmitting mailbox 1 is empty, this bit is set to 1 by hardware.<br>0: There is message to be sent in mailbox 1<br>1: There is no message to be sent in mailbox 1                                  |
| 28    | TXMEFLG2 | R   | Transmit Mailbox 2 Empty Flag<br>When the transmitting mailbox 2 is empty, this bit is set to 1 by hardware.<br>0: There is message to be sent in mailbox 2<br>1: There is no message to be sent in mailbox 2                                  |
| 29    | LOWESTP0 | R   | The Lowest Transmission Priority Flag for Mailbox 0<br>0: Meaningless<br>1: The priority of mailbox 0 is the lowest among those mailboxes waiting to transmit messages<br>Note: If there is only one mailbox waiting, LOWESTP[2:0] is cleared. |
| 30    | LOWESTP1 | R   | The Lowest Transmission Priority Flag for Mailbox 1<br>0: Meaningless<br>1: The priority of mailbox 1 is the lowest among those mailboxes waiting to transmit messages                                                                         |
| 31    | LOWESTP2 | R   | The Lowest Transmission Priority Flag for Mailbox 2<br>0: Meaningless<br>1: The priority of mailbox 2 is the lowest among those mailboxes waiting to transmit messages                                                                         |

#### 24.6.1.4 CAN receive FIFO 0 register (CAN\_RXF0)

Offset address: 0x0C

Reset value: 0x00

| Field | Name        | R/W   | Description                                                                                                                                                                                                                                                                       |
|-------|-------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | FMNUM0[1:0] | R     | The number of Message in receive FIFO0<br>These bits are used to reflect the number of messages stored in current receive FIFO0. Every time a new message is received, add 1 to FMNUM0 bit; every time the mailbox message is released and outputted, subtract 1 from FMNUM0 bit. |
| 2     | Reserved    |       |                                                                                                                                                                                                                                                                                   |
| 3     | FFULLFLG0   | RC_W1 | Receive FIFO0 Full Flag<br>When there are three messages in FIFO0, it means the FIFO0 has been full; this bit is set to 1 by hardware and written to 1 and cleared by software.<br>0: Not full<br>1: Full                                                                         |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4     | FOVRFLG0 | RC_W1 | Receive FIFO 0 Overrun Flag<br>When there are three messages in FIFO0 and then a new message is received, it means the FIFO0 overrun; this bit is set to 1 by hardware and written to 1 and cleared by software.<br>0: No overrun<br>1: Overrun is generated                                                                                                     |
| 5     | RFOM0    | R/S   | Release Receive FIFO0 Output Mailbox to Receive Message<br>This bit is set to 1 by hardware and cleared by software. If there is no message in FIFO, this bit is invalid. When FIFO contains more than two messages, the output mailbox must be first released to access the second message.<br>0: Meaningless<br>1: Release the output mailbox of receive FIFO0 |
| 31:6  | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                  |

#### 24.6.1.5 CAN receive FIFO 1 register (CAN\_RXF1)

Offset address: 0x10

Reset value: 0x00

| Field | Name        | R/W   | Description                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | FMNUM1[1:0] | R     | The number of Message in receive FIFO1<br>These bits are used to reflect the number of messages stored in current receive FIFO1. Every time a new message is received, add 1 to FMNUM1 bit; every time the mailbox message is released and outputted, subtract 1 from FMNUM1 bit.                                                                                |
| 2     | Reserved    |       |                                                                                                                                                                                                                                                                                                                                                                  |
| 3     | FFULLFLG1   | RC_W1 | Receive FIFO0 Full Flag<br>When there are three messages in FIFO1, it means the FIFO1 has been full; this bit is set to 1 by hardware and written to 1 and cleared by software.<br>0: Not full<br>1: Full                                                                                                                                                        |
| 4     | FOVRFLG1    | RC_W1 | Receive FIFO1 Overrun Flag<br>When there are three messages in FIFO1 and then a new message is received, it means the FIFO1 overrun ; this bit is set to 1 by hardware and written to 1 and cleared by software.<br>0: No overrun<br>1: Overrun is generated                                                                                                     |
| 5     | RFOM1       | R/S   | Release Receive FIFO1 Output Mailbox to Receive Message<br>This bit is set to 1 by hardware and cleared by software. If there is no message in FIFO, this bit is invalid. When FIFO contains more than two messages, the output mailbox must be first released to access the second message.<br>0: Meaningless<br>1: Release the output mailbox of receive FIFO1 |
| 31:6  | Reserved    |       |                                                                                                                                                                                                                                                                                                                                                                  |

#### 24.6.1.6 CAN interrupt enable register (CAN\_INTEN)

Offset address: 0x14

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                |
|-------|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TXMEIEN   | R/W | <p>Transmit Mailbox Empty Interrupt Enable</p> <p>When REQCFGx bit is set to 1, it means transmission has been completed, and the transmitting mailbox is empty; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p>            |
| 1     | FMIEN0    | R/W | <p>Interrupt Enable When the Number of FIFO0 Message Is Not 0</p> <p>When FMNUM0[1:0] bit of FIFO 0 is not zero, it means that the number of messages in FIFO0 is not zero; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p> |
| 2     | FFULLIEN0 | R/W | <p>FIFO0 Full Interrupt Enable</p> <p>When the FFULLFLG0 bit of FIFO0 is set to 1, it means that the message of FIFO0 is full; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p>                                              |
| 3     | FOVRIEN0  | R/W | <p>FIFO0 Overrun Interrupt Enable</p> <p>When the FOVRFLG0 bit of FIFO0 is set to 1, it means that the FIFO0 has been overloaded; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p>                                           |
| 4     | FMIEN1    | R/W | <p>Interrupt Enable when the number of FIFO1 Message is not 0</p> <p>When FMNUM1[1:0] bit of FIFO 1 is not zero, it means that the number of messages in FIFO1 is not zero; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p> |
| 5     | FFULLIEN1 | R/W | <p>FIFO1 Full Interrupt Enable</p> <p>When the FFULLFLG1 bit of FIFO1 is set to 1, it means that the message of FIFO1 is full; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p>                                              |
| 6     | FOVRIEN1  | R/W | <p>FIFO1 Overrun Interrupt Enable</p> <p>When the FOVRFLG1 bit of FIFO1 is set to 1, it means that the FIFO1 has been overloaded; if this bit is set to 1, an interrupt will be generated.</p> <p>0: No interrupt<br/>1: Interrupt generated</p>                                           |
| 7     | Reserved  |     |                                                                                                                                                                                                                                                                                            |



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                 |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8     | ERRWIEN  | R/W | Error Warning Interrupt Enable<br>When ERRWFLG bit is set to 1, an error warning will occur; if this bit is set to 1, ERRIFLG shall be set and a warning error interrupt will be generated.<br>0: ERRIFLG bit is not set<br>1: ERRIFLG bit is set to 1                      |
| 9     | ERRPIEN  | R/W | Error Passive Interrupt Enable<br>When ERRPFLG bit is set to 1, a passive error will occur; if this bit is set to 1, ERRIFLG shall be set and a passive error interrupt will be generated.<br>0: ERRIFLG bit is not set<br>1: ERRIFLG bit is set to 1                       |
| 10    | BOFFIEN  | R/W | Bus-Off Interrupt Enable<br>When BOFFFLG bit is set to 1, bus-line will occur; if this bit is set to 1, ERRIFLG shall be set and an bus-line error interrupt will be generated.<br>0: ERRIFLG bit is not set<br>1: ERRIFLG bit is set to 1                                  |
| 11    | LECIEN   | R/W | Last Error Code Interrupt Enable<br>When an error is detected and the hardware sets LERRC [2:0], the last error code is recorded. If this bit set to 1, the ERRIFLG is set to generate the last error interrupt.<br>0: ERRIFLG bit is not set<br>1: ERRIFLG bit is set to 1 |
| 14:12 | Reserved |     |                                                                                                                                                                                                                                                                             |
| 15    | ERRIEN   | R/W | Error interrupt Enable<br>When the corresponding error state register is set to 1, if this bit is set to 1, an error interrupt will be generated.<br>0: No interrupt<br>1: Interrupt generated                                                                              |
| 16    | WUPIEN   | R/W | Wakeup Interrupt Enable<br>When WUPINT bit is set to 1, if this bit is set to 1, a wake-up interrupt will be generated.<br>0: No interrupt<br>1: Interrupt generated                                                                                                        |
| 17    | SLEEPEN  | R/W | Sleep Interrupt Enable<br>When SLEEPFLG bit is set to 1, if this bit is set to 1, a sleep interrupt will be generated.<br>0: No interrupt<br>1: Interrupt generated                                                                                                         |
| 31:18 | Reserved |     |                                                                                                                                                                                                                                                                             |

#### 24.6.1.7 CAN error state register (CAN\_ERRSTS)

Offset address: 0x18

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ERRWFLG  | R   | Error Warning Occur Flag<br>When the value of the receiving error counter or transmitting error counter $\geq 96$ , this bit is set to 1 by hardware.<br>0: No error warning<br>1: Error warning occurred                                                                                                                                                                                                          |
| 1     | ERRPFLG  | R   | Error Passive Occur Flag<br>When the value of the receiving error counter or transmitting error counter $\geq 127$ , this bit is set to 1 by hardware.<br>0: No passive error<br>1: Passive error occurred                                                                                                                                                                                                         |
| 2     | BOFLG    | R   | Enter Bus-Off Flag<br>When the value of the transmitting error counter TXERRCNT is greater than 255, CAN will enter the bus-line state and this bit is set to 1 by hardware.<br>0: CAN not in bus-line state<br>1: CAN in bus-line state                                                                                                                                                                           |
| 3     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 6:4   | LERRC    | R/W | Record Last Error Code<br>When the error on CAN bus is detected, it is set by hardware according to the error category; when the message is sent or received correctly, this bit is cleared by hardware.<br>000: No error<br>001: Bit stuffing error<br>010: Form (Form) error<br>011: Acknowledgment (ACK) error<br>100: Recessive bit error<br>101: Dominant bit error<br>110: CRC error<br>111: Set by software |
| 15:7  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 23:16 | TXERRCNT | R   | Least Significant Byte Of The 9-Bit Transmit Error Counter<br>The counter is implemented according to the transmission part of fault definition mechanism of CAN protocol.                                                                                                                                                                                                                                         |
| 31:24 | RXERRCNT | R   | Receive Error Counter<br>The receiving error counter is implemented according to the receiving part of fault definition mechanism of CAN protocol. When receiving error occurs, according to the condition of error, add 1 or 8 to the counter, and subtract 1 after receiving successfully. When the value of the counter is greater than 127, set the counter value to 120.                                      |

#### 24.6.1.8 CAN bit timing register (CAN\_BITTIM)

Offset address: 0x1C

Reset value: 0x0123 0000

| Field | Name  | R/W | Description                                                                       |
|-------|-------|-----|-----------------------------------------------------------------------------------|
| 9:0   | BRPSC | R/W | Baud Rate Prescaler Factor Setup<br>Time cell $t_q = (BRPSC + 1) \times t_{PCLK}$ |

| Field | Name     | R/W | Description                                                                                                              |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------|
| 15:10 | Reserved |     |                                                                                                                          |
| 19:16 | TIMSEG1  | R/W | Set the time segment 1 (Time Segment 1 Setup)<br>Time occupied by time period 1 $tBS1 = tCAN \times (TIMSEG1+1)$ .       |
| 22:20 | TIMSEG2  | R/W | Set the time segment 2 (Time Segment 2 Setup)<br>Time occupied by time period 2 $tBS2 = tCAN \times (TIMSEG2+1)$ .       |
| 23    | Reserved |     |                                                                                                                          |
| 25:24 | RSYNJW   | R/W | Resynchronization Jump Width<br>Time that CAN hardware can extend or shorten in this bit $tRJW=tCAN \times (RSYNJW+1)$ . |
| 29:26 | Reserved |     |                                                                                                                          |
| 30    | LBKMEN   | R/W | Loop Back Mode Enable<br>0: Disable<br>1: Enable                                                                         |
| 31    | SILMEN   | R/W | Silent Mode Enable<br>0: Normal state<br>1: Silent mode                                                                  |

Note: When CAN is in initialization mode, this register can be accessed only by software

## 24.6.2 CAN mailbox register

This section describes the transmitting and receiving mailbox registers.

The transmitting and receiving mailboxes are almost the same except the following examples:

- FMIDX domain of CAN\_RXDLENx register;
- The receiving mailbox is read-only;
- The transmitting mailbox is writable only when it is empty, and if the corresponding TXMEFLG bit of CAN\_TXSTS register is 1, it means the transmitting mailbox is empty.

There are three transmitting mailboxes and two receiving mailboxes in total.

Each receiving mailbox is FIFO with three levels of depth, and can only access the message that is received first in FIFO.

### 24.6.2.1 Transmitting mailbox identifier register (CAN\_TXMIDx) (x=0...2)

Offset address: 0x180, 0x190, 0x1A0

Reset value: 0xFFFF XXXX, X=undefined bit (except Bit 0, TXMREQ=0 after reset)

| Field | Name    | R/W | Description                                                                                                                                                                                            |
|-------|---------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TXMREQ  | R/W | Transmit Mailbox Data Request<br>0: When the data in the mailbox is sent, the mailbox is empty and this bit is cleared by hardware<br>1: Software writes 1, to enable request to transmit mailbox data |
| 1     | TXRFREQ | R/W | Transmit Remote Frame Request<br>0: Data frame<br>1: Remote frame                                                                                                                                      |

| Field | Name                     | R/W | Description                                                                                                                                                                                 |
|-------|--------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | IDTYPESEL                | R/W | Identifier Type Select<br>0: Standard identifier<br>1: Extended identifier                                                                                                                  |
| 20:3  | EXTID[17:0]              | R/W | Extended Identifier Setup<br>Low byte of extended identity label.                                                                                                                           |
| 31:21 | STDID[10:0]/EXTID[28:18] | R/W | Standard Identifier or Extended Identifier<br>According to the content of IDTYPESEL bit, these bits are standard identifier STDID [10:0] and high byte EXTID[28:18] of extended identifier. |

Note:

- (1) When its mailbox is in the state of waiting for transmission, this register is write-protected.
- (2) This register achieves transmission request control function (No. 0 bit) - the reset value is 0.

#### 24.6.2.2 Transmitting mailbox data length register (CAN\_TXDLENx) (x=0...2)

Offset address: 0x184, 0x194, 0x1A4

Reset value: 0xFFFF XXXX

When the mailbox is not idle, all bits of this register are write-protected.

| Field | Name     | R/W | Description                     |
|-------|----------|-----|---------------------------------|
| 3:0   | DLCODE   | R/W | Transmit Data Length Code Setup |
| 31:4  | Reserved |     |                                 |

#### 24.6.2.3 Transmitting mailbox low-byte data register (CAN\_TXMDLx) (x=0...2)

Offset address: 0x188, 0x198, 0x1A8

Reset value: 0xFFFF XXXX

When the mailbox is not idle, all bits of this register are write-protected, and the message contains 0 to 7-byte data and starts from the byte 0.

| Field | Name      | R/W | Description                |
|-------|-----------|-----|----------------------------|
| 7:0   | DATABYTE0 | R/W | Data Byte 0 of the Message |
| 15:8  | DATABYTE1 | R/W | Data Byte 1 of the Message |
| 23:16 | DATABYTE2 | R/W | Data Byte 2 of the Message |
| 31:24 | DATABYTE3 | R/W | Data Byte 3 of the Message |

#### 24.6.2.4 Transmitting mailbox high-byte data register (CAN\_TXMDHx) (x=0...2)

Offset address: 0x18C, 0x19C, 0x1AC

Reset value: 0xFFFF XXXX, X=undefined bit

When the mailbox is not idle, all bits of this register are write-protected.

| Field | Name      | R/W | Description                |
|-------|-----------|-----|----------------------------|
| 7:0   | DATABYTE4 | R/W | Data Byte 4 of the Message |
| 15:8  | DATABYTE5 | R/W | Data Byte 5 of the Message |
| 23:16 | DATABYTE6 | R/W | Data Byte 6 of the Message |

| Field | Name      | R/W | Description                |
|-------|-----------|-----|----------------------------|
| 31:24 | DATABYTE7 | R/W | Data Byte 7 of the Message |

#### 24.6.2.5 Receive FIFO mailbox identifier register (CAN\_RXMIDx) (x=0...1)

Offset address: 0x1B0, 0x1C0

Reset value: 0xFFFF XXXX, X=undefined bit

| Field | Name                     | R/W | Description                                                                                                                                                                                 |
|-------|--------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Reserved                 |     |                                                                                                                                                                                             |
| 1     | RFTXREQ                  | R   | Remote Frame Transmission Request<br>0: Data frame<br>1: Remote frame                                                                                                                       |
| 2     | IDTYPESEL                | R   | Identifier Type Select<br>0: Standard identifier<br>1: Extended identifier                                                                                                                  |
| 20:3  | EXTID[17:0]              | R   | Extended Identifier Setup<br>Low byte of extended identifier.                                                                                                                               |
| 31:21 | STDID[10:0]/EXTID[28:18] | R   | Standard Identifier or Extended Identifier<br>According to the content of IDTYPESEL bit, these bits are standard identifier STDI [10:0] and high byte EXTID [28:18] of extended identifier. |

Note: All receiving mailbox registers are read-only.

#### 24.6.2.6 Receive FIFO mailbox data length register (CAN\_RXDLENx) (x=0...1)

Offset address: 0x1B4, 0x1C4

Reset value: 0xFFFF XXXX

| Field | Name     | R/W | Description                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | DLCODE   | R   | Receive Data Length Code Setup<br>This bit represents the data length in the frame; for remote frame, DLCODE is constantly 0. |
| 7:4   | Reserved |     |                                                                                                                               |
| 15:8  | FMIDX    | R   | Filter Match Index Setup                                                                                                      |
| 31:16 | Reserved |     |                                                                                                                               |

Note: All receiving mailbox registers are read-only.

#### 24.6.2.7 Receive FIFO mailbox low-byte data register (CAN\_RXMDLx) (x=0..1)

Offset address: 0x1B8, 0x1C8; the message contains 0 to 8-byte data, which starts from the byte 0.

Reset value: 0xFFFF XXXX

| Field | Name      | R/W | Description                |
|-------|-----------|-----|----------------------------|
| 7:0   | DATABYTE0 | R   | Data Byte 0 of the Message |
| 15:8  | DATABYTE1 | R   | Data Byte 1 of the Message |
| 23:16 | DATABYTE2 | R   | Data Byte 2 of the Message |

| Field | Name      | R/W | Description                |
|-------|-----------|-----|----------------------------|
| 31:24 | DATABYTE3 | R   | Data Byte 3 of the Message |

Note: All receiving mailbox registers are read-only.

#### 24.6.2.8 Receive FIFO mailbox high-byte data register (CAN\_RXMDHx) (x=0...1)

Offset address: 0x1BC, 0x1CC

Reset value: 0xFFFF XXXX, X=undefined bit

| Field | Name      | R/W | Description                |
|-------|-----------|-----|----------------------------|
| 7:0   | DATABYTE4 | R   | Data Byte 4 of the Message |
| 15:8  | DATABYTE5 | R   | Data Byte 5 of the Message |
| 23:16 | DATABYTE6 | R   | Data byte 6 of the Message |
| 31:24 | DATABYTE7 | R   | Data byte 7 of the Message |

Note: All receiving mailbox registers are read-only.

### 24.6.3 CAN filter register

#### 24.6.3.1 CAN filter control register (CAN\_FCTRL)

Offset address: 0x200

Reset value: 0x2A1C 0E01

| Field | Name     | R/W | Description                                                                                                                                                                                                                                    |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | FINITEN  | R/W | Filter Init Mode Enable<br>0: Normal mode<br>1: Initialization mode                                                                                                                                                                            |
| 7:1   | Reserved |     |                                                                                                                                                                                                                                                |
| 13:8  | CAN2SB   | R/W | CAN2 Start Bank<br>They define the start bank for the CAN2 interface (Slave) in the range 0 to 27.<br>Note: When CAN2SB[5:0] = 28d, all the filters to CAN1 can be used.<br>When CAN2SB[5:0] is set to 0, all the filters to CAN2 can be used. |
| 31:14 | Reserved |     |                                                                                                                                                                                                                                                |

Note: The non-reserved bit of this register is completely controlled by software.

#### 24.6.3.2 CAN filter mode configuration register (CAN\_FCFG)

Offset address: 0x204

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------|
| 27:0  | FMCFGx   | R/W | Filter Mode Configure<br>The value of x is within 0-27.<br>0: Identifier mask bit mode<br>1: Identifier list mode |
| 31:28 | Reserved |     |                                                                                                                   |

Note: Only when CAN\_FCTRL (FINITEN =1) is set to make the filter in initialization mode, can this register be written.

### 24.6.3.3 CAN filter bit width configuration register (CAN\_FSCFG)

Offset address: 0x20C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------|
| 27:0  | FSCFGx   | R/W | Filterx Scale Configure<br>The value of x is within 0-27.<br>0: Two 16 bits<br>1: Single 32 bits |
| 31:28 | Reserved |     |                                                                                                  |

Note: Only when CAN\_FCTRL (FINITEN =1) is set to make the filter in initialization mode, can this register be written.

### 24.6.3.4 CAN filter FIFO association register (CAN\_FFASS)

Offset address: 0x214

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                                                       |
|-------|---------|-----|-----------------------------------------------------------------------------------------------------------------------------------|
| 0     | FFASS0  | R/W | Configure Filter0 Associated with FIFO<br>0: The filter is associated with FIFO0<br>1: The filter is associated with FIFO1        |
| 1     | FFASS1  | R/W | Configure Filter1 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 2     | FFASS2  | R/W | Configure Filter2 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 3     | FFASS3  | R/W | Configure Filter3 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 4     | FFASS4  | R/W | Configure Filter4 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 5     | FFASS5  | R/W | Configure Filter5 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 6     | FFASS6  | R/W | Configure Filter6 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 7     | FFASS7  | R/W | Configure Filter7 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 8     | FFASS8  | R/W | Configure the filter 8 associated with FIFO (Configure Filter8 Associated with FIFO)<br>Refer to FFASS0 for specific description. |
| 9     | FFASS9  | R/W | Configure Filter9 Associated with FIFO<br>Refer to FFASS0 for specific description.                                               |
| 10    | FFASS10 | R/W | Configure Filter10 Associated with FIFO<br>Refer to FFASS0 for specific description.                                              |
| 11    | FFASS11 | R/W | Configure Filter11 Associated with FIFO<br>Refer to FFASS0 for specific description.                                              |
| 12    | FFASS12 | R/W | Configure Filter12 Associated with FIFO<br>Refer to FFASS0 for specific description.                                              |

| Field | Name     | R/W | Description                                                                          |
|-------|----------|-----|--------------------------------------------------------------------------------------|
| 13    | FFASS13  | R/W | Configure Filter13 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 14    | FFASS14  | R/W | Configure Filter14 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 15    | FFASS15  | R/W | Configure Filter15 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 16    | FFASS16  | R/W | Configure Filter16 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 17    | FFASS17  | R/W | Configure Filter17 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 18    | FFASS18  | R/W | Configure Filter18 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 19    | FFASS19  | R/W | Configure Filter19 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 20    | FFASS20  | R/W | Configure Filter20 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 21    | FFASS21  | R/W | Configure Filter21 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 22    | FFASS22  | R/W | Configure Filter22 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 23    | FFASS23  | R/W | Configure Filter23 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 24    | FFASS24  | R/W | Configure Filter24 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 25    | FFASS25  | R/W | Configure Filter25 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 26    | FFASS26  | R/W | Configure Filter26 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 27    | FFASS27  | R/W | Configure Filter27 Associated with FIFO<br>Refer to FFASS0 for specific description. |
| 31:28 | Reserved |     |                                                                                      |

Note: Only when CAN\_FCTRL (FINITEN =1) is set to make the filter in initialization mode, can this register be written.

#### 24.6.3.5 CAN filter activation register (CAN\_FACT)

Offset address: 0x21C

Reset value: 0x0000 0000

| Field | Name  | R/W | Description                                                |
|-------|-------|-----|------------------------------------------------------------|
| 0     | FACT0 | R/W | Filter0 Active<br>0: Disable<br>1: Active                  |
| 1     | FACT1 | R/W | Filter1 Active<br>Refer to FACT0 for specific description. |



| Field | Name   | R/W | Description                                                  |
|-------|--------|-----|--------------------------------------------------------------|
| 2     | FACT2  | R/W | Filter2 Active<br>Refer to FACT0 for specific description.   |
| 3     | FACT3  | R/W | Filter3 Active<br>Refer to FACT0 for specific description.   |
| 4     | FACT4  | R/W | Filter4 Active<br>Refer to FACT0 for specific description.   |
| 5     | FACT5  | R/W | Filter5 Active<br>Refer to FACT0 for specific description.   |
| 6     | FACT6  | R/W | Filter6 Active<br>Refer to FACT0 for specific description.   |
| 7     | FACT7  | R/W | Filter7 Active<br>Refer to FACT0 for specific description.   |
| 8     | FACT8  | R/W | Filter8 Active<br>Refer to FACT0 for specific description.   |
| 9     | FACT9  | R/W | Filter9 Active<br>Refer to FACT0 for specific description.   |
| 10    | FACT10 | R/W | Filter10 Active<br>Refer to FACT0 for specific description.  |
| 11    | FACT11 | R/W | Filter11 Active<br>Refer to FACT0 for specific description.  |
| 12    | FACT12 | R/W | Filter12 Active)<br>Refer to FACT0 for specific description. |
| 13    | FACT13 | R/W | Filter13 Active<br>Refer to FACT0 for specific description.  |
| 14    | FACT14 | R/W | Filter14 Active<br>Refer to FACT0 for specific description.  |
| 15    | FACT15 | R/W | Filter15 Active<br>Refer to FACT0 for specific description.  |
| 16    | FACT16 | R/W | Filter16 Active<br>Refer to FACT0 for specific description.  |
| 17    | FACT17 | R/W | Filter17 Active<br>Refer to FACT0 for specific description.  |
| 18    | FACT18 | R/W | Filter18 Active<br>Refer to FACT0 for specific description.  |
| 19    | FACT19 | R/W | Filter19 Active<br>Refer to FACT0 for specific description.  |
| 20    | FACT20 | R/W | Filter20 Active<br>Refer to FACT0 for specific description.  |
| 21    | FACT21 | R/W | Filter21 Active<br>Refer to FACT0 for specific description.  |
| 22    | FACT22 | R/W | Filter22 Active<br>Refer to FACT0 for specific description.  |
| 23    | FACT23 | R/W | Filter23 Active<br>Refer to FACT0 for specific description.  |

| Field | Name     | R/W | Description                                                 |
|-------|----------|-----|-------------------------------------------------------------|
| 24    | FACT24   | R/W | Filter24 Active<br>Refer to FACT0 for specific description. |
| 25    | FACT25   | R/W | Filter25 Active<br>Refer to FACT0 for specific description. |
| 26    | FACT26   | R/W | Filter26 Active<br>Refer to FACT0 for specific description. |
| 27    | FACT27   | R/W | Filter27 Active<br>Refer to FACT0 for specific description. |
| 31:28 | Reserved |     |                                                             |

#### 24.6.3.6 Register x of CAN filter group i (CAN\_FiBANKx) (i=0...27; x=1...2)

Offset address: 0x240...0x31C

CAN\_F0BANK1 offset address: 0x240      CAN\_F0BANK2 offset address: 0x244

CAN\_F1BANK1 offset address: 0x248      CAN\_F1BANK2 offset address:  
0x24C

The following offset addresses can be obtained in the same way.

Reset value: 0xFFFF XXXX

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | FBIT[31:0] | R/W | Filter Bits Setup<br>Identifier list mode:<br>0: FBITx bit is dominant bit<br>1: FBITx bit is recessive bit<br>Identifier mask bit mode:<br>0: FBITx is not used for comparison<br>1: FBITx must match<br>Note: The value of x is 0~31, indicating the bit number of FBIT. |

Note: There are 28 sets of filters in product: i=0...27. Each set of filters consists of two 32-bit registers and CAN\_FiBANK [2:1]. The corresponding filter registers can be modified only when the corresponding FACTx bit of CAN\_FACT register is cleared or the FINITEN bit of CAN\_FCTRL register is 1.

## 25 Secure Digital Input/Output Interface (SDIO)

### 25.1 Full name and abbreviation description of terms

Table 105 Full name and abbreviation description of terms

| Full name in English       | English abbreviation |
|----------------------------|----------------------|
| First Input First Output   | FIFO                 |
| Command Path State Machine | CPSM                 |
| Data Path State Machine    | DPSM                 |

### 25.2 Introduction

The secure digital input/output interface can connect SD card, SD I/O card, multi-media card (MMC) and CE-ATA card master interfaces, and provide data transmission between APB2 system bus and SD memory card, SD I/O card, MMC and CE-ATA device.

### 25.3 Main characteristics

- (1) SD card: Compatible with SD memory card specification version 2.0
- (2) SD I/O card: Compatible with SD I/O card specification version 2.0: support two different bus modes: 1 bit (default) and 4 bits.
- (3) MMC: Compatible with multimedia card system specification 4.2 and previous versions. Three different data bus modes are supported: 1 bit (default), 4 bits and 8 bits.
- (4) CE-ATA: Compatible with CE-ATA digital protocol version 1.1.
- (5) The data transmission rate in 8-bit bus mode is up to 48MHz
- (6) Interrupt and DMA request
- (7) Data and command output enable signal, used for controlling bidirectional driver.

Note: SDIO of current version only supports one SD/SD IO/MMC 4.2 card at the same time, however, it supports multiple MMC4.1 or cards of previous version.

### 25.4 Functional description

SDIO structure mainly contains two parts:

SDIO adapter: Achieves the related functions of MMC/SD/SD I/O cards, and consist of control unit, data unit and command unit. The control unit manages

the clock signal, the data unit manages the data transmission, and the command unit manages the command transmission.

APB2 bus interface: Operate the registers in SDIO adapter, used for FIFO unit for data transmission, generate an interrupt and DMA request signal.

Figure 106 SDIO Structure Block Diagram

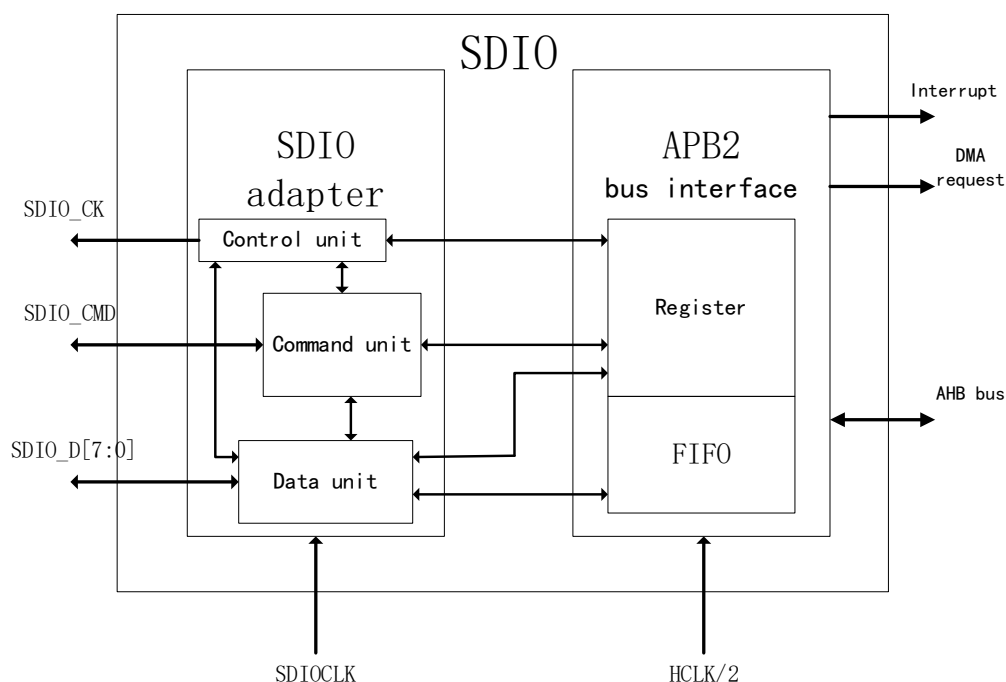


Table 106 SDIO Pin Definition

| Pin         | Direction | Description                                         |
|-------------|-----------|-----------------------------------------------------|
| SDIO_CK     | Output    | MMC/SD/SD I/O clock, clock line from master to card |
| SDIO_CMD    | Bilateral | MMC/SD/SD I/O command, bidirectional command signal |
| SDIO_D[7:0] | Bilateral | MMC/SD/SD I/O data, bidirectional data bus          |

### 25.4.1 SDIO bus topology

After power-on reset, the master must initialize the device through a special message-based bus protocol.

Each message is represented by one of the following parts:

- **Command:** Command is a token to start an operation, from the master to the card, and the command is transmitted to the CMD line serially.
- **Response:** From the card to the master, as a response to the previously received command, the response is transmitted onto the CMD serially.
- **Data:** It can be transmitted from the master to the card or from the card to the master. Transmit through data cable. The number of data cables for data transmission can be 1 (D0), 4 (D0-D3), or 8 (D0-D7).

The basic operation on the multimedia card, SD or SD I/O bus is command/response structure.

The data transmitted on SD/SD I/O memory card is transmitted in the form of data block; the data transmitted on MMC is transmitted in the form of data block or data stream; the data transmitted on CE-ATA device is also transmitted in the form of data block.

Figure 107 SDIO "No-response" and "No-data" Operation

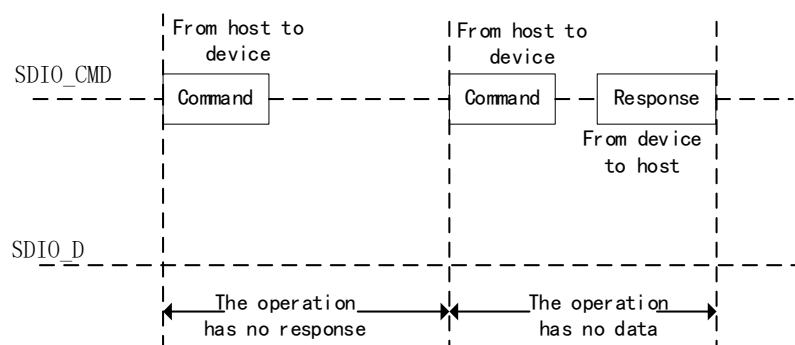


Figure 108 SDIO (Multi-) Data Block Read Operation

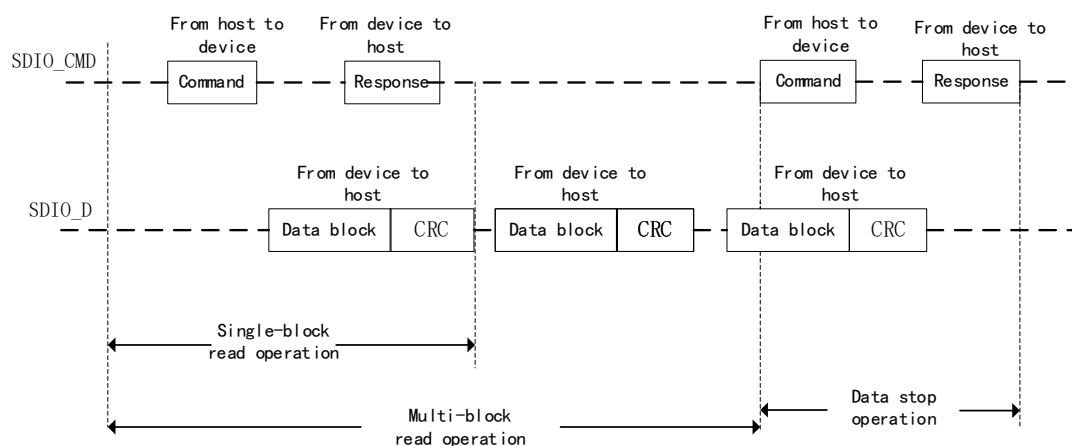


Figure 109 SDIO (Multi-) Data Block Write Operation

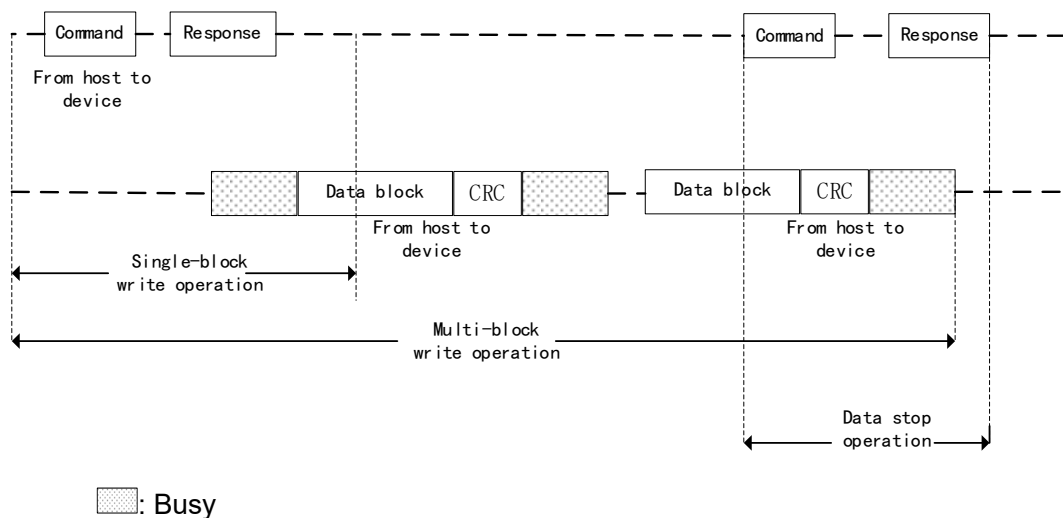


Figure 110 SDIO Data Flow Read Operation

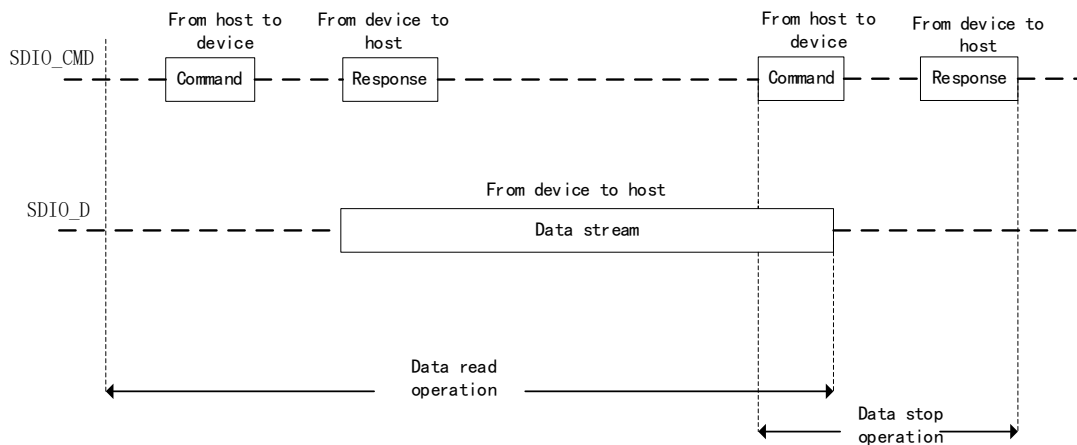
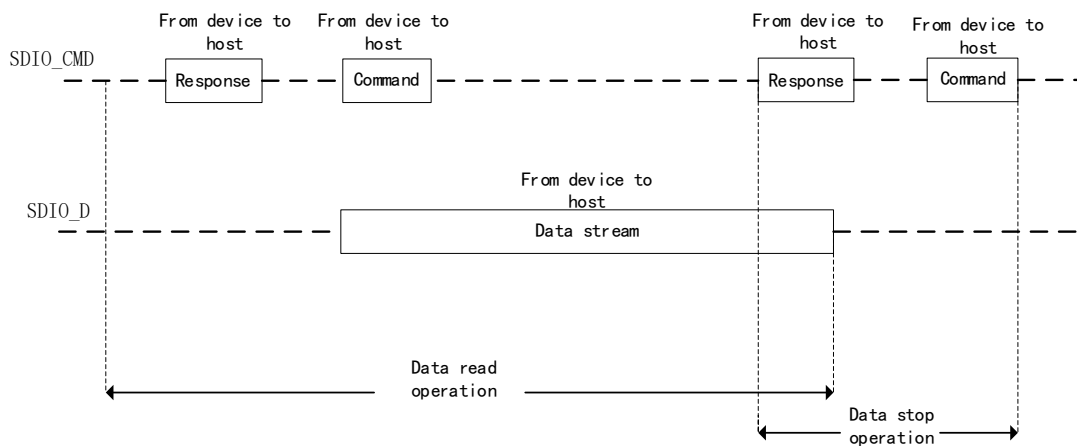


Figure 111 SDIO Data Flow Write Operation



## 25.4.2 SDIO Adapter

SDIO generates the following signals:

- **SDIO\_CLK**: Clock provided by SDIO controller to the card. Each clock cycle directly transmits 1-bit command or data on the command line (SDIO\_CMD) and all data lines (SDIO\_D). SDIO\_CLK frequency is within 0-20MHz for MMC card V3.31, within 0-48MHz for MMC card V4.2, and within 0-25MHz for SD or SD I/O card.
- **SDIO\_CMD**: The signal is a bidirectional command channel, which is used for card initialization and command transmission. Command is sent from SDIO controller to the card, and the response is sent from the card to the master. There are two operation modes of CMD signal: the open-drain mode of initialization (used for MMC card V3.31 and previous versions) and the push-pull mode of command transmitting (SD, SD I/O, and MMC card V4.2 initialization are also push-pull mode).
- **SDIO\_D[7:0]**: The signal lines are bidirectional data channels and in push-pull mode. By default, after power-on or reset, only D0 is used for data transmission. SDIO adapter can be configured with wider

data bus for data transmission, using D0-D3 and D0-D7 (only on MMC V4.2).

## Control unit

The control unit includes power management and clock management functions.

## Command unit

The command unit realizes transmitting commands to the card and receiving commands from the card, and the data transmission is controlled by the command state machine (CPSM).

## Command state machine

CS\_Idle gets ready to transmit the command after reset

- |                                             |   |         |
|---------------------------------------------|---|---------|
| 1. CPSM is enabled and WAITDEND is enabled  | → | CS_Pend |
| 2. CPSM is enabled and WAITDEND is disabled | → | CS_Send |
| 3. CPSM is turned off                       | → | CS_Idle |

Note: The idle state of command state machine is maintained for at least 8 SDIO\_CLK cycles, so as to meet the timing restriction of  $N_{CC}$  and  $N_{RC}$ .

$N_{CC}$ : Minimum time interval between two host commands

$N_{RC}$ : Minimum time interval between host command and card response

CS\_Pend waits for the end of data transmission

- |                                   |   |         |
|-----------------------------------|---|---------|
| 1. Data transmission is completed | → | CS_Send |
| 2. CPSM is turned off             | → | CS_Idle |

CS\_Send transmits commands

- |                                                          |   |         |
|----------------------------------------------------------|---|---------|
| 1. There is response after the command is transmitted    | → | CS_Wait |
| 2. There is no response after the command is transmitted | → | CS_Idle |
| 3. CPSM is turned off                                    | → | CS_Idle |

CS\_Wait waits for response start bit

- |                                                      |   |         |
|------------------------------------------------------|---|---------|
| 1. Received the response (the start bit is detected) | → | CS_Wait |
| 2. Receiving response times out                      | → | CS_Idle |
| 3. CPSM is turned off                                | → | CS_Idle |

Note: The command timeout period is fixed as 64 SDIO\_CLK clock cycles

CS\_Receive receives response and detects CRC

1. Receive the response in CE-ATA mode, disable CE-ATA interrupt and wait for enabling of CE-ATA device command completion signal → CS\_Waitcompl
2. Receive the response in CE-ATA mode, disable CE-ATA interrupt and wait for disabling of CE-ATA device command completion signal → CS\_Pend
3. CPSM is turned off → CS\_Idle
4. Receive the response → CS\_Idle
5. The command CRC detection fails → CS\_Idle

CS\_Waitcompl waits for CE-ATA device command completion signal

1. Receive CE-ATA command completion signal → CS\_Idle
2. CPSM is turned off → CS\_Idle
3. The command CRC detection fails → CS\_Idle

## Data unit

The data unit implements the data transmission between the master and the card. When the data width is 8 bits, SDIO\_D[7:0] signal line is used for data transmission. When the data width is 4 bits, SDIO\_D[3:0] signal line is used for data transmission. When the data width is 1 bit, SDIO\_D[0] signal line is used for data transmission.

Data transmission stream is controlled by data state machine (DPSM).

## Data state machine

DS\_Idle data unit is idle, waiting for transmitting and receiving data

1. DPSM is enabled and the data are transmitted from host to card → DS\_WaitS
2. DPSM is enabled and the data are transmitted from card to host → DS\_WaitR
3. DPSM is enabled, read wait has started and SDIO mode is enabled → DS\_Readwait

DS\_WsitS waits that the empty data FIFO flag is invalid or data transmission ends

1. Data transmission ends → DS\_Idle
2. DPSM is turned off → DS\_Idle
3. The empty data FIFO flag is invalid → DS\_Send



| DS_Send transmits data to the card         |   |         |
|--------------------------------------------|---|---------|
| 1. The data have been transmitted          | → | DS_Busy |
| 2. DPSM is turned off                      | → | DS_Idle |
| 3. Data FIFO underrun error is transmitted | → | DS_Idle |
| 4. Internal CRC error                      | → | DS_Idle |

| DS_Busy waits for CRC state flag           |   |         |
|--------------------------------------------|---|---------|
| 1. The data have been transmitted          | → | DS_Busy |
| 2. DPSM is turned off                      | → | DS_Idle |
| 3. Data FIFO underrun error is transmitted | → | DS_Idle |
| 4. Internal CRC error                      | → | DS_Idle |

| DS_WaitR waits for the start bit of received data |   |            |
|---------------------------------------------------|---|------------|
| 1. Data receiving ends                            | → | DS_Idle    |
| 2. DPSM is turned off                             | → | DS_Idle    |
| 3. Data timeout                                   | → | DS_Idle    |
| 4. Receive the start bit before timeout           | → | DS_Receive |

| DS_Receive receives the card data and writes them to data FIFO             |   |             |
|----------------------------------------------------------------------------|---|-------------|
| 1. The data block has been received                                        | → | DS_WaitR    |
| 2. The data transmission ends                                              | → | DS_WaitR    |
| 3. The data FIFO underrun is transmitted                                   | → | DS_Idle     |
| 4. The data have been received, read wait starts and SDI/O mode is enabled | → | DS_Readwait |
| 5. DPSM is turned off or CRC error occurs                                  | → | DS_Idle     |

| DS_Readwait waits for "read wait stop" command |   |          |
|------------------------------------------------|---|----------|
| 1. "Read wait stop" is enabled                 | → | DS_WaitR |
| 2. DPSM is turned off                          | → | DS_Idle  |

### 25.4.3 APB2 interface

APB2 interface implements access to SDIO register, data FIFO and generation of interrupt and DMA request. It includes data FIFO unit, register unit and interrupt/DMA request control logic.

#### SDIO interrupt

When at least one of the selected state flags is high, the interrupt logic will generate an interrupt request. Interrupt enable register enables the interrupt logic to generate corresponding interrupt.

### **Data FIFO**

The data FIFO unit has a data buffer area for receive and transmit FIFO. FIFO includes a data buffer with 32-bit width for each word and with depth of 32 words. The transmit FIFO is used when data needs to be written to the card; the data to be transmitted is written to the transmit FIFO through APB2 bus, and the data unit in SDIO adapter reads data from the transmit FIFO and then transmits the data to the card. The receive FIFO is used to read data from the card, and then write the data to be transmitted to the receive FIFO.

### **Register unit**

The register unit includes all system registers and generates signals for communication between the control card and the controller.

## **25.4.4 Card Function Description**

### **25.4.4.1 Card register**

The card internally defines the interface registers: OCR, CID, CSD, EXT\_CSD, RCA, DSR and SCR. These registers can access only through corresponding commands. OCR, CID, CSD and SCR registers include the specific information of the card. RCA and DSR registers are configuration registers for storing the actual configuration parameters. EXT\_CSD register includes both the specific information of the card and the actual structure parameters.

OCR register: 32-bit operating condition register stores  $V_{DD}$  voltage description and memory mode indication (MMC) of the card. In addition, the register includes a state information bit. If the card power-on process has been completed, this state bit will be set. This register is slightly different between MMC and SD card. The master can use CMD1 (MMC), ACMD41 (SD memory card), and CMD5 (SD I/O) to capture the content of this register.

CID register: The card identification register (CID) is 128-bit wide. It contains the card identification information used in the card identification phase. Each read/write (RW) card shall have a unique identification number.

CSD register: The specific card data register provides the content information in the access card. CSD defines data format, error correction type, maximum data access time, and data transmission speed.

Extended CSD register: Only MMC4.2 has this register. Extended CSD register defines the card attributes and selection mode. Its length is 512 bytes. At most 320 bytes are the attribute section, which defines the function of the card and cannot be modified by the master. At least 192 bytes are the mode section,

which defines under which configuration the card works.

**RCA register:** The writable 16-bit relative card address register stores the card address, which is released by the card during card initialization. This address is used for communication between the addressing master and the card after the card identification process.

**DSR register:** 16-bit drive stage register, which can be used to improve bus performance in extended operating conditions (depending on bus length, transmission rate and other parameters).

**SCR register:** Only SD/SD I/O has this register.

#### 25.4.4.2 Command

The command for the control card consists of four different types:

Table 107 Command Type

| Command type                                                 | Meaning                                                                       |
|--------------------------------------------------------------|-------------------------------------------------------------------------------|
| Broadcast command (BC)                                       | Transmit to all cards, but there is no response returned                      |
| Broadcast command with response (BCR)                        | Transmit to all cards and receive response from all cards                     |
| Addressing (point-to-point) command (AC)                     | Transmit to addressing card, and there is no data transmission on SDIO_D line |
| Addressing (point-to-point) data transmission command (ADTC) | Transmit to addressing card, and there is data transmission on SDIO_D line    |

#### Command format

All command formats are 48-bit fixed code length, which requires 1.92us (25MHz), 0.96us (50MHz) and 0.92us (52MHz) transmission time.

Table 108 Command Format

| Bit             | 47        | 46               | [45:40]       | [39:8]    | [7:1] | 0       |
|-----------------|-----------|------------------|---------------|-----------|-------|---------|
| Width           | 1         | 1                | 6             | 32        | 7     | 1       |
| Numerical Value | 0         | 1                | -             | -         | -     | 1       |
| Description     | Start Bit | Transmission Bit | Command Index | Parameter | CRC7  | End bit |

SD I/O supports two types of response, both of which support CRC error detection.

- 48-bit short response
- 136-bit long response

Table 109 Short Response Format

| Bit   | 47 | 46 | [45:40] | [39:8] | [7:1] | 0 |
|-------|----|----|---------|--------|-------|---|
| Width | 1  | 1  | 6       | 32     | 7     | 1 |

| Bit             | 47        | 46               | [45:40]       | [39:8]    | [7:1]             | 0       |
|-----------------|-----------|------------------|---------------|-----------|-------------------|---------|
| Numerical Value | 0         | 0                | -             | -         | -                 | 1       |
| Description     | Start Bit | Transmission Bit | Command Index | Parameter | CRC7 or (1111111) | End bit |

Table 110 Long Response Format

| Bit             | 135       | 134              | [133:128] | [127:1]    | 0       |
|-----------------|-----------|------------------|-----------|------------|---------|
| Width           | 1         | 1                | 6         | 127        | 1       |
| Numerical Value | 0         | 0                | 111111    | -          | 1       |
| Description     | Start Bit | Transmission Bit | Reserved  | CID or CSD | End bit |

## Command description

Table 111 Basic Command

| Command Index | Type | Parameter                                        | Response format | Short name            | Description                                                                                                                                   |
|---------------|------|--------------------------------------------------|-----------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| CMD0          | bc   | [31:0] Stuffing bit                              | -               | GO_IDLE_STATE         | Reset all cards to the idle state.                                                                                                            |
| CMD1          | bc   | [31:0]OCR                                        | R3              | SEND_OP_COND          | In the idle state, request the card to transmit the response (including the content of the operating condition register) through the CMD line |
| CMD2          | bcr  | [31:0] Stuffing bit                              | R2              | ALL_SEND_CID          | Request any card to transmit CID data through the CMD line (all cards connected to the master will respond)                                   |
| CMD3          | bcr  | [31:0] Stuffing bit                              | R6              | SEND_RELATIVE_ADDRESS | Request the card to release new relative card address (RCA)                                                                                   |
| CMD4          | bc   | 31:16]DSR<br>[15:0]Stuffing bit                  | -               | SET_DSR               | Set DSR registers of all cards.                                                                                                               |
| CMD5          | bcr  | [31:25]Reserved bit<br>[24]S18R<br>[23:0]I/O OCR | R4              | IO_SEND_OP_COND       | Only apply to I/O card. Query voltage range of all IO cards.                                                                                  |

| Command Index | Type | Parameter                                                                                            | Response format | Short name                   | Description                                                                                                                                                                       |
|---------------|------|------------------------------------------------------------------------------------------------------|-----------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CMD6          | ac   | [31:26]Set to 0<br>[25:24]Access<br>[23:16]Index<br>[15:8]Value<br>[7:3]Set to 0<br>[2:0]Command set | R1b             | SWITCH                       | Only apply to MMC card.<br>Switch the operation mode of the selected card or modify EXT_CSD register.                                                                             |
| CMD7          | ac   | [31:16]RCA<br>[15:0]Stuffing bit                                                                     | R1b             | SELECT/D<br>ESELECT_<br>CARD | Used for switching of the card state.                                                                                                                                             |
| CMD8          | bcr  | [31:12]Reserved bit<br>[11:8]Operating voltage (VHS)<br>[7:0]Inspection mode                         | R7              | SEND_IF_<br>COND             | Transmit interface conditions to SD card, including master power supply voltage information and query whether the card supports the voltage. The reserved bit should be set to 0. |
| CMD9          | ac   | [31:16]RCA<br>[15:0]Stuffing bit                                                                     | R2              | SEND_CS<br>D                 | The selected card transmits to its card specific data (CSD) through CMD                                                                                                           |
| CMD10         | ac   | [31:16]RCA<br>[15:0]Stuffing bit                                                                     | R2              | SEND_CID                     | The selected card transmits to its card identification (CID) through CMD                                                                                                          |
| CMD12         | ac   | [31:0]<br>Stuffing bit                                                                               | R1b             | STOP_TRA<br>NSMISSIO<br>N    | Force the card to stop transmission.                                                                                                                                              |
| CMD13         | ac   | [31:16]RCA<br>[15:0]Stuffing bit                                                                     | R1              | SEND_STA<br>TUS              | The selected card transmits its state register.                                                                                                                                   |
| CMD14         | adtc | [31:0]<br>Stuffing bit                                                                               | R1              | BUSTEST_<br>R                | The master reads the reverse bus test data mode from the card.                                                                                                                    |
| CMD15         | ac   | [31:16]RCA<br>[15:0]Stuffing bit                                                                     | -               | GO_INACTI<br>VE_STATE        | Convert the selected card to inactive state.                                                                                                                                      |

| Command Index | Type | Parameter              | Response format | Short name | Description                                         |
|---------------|------|------------------------|-----------------|------------|-----------------------------------------------------|
| CMD19         | adtc | [31:0]<br>Stuffing bit | R1              | BUSTEST_W  | The master transmits the bus test mode to the card. |

Table 112 Block-oriented Write Command

| Command Index | Type | Parameter                                 | Response format | Short name           | Description                                                                                                                                                                                                                                              |
|---------------|------|-------------------------------------------|-----------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CMD23         | ac   | [31:16]Set to 0<br>[15:0]Number of blocks | R1              | SET_BLOCK_COUNT      | Define the number of blocks to be transferred in subsequent blocks or write commands.                                                                                                                                                                    |
| CMD24         | adtc | [31:0]Data address                        | R1              | WRITE_BLOCK          | Write a block according to the selected length of SET_BLOCKLEN command.                                                                                                                                                                                  |
| CMD25         | adtc | [31:0]Data address                        | R1              | WRITE_MULTIPLE_BLOCK | Continue to write the data block until receiving STOP_TRANSMISSION command or achieving the specified number of blocks.                                                                                                                                  |
| CMD26         | adtc | [31:0] Stuffing bit                       | R1              | PROGAM_CID           | Program the card identification register. This command can be sent to each card once only.<br>The programming involves hardware changes to prevent subsequent operations after the first programming. Reserved to the manufacturer through this command. |
| CMD27         | adtc | [31:0] Stuffing bit                       | R1              | PROGAM_CSD           | Program the programmable bits in the card CSD.                                                                                                                                                                                                           |
| CMD28         | ac   | [31:0]Data address                        | R1b             | SET_WRITE_PROT       | If the card has write protection function, this command will set the write protection bit of the specified group. The write protection characteristic is set in the special data area of the card (WP_GRP_SIZE)                                          |

| Command Index | Type | Parameter                           | Response format | Short name      | Description                                                                                                          |
|---------------|------|-------------------------------------|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------|
| CMD29         | ac   | [31:0]Data address                  | R1b             | CLR_WRITE_PROT  | If the card has write protection function, this command will clear the write protection bit of the addressing group. |
| CMD30         | adtc | [31:0]Write protection data address | R1              | SEND_WRITE_PROT | If the card has write protection function, the command requests the card to transmit write protection bit state.     |

## 25.4.5 Specific Operations

### 25.4.5.1 SD I/O card operations

SD I/O card (including IO card and combined card) supports the following specific operations:

- Read wait operation
- Pause/Recovery operation
- Interrupt

SDIO supports these operations only when setting SDIO\_DCTRL SDIOEN bit; except for read pause, it does not require special hardware operation.

#### SD I/O read wait operation

Read wait (RW) is only used for SD I/O 1-bit and 4-bit modes. Read wait operation allows a master to transmit a signal to stop data transmission when performing the operation of reading multiple blocks for the card, and allows the master to transmit commands to any function in the SD I/O card.

Before receiving the first data block, it is allowed to start the read wait process, enable the data channel (DTEN bit is set to 1), enable SDIO specific operation (SDIOEN bit is set to 1), and start read wait. At the same time, the data are transmitted from the card to the SDIO master, and DPSM will directly enter the read wait state from idle state.

In the read wait state, after 2 SDIO\_CK clock cycles, DPSM drive SDIO\_D2 is 0. In this state, if RWSTOP bit is set, DPSM will stay for 2 more SDIO\_CK clock cycles in the waiting state, and (according to SDIO specification) the drive SDIO\_D2 is 1 in one clock cycle. Then DPSM starts to wait to receive data from the card. When receiving data block, DPSM will not enter the read wait state even if the start wait is set.

SDIO card cannot perform the above read wait operation, SDIO can stop SDIO\_CK entering the read wait and two SDIO\_CK cycles later after receiving the current data block, DPSM stops the clock and recovers the clock after

setting the read wait start bit.

Figure 112 Read Wait Operation Using SDIO\_D2 Signal Line

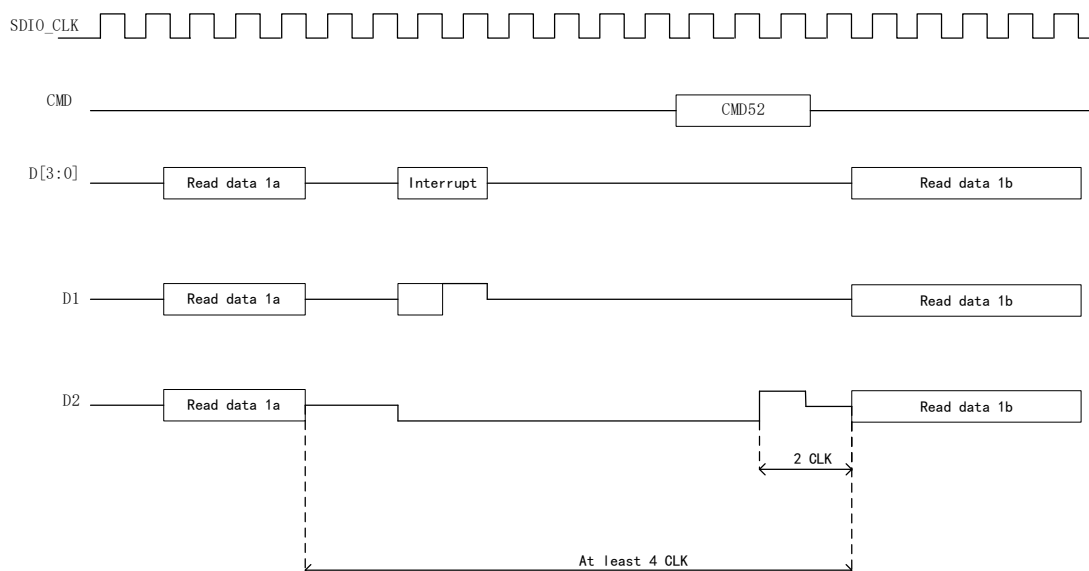
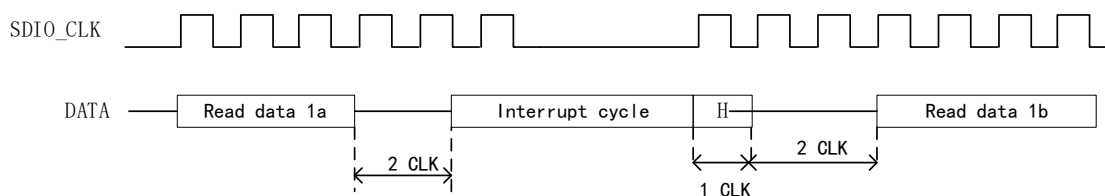


Figure 113 Read Wait Operation through Stop SDIO\_CLK



## SDIO interrupt

When the SDIOEN bit is set, the SDIO master detects SDIO interrupt on SDIO\_D signal line.

### 25.4.5.2 CE-ATA specific operation

CE-ATA device supports the following specific operation:

- Receive command completion signal
- Transmit command completion and closing signal

SDIO supports these operations only when SDIO\_CMD ATACMD bit is set.

## Command completion signal

CE-ATA defines the command completion signal. The device uses this signal to notify the master that the ATA command is completed or encounters an error, and ATA command is terminated.

## Command completion and closing signal



The master can transmit a command to complete the function of closing the signal and canceling the device return command to complete the signal.

If the "Enable CMD end bit" of ATACMD is not set and the "Non-terminal enable bit" of INTDIS is set, the command completion and closing signal will be sent 8-bit cycle later after receiving a short response.

#### 25.4.6 Card state register functional description

The response format R1 contains a 32-bit card state field, which is used to transmit the card state information to the card master (the information may be stored in the local state register). Unless otherwise specified, the state returned by the card is always related to the previous command.

The following table defines different state information:

Table 113 Different State Information Types

| Abbreviation | Definition                                                                                                                                                 |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E            | Error bit                                                                                                                                                  |
| S            | State bit                                                                                                                                                  |
| R            | Detection bit, set according to the actual command response                                                                                                |
| X            | Detection bit, set during the execution of command. The master of SDIO card reads these bits and queries the card state by transmitting the state command. |

Table 114 Clear Conditions

| Abbreviation | Definition                                                                                                       |
|--------------|------------------------------------------------------------------------------------------------------------------|
| A            | According to current state of the card                                                                           |
| B            | Always related to previous command. Can be cleared once correct command is received (with delay of one command). |
| C            | Clear once read                                                                                                  |

Table 115 Card State

| Bit | Name                                             | Type | Numerical Value            | Description                                                                                | Clear conditions |
|-----|--------------------------------------------------|------|----------------------------|--------------------------------------------------------------------------------------------|------------------|
| 1:0 | Reserved for the test mode of the manufacturer.  |      |                            |                                                                                            |                  |
| 2   | Reserved for the command related to application. |      |                            |                                                                                            |                  |
| 3   | AKE_SEQ_ERROR                                    | ER   | 0=No error<br>1=Error      | Verification sequence error.                                                               | C                |
| 4   | Reserved for SD I/O card                         |      |                            |                                                                                            |                  |
| 5   | APP_CMD                                          | SR   | 0=Not allowed<br>1=Allowed | The card expects ACMD, or the instruction command has been interpreted as an ACMD command. | C                |
| 6   | Reserved                                         |      |                            |                                                                                            |                  |

| Bit  | Name              | Type | Numerical Value                                                                                                                                 | Description                                                                                                                                                                                                                                         | Clear conditions |
|------|-------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| 7    | SWITCH_ERROR      | EX   | 0=No error<br>1=Conversion error                                                                                                                | The card is not switched to the desired mode according to the requirements of SWITCH command.                                                                                                                                                       | B                |
| 8    | READY_FOR_DATA    | SR   | 0=Not ready<br>1=Ready                                                                                                                          | Corresponding to the empty signal of the buffer on the bus.                                                                                                                                                                                         |                  |
| 12:9 | CURRENT_STATE     | SR   | 0=Idle<br>1=Ready<br>2=Identify<br>3=Standby<br>4=Transmit<br>5=Data<br>6=Receive<br>7=Program<br>8=Disconnect<br>9=Busy test<br>10~15=Reserved | The state of the state machine in the card when receiving a command. If the execution of a command causes a state change, the change will be reflected in the response of next command. These four bits are interpreted by decimal numbers 0 to 15. | B                |
| 13   | ERASE_RESET       |      | 0=Clear<br>1=Set                                                                                                                                | Because a command other than the erase sequence (rather than CMD35, CMD36, CMD38 or CMD13 command) is received, the sequence of entering the erase process is aborted.                                                                              | C                |
| 14   | CARD_ECC_DISABLED | SX   | 0=Allowed<br>1=Not allowed                                                                                                                      | Internal ECC is not used during execution of the command.                                                                                                                                                                                           | A                |
| 15   | WP_ERASE_SKIP     | EX   | 0=Not protected<br>1=Protected                                                                                                                  | Encounter existing write protection data block, and only part of address space is erased.                                                                                                                                                           | C                |

| Bit | Name               | Type | Numerical Value                  | Description                                                                                                                                                                                                                                                                                                      | Clear conditions |
|-----|--------------------|------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| 16  | CID/CSD_OVERWRITE  | EX   | 0=No error<br>1=Error            | <p>It can be any of the following errors:</p> <p>It has been written into the CID register and cannot be overridden</p> <p>The read-only part of the CSD does not match the content of the card</p> <p>Attempt to reverse copy or permanent write protection, i.e., restore or release the write protection.</p> | C                |
| 17  | Reserved           |      |                                  |                                                                                                                                                                                                                                                                                                                  |                  |
| 18  | Reserved           |      |                                  |                                                                                                                                                                                                                                                                                                                  |                  |
| 19  | ERROR              | EX   | 0=No error<br>1=Error            | <p>Generate an error related to the previous master command executed (not defined in the standard)</p> <p>Error inside the card (such as read or write error).</p>                                                                                                                                               | C                |
| 20  | CC_ERROR           | ER   | 0=No error<br>1=Error            | Error inside the card (not defined in the standard), which has nothing to do with the command of the master.                                                                                                                                                                                                     | C                |
| 21  | CARD_ECC_FAILED    | EX   | 0=Succeeded<br>1=Failed          | ECC check is implemented in the card, but it fails when correcting the data.                                                                                                                                                                                                                                     | C                |
| 22  | ILLEGAL_COMMAND    | ER   | 0=No error<br>1=Error            | The command is illegal for current card state.                                                                                                                                                                                                                                                                   | B                |
| 23  | COM_CRC_ERROR      | ER   | 0=No error<br>1=Error            | CRC parity error in previous command.                                                                                                                                                                                                                                                                            | B                |
| 24  | LOCK_UNLOCK_FAILED | EX   | 0=No error<br>1=Error            | Sequence error of command or wrong password detected in lock/unlock.                                                                                                                                                                                                                                             | C                |
| 25  | CARD_IS_LOCKED     | SR   | 0=Card unlocked<br>1=Card locked | When this bit is set, it means the card has been locked.                                                                                                                                                                                                                                                         | A                |
| 26  | WP_VIOLATION       | EX   | 0=No error<br>1=Error            | Attempt to program the data block of a write protection.                                                                                                                                                                                                                                                         | C                |

| Bit | Name                 | Type | Numerical Value       | Description                                                                                                                                                                                                                                                                                                                                                          | Clear conditions |
|-----|----------------------|------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| 27  | ERASE_PARAM          | EX   | 0=No error<br>1=Error | Illegal erase group selected when erasing.                                                                                                                                                                                                                                                                                                                           | C                |
| 28  | ERASE_SEQ_ERROR      |      | 0=No error<br>1=Error | The sequence of transmitting erase command is wrong.                                                                                                                                                                                                                                                                                                                 | C                |
| 29  | BLOCK_LEN_ERROR      |      | 0=No error<br>1=Error | The parameters of SET_BLOCKLEN command exceed the maximum allowable range of the card, or the previously defined data block length is illegal for the current command (for example, the master transmits a write command, and the current block length is less than the minimum allowable length of the card, while some data blocks are not allowed to be written). | C                |
| 30  | ADDRESS_MISALIGN     |      | 0=No error<br>1=Error | The first block defined by the address parameter in the command (compared with the current block length) is not aligned with the physical block of the card.<br><br>A multi-data block or data stream read/write operation (even starting from a legal address) attempts to read or write a data block that is not aligned with the physical block.                  | C                |
| 31  | ADDRESS_OUT_OF_RANGE | ERX  | 0=No error<br>1=Error | The address parameter in the command is beyond the allowed range of the card.<br><br>A multi-data block or data stream read/write operation (even starting from a legal address) attempts to read or write the part beyond the capacity of the card.                                                                                                                 | C                |

### 25.4.6.1 SD state register functional description

The SD state includes the state bits related to the specific functions of the SD memory card and some state bits related to future applications. The length of the SD state is a 512-bit data block. After receiving the ACMD13 command (CMD55, then CMD13), the content of this register will be transmitted to the SDIO card host. The ACMD13 command can be sent only when the card is in transmission state (the card has been selected).

The following table defines different SD state register information.

Table 116 SD State Register Information

| Abbreviation | Definition                                                                                                                                                 |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E            | Error bit                                                                                                                                                  |
| S            | State bit                                                                                                                                                  |
| R            | Detection bit, set according to the actual command response                                                                                                |
| X            | Detection bit, set during the execution of command. The master of SDIO card reads these bits and queries the card state by transmitting the state command. |

Note: For the abbreviations and definitions of related types and clear condition fields in the table, see.

Table 117 Clear Conditions

| Abbreviation | Definition                                                                                                       |
|--------------|------------------------------------------------------------------------------------------------------------------|
| A            | According to current state of the card                                                                           |
| B            | Always related to previous command. Can be cleared once correct command is received (with delay of one command). |
| C            | Clear once read                                                                                                  |

Table 118 SD State

| Bit     | Name                         | Type | Numerical Value                                                | Description                  | Clear conditions |
|---------|------------------------------|------|----------------------------------------------------------------|------------------------------|------------------|
| 311:0   | Reserved to the manufacturer |      |                                                                |                              |                  |
| 399:312 | Reserved                     |      |                                                                |                              |                  |
| 401:400 | ERASE_OFF SET                | -    | -                                                              | -                            | -                |
| 407:402 | ERASE_TIME OUT               | S R  | Fixed offset value added in erase                              | (See the instructions below) | A                |
| 423:408 | ERASE_SIZE                   | S R  | Erase the timeout value of specified range of UNIT_OF_ERASE_AU | (See the instructions below) | A                |
| 427:424 | Reserved                     | S R  | The number of AU that can be erased at a time                  | (See the instructions below) | A                |

| Bit     | Name                   | Type | Numerical Value                                                                                                                                                                  | Description                                                                                                                                                                                                                                                         | Clear conditions |
|---------|------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| 431:428 | AU_SIZE                | S R  | AU size (see the instructions below)                                                                                                                                             | (See the instructions below)                                                                                                                                                                                                                                        | A                |
| 439:432 | PERFORMANCE_MOVE       | S R  | Transmission performance in 1MB/s (see the instructions below)                                                                                                                   | (See the instructions below)                                                                                                                                                                                                                                        | A                |
| 447:440 | SPEED_CLASS            | S R  | Speed type of the card (see the instructions below)                                                                                                                              | (See the instructions below)                                                                                                                                                                                                                                        | A                |
| 479:448 | SIZE_OF_PROTECTED_AREA | S R  | Size of protected area (see the instructions below)                                                                                                                              | (See the instructions below)                                                                                                                                                                                                                                        | A                |
| 495:480 | SD_CARD_TYPE           | S R  | '00xxh'= SD memory card in physical specification version 1.01~2.00 ('x' means any value). The defined cards are:<br>'0000'= Universal SD read-write card<br>'0001'= SD ROM card | The low 8 bits of this field can define different variants of SD memory card in the future (each bit can be used to define different SD types). The high 8 bits can be used to define SD cards that do not comply with the current SD physical layer specification. | A                |
| 508:496 | Reserved               |      |                                                                                                                                                                                  |                                                                                                                                                                                                                                                                     |                  |
| 509     | SECURED_MODE           | S R  | 0=Not in the secret mode<br>1=In the secret mode                                                                                                                                 | The card is in secret operation mode (see "SD Confidentiality Specification").                                                                                                                                                                                      | A                |
| 511:510 | DAT_BUS_WIDTH          | S R  | 00=1 (default)<br>01-Reserve<br>10=4-bit width<br>11=Reserved                                                                                                                    | Current data bus width defined by SET_BUS_WIDTH command.                                                                                                                                                                                                            | A                |

### SIZE\_OF\_PROTECTED\_AREA

The way of setting this bit is different between standard-capacity card and high-capacity card:

- For the standard-capacity card, the capacity of the protected area is calculated as follows:  
Protected area=SIZE\_OF\_PROTECTED\_AREA \* MULT \* BLOCK\_LEN  
The unit of SIZE\_OF\_PROTECTED\_AREA is MULT \* BLOCK\_LEN.
- For the high-capacity card, the capacity of the protected area is calculated as follows:  
Protected area=SIZE\_OF\_PROTECTED\_AREA  
The unit of SIZE\_OF\_PROTECTED\_AREA is byte.

## SPEED\_CLASS

These 8 bits indicate the type of speed and can be used for calculating the value of PW/2 (PW is the performance of write).

Table 119 Speed Type Code

| SPEED_CLASS | Definition of Numerical Value |
|-------------|-------------------------------|
| 00h         | Type 0                        |
| 01h         | Type 2                        |
| 02h         | Type 4                        |
| 03h         | Type 6                        |
| 04h~FFh     | Reserved                      |

## PERFORMANCE\_MOVE

These 8 bits indicate mobility performance (Pm) in 1MB/s. If the card does not use RU (record unit) mobile data, it should be considered that Pm is infinitely great. Setting this field for FFh means infinitely great.

Table 120 Mobility Performance Code

| PERFORMANCE_MOVE | Definition of Numerical Value |
|------------------|-------------------------------|
| 00h              | Undefined                     |
| 01h              | 1MB/s                         |
| 02h              | 2MB/s                         |
| .....            | .....                         |
| Feh              | 254MB/s                       |
| FFh              | Infinitely great              |

## AU\_SIZE

These four bits indicate the length of AU, and the value is the multiple of the power of 2 in 16KB.

Table 121 AU\_SIZE Codes

| AU_SIZE | Definition of Numerical Value |
|---------|-------------------------------|
| 00h     | Undefined                     |
| 01h     | 16KB                          |
| 02h     | 32KB                          |
| 03h     | 64KB                          |
| 04h     | 128KB                         |
| 05h     | 256KB                         |
| 06h     | 512KB                         |
| 07h     | 1MB                           |
| 08h     | 2MB                           |
| 09h     | 4MB                           |
| Ah~Fh   | Reserved                      |

According to the capacity of the card, the maximum AU length is defined by the following table. The card can set any AU length between the RU length and the maximum AU length.

Table 122 Maximum AU Length

| Capacity    | Maximum AU length |
|-------------|-------------------|
| 16MB~64MB   | 512KB             |
| 128MB~256MB | 1MB               |
| 512MB       | 2MB               |
| 1GB~32GB    | 4MB               |

## ERASE\_SIZE

This 16-bit field gives the value of NERASE, and when MERASE number of AU is erased, ERASE\_TIMEOUT defines the timeout period.

If the master can determine the value of NERASE in a certain erase, the erase progress can be displayed.

Table 123 ERASE\_SIZE Codes

| ERASE_SIZE | Definition of Numerical Value             |
|------------|-------------------------------------------|
| 0000h      | Overtime calculation not supporting erase |
| 0001h      | One AU                                    |
| 0002h      | Two AUs                                   |
| 0003h      | Three AUs                                 |
| .....      | .....                                     |



| ERASE_SIZE | Definition of Numerical Value |
|------------|-------------------------------|
| FFFFh      | 65535 AUs                     |

## ERASE\_TIMEOUT

These 6 bits give TERASE. When multiple AUs are erased, TERASE gives the erase timeout calculated from offset.

Table 124 Erase Timeout Codes

| ERASE_TIMEOUT | Definition of Numerical Value             |
|---------------|-------------------------------------------|
| 00            | Overtime calculation not supporting erase |
| 01            | 1 second                                  |
| 02            | 2 seconds                                 |
| 03            | 3 seconds                                 |
| .....         | .....                                     |
| 63            | 63 seconds                                |

## ERASE\_OFFSET

These two bits give TOFFSET, and when both ERASE\_SIZE and ERASE\_TIMEOUT are 0, this value is meaningless.

Table 125 Erase Offset Codes

| ERASE_OFFSET | Definition of Numerical Value |
|--------------|-------------------------------|
| 0            | 0 second                      |
| 1            | 1 second                      |
| 2            | 2 seconds                     |
| 3            | 3 seconds                     |

## 25.5 Register address mapping

Table 126 SDIO Register Address Mapping

| Register name | Description                    | Offset address                         |
|---------------|--------------------------------|----------------------------------------|
| SDIO_PWRCTRL  | SDIO power control register    | 0x00                                   |
| SDIO_CLKCTRL  | SDIO clock control register    | 0x04                                   |
| SDIO_ARG      | SDIO parameter register        | 0x08                                   |
| SDIO_CMD      | SDIO command register          | 0x0C                                   |
| SDIO_CMDRES   | SDIO command response register | 0x10                                   |
| SDIO_RESx     | SDIO response x register       | $0x14 + 4 * (x-1)$ , wherein $x=1...4$ |

| Register name | Description                   | Offset address |
|---------------|-------------------------------|----------------|
| SDIO_DATATIME | SDIO data timer register      | 0x24           |
| SDIO_DATALEN  | SDIO data length register     | 0x28           |
| SDIO_DCTRL    | SDIO data control register    | 0x2C           |
| SDIO_DCNT     | SDIO data counter register    | 0x30           |
| SDIO_STS      | SDIO state register           | 0x34           |
| SDIO_ICF      | SDIO clear interrupt register | 0x38           |
| SDIO_MASK     | SDIO interrupt mask register  | 0x3C           |
| SDIO_FIFOCNT  | SDIO counter register         | 0x48           |
| SDIO_FIFODATA | SDIO data FIFO register       | 0x80           |

## 25.6 Register functional description

The device communicates with the system through the 32-bit control registers that can be operated on APB2. These peripheral registers must be operated in word (32-bit) mode.

### 25.6.1 SDIO power control register (SDIO\_PWRCTRL)

Offset address: 0x00

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                            |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | PWRCTRL  | R/W | Power Supply Control<br>Select current function state of card clock.<br>00: Power off, card clock stopped.<br>01: Reserved.<br>10: Reserved power-on state.<br>11: Power-on state, card clock started. |
| 31:2  | Reserved |     |                                                                                                                                                                                                        |

Note: This register cannot be written within 3 SDIOCLK (48 MHz) clock cycles and 2 PCLK2 clock cycles after writing data.

### 25.6.2 SDIO clock control register (SDIO\_CLKCTRL)

Offset address: 0x04

Reset value: 0x0000 0000

SDIO\_CLKCTRL register controls SDIO\_CLK to output the clock.

| Field | Name   | R/W | Description                                                                                                                                                                    |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | CLKDIV | R/W | Clock Divide Factor<br>This domain defines the division factor between input clock (SDIOCLK) and output clock (SDIO_CLK):<br>$SDIO\_CLK\ frequency = SDIOCLK / [CLKDIV + 2]$ . |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                          |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8     | CLKEN    | R/W | Clock Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                              |
| 9     | PWRSAPV  | R/W | Power Saving Mode Configuration<br>Reduce power consumption by disabling SDIO_ CLK outputs beyond the bus activity.<br>0: Enable<br>1: Disable                                                                                                       |
| 10    | BYPASSEN | R/W | Clock Divider Bypass Enable<br>Before driving SDIO_CLK to output signals, it is required to divide the frequency of SDIOCLK; however, if the divider is bypassed, SDIOCLK will directly drive SDIO_CLK to output signals.<br>0: Disable<br>1: Enable |
| 12:11 | WBSEL    | R/W | Wide Bus Mode Select<br>Select bus mode for different bits, corresponding to different SDIO_D bits.<br>00: Default, using SDIO_D0<br>01: 4 bits, using SDIO_D[3:0]<br>10: 8 bits, using SDIO_D[7:0]<br>11: Reserved                                  |
| 13    | DEPSEL   | R/W | SDIO_CLK Dephasing Select<br>Select SDIOCLK rising edge or falling edge to generate SDIO_CLK.<br>0: Rising edge<br>1: Falling edge                                                                                                                   |
| 14    | HFCEN    | R/W | HW Flow Control Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                    |
| 31:15 | Reserved |     |                                                                                                                                                                                                                                                      |

Note:

- (1) When SD/SD I/O card or multimedia card is in identification mode, the frequency of SDIO\_CLK must be less than 400kHz.
- (2) When all cards have been assigned the corresponding address, the clock frequency can be changed to the maximum frequency allowed by the card bus.
- (3) This register cannot be written within 3 SDIOCLK (48 MHz) clock cycles and 2 PCLK2 clock cycles after writing data. For SD I/O card, SDIO\_CLK can be stopped during read wait period, and then SDIO\_CLKCTRL register does not control SDIO\_CLK.

### 25.6.3 SDIO parameter register (SDIO\_ARG)

Offset address: 0x08

Reset value: 0x0000 0000

Command parameters are also part of the command, and SDIO\_ARG register contains 32-bit command parameters and is sent to the card together with the command.

| Field | Name   | R/W | Description                                       |
|-------|--------|-----|---------------------------------------------------|
| 31:0  | CMDARG | R/W | Command Argument<br>Store the command parameters. |

#### 25.6.4 SDIO command register (SDIO\_CMD)

Offset address: 0x0C

Reset value: 0x0000 0000

SDIO\_CMD register contains command index and command type bit.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0   | CMDINDEX | R/W | Command Index<br>The command index, as part of the command, is transmitted to the card together with the command.                                                                                                                                                                                                                                                  |
| 7:6   | WAITRES  | R/W | Wait for Response<br>Indicate whether CPSM needs to wait for the response, and if it needs to wait for the response, the response type will be indicated.<br>00: No response, expecting CMDSENT flag<br>01: Short response, expecting CMDREND or CCRCFAIL flag<br>10: No response, expecting CMDSENT flag<br>11: Long response, expecting CMDREND or CCRCFAIL flag |
| 8     | WAITINT  | R/W | CPSM Waits for Interrupt Request<br>CPSM enables or disables the command timeout control and waits for interrupt request.<br>0: Enable<br>1: Disable                                                                                                                                                                                                               |
| 9     | WENDDATA | R/W | CPSM Waits for Ends of Data Transfer (CmdPend Internal Signal)<br>0: Invalid<br>1: CPSM waits for the end of data transmission before starting to transmit a command.                                                                                                                                                                                              |
| 10    | CPSMEN   | R/W | Command Path State Machine (CPSM) Enable<br>Enable CPSM.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                |
| 11    | SDIOSC   | R/W | SD I/O Suspend Command<br>0: Invalid<br>1: The command to be sent is a suspend command (only used for SD I/O card).                                                                                                                                                                                                                                                |
| 12    | CMDCPEN  | R/W | Enable CMD Completion<br>Enable command completion signal.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                              |
| 13    | INTEN    | R/W | Interrupt Enable<br>0: Enable<br>1: Disable                                                                                                                                                                                                                                                                                                                        |
| 14    | ATACMD   | R/W | CE-ATA Command<br>0: Invalid<br>1: Switch CPSM to CMD61                                                                                                                                                                                                                                                                                                            |

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 31:15 | Reserved |     |             |

Note:

- (1) This register cannot be written within 3 SDIOCLK (48 MHz) clock cycles and 2 PCLK2 clock cycles after writing data.
- (2) The multimedia card can transmit two kinds of responses: 48-bit short response or 136-bit long response. The SD card and SD I/O card can only transmit short response, parameters can be changed according to the type of response, and the software will distinguish the type of response according to the command sent. CE-ATA devices only transmit short responses.

### 25.6.5 SDIO command response register (SDIO\_CMDRES)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                 |
|-------|----------|-----|---------------------------------------------------------------------------------------------|
| 5:0   | CMDRES   | R   | Response Command Index<br>Store the command index in the finally received command response. |
| 31:6  | Reserved |     |                                                                                             |

### 25.6.6 SDIO response x register (SDIO\_RESx)

Offset address:  $0x14 + 4 * (x-1)$ , wherein  $x=1...4$

Reset value: 0x0000 0000

SDIO\_RES1/2/3/4 register contains the card state, which is information about the received response.

| Field | Name     | R/W | Description          |
|-------|----------|-----|----------------------|
| 31:0  | CARDSTSx | R   | See the table below. |

The state length of the card is 32 bits or 127 bits based on the response state.

Table 127 Response Type and SDIO\_RESPx Register

| Register  | Short response    | Long response       |
|-----------|-------------------|---------------------|
| SDIO_RES1 | Card state [31:0] | Card state [127:96] |
| SDIO_RES2 | Unused            | Card state [95:64]  |
| SDIO_RES3 | Unused            | Card state [63:32]  |
| SDIO_RES4 | Unused            | Card state [31:1]   |

Always receive the most significant bit of card state first, and the lowest bit of SDIO\_RES3 register is always 0.

### 25.6.7 SDIO data timer register (SDIO\_DATATIME)

Offset address: 0x24

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                    |
|-------|----------|-----|--------------------------------------------------------------------------------|
| 31:0  | DATETIME | R/W | Data Timeout Period<br>Record the data timeout period in card bus clock cycle. |

Note: Before writing the data control register for data transmission, first write the data timer register and data length register.

### 25.6.8 SDIO data length register (SDIO\_DATALEN)

Offset address: 0x28

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                           |
|-------|----------|-----|-------------------------------------------------------|
| 24:0  | DATALEN  | R/W | Data Length<br>Byte length of data to be transmitted. |
| 31:25 | Reserved |     |                                                       |

Note: For block data transfer, the value in SDIO\_DATALEN must be a multiple of the data block length.  
Before writing SDIO\_DCTRL for data transmission, first write SDIO\_DATETIME and SDIO\_DATALEN.

### 25.6.9 SDIO data control register (SDIO\_DCTRL)

Offset address: 0x2C

Reset value: 0x0000 0000

SDIO\_DCTRL register control data channel state channel (DPSM).

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|---------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | DTEN    | R/W | Data Transfer Enabled<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                   |
| 1     | DTDRCFG | R/W | Data Transfer Direction Configuration<br>0: From controller to card<br>1: From card to controller                                                                                                                                                                                                                                                                                                  |
| 2     | DTSEL   | R/W | Data Transfer Mode Select<br>0: Block data transfer<br>1: Stream data transfer                                                                                                                                                                                                                                                                                                                     |
| 3     | DMAEN   | R/W | DMA Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                              |
| 7:4   | DBSIZE  | R/W | Data Block Size<br>Define the data block length:<br>0000: Block length=20=1 byte<br>0001: Block length=21=2 bytes<br>0010: Block length=22=4 bytes<br>0011: Block length=23=8 bytes<br>0100: Block length=24=16 bytes<br>0101: Block length=25=32 bytes<br>0110: Block length=26=64 bytes<br>0111: Block length=27=128 bytes<br>1000: Block length=28=256 bytes<br>1001: Block length=29=512 bytes |

| Field | Name     | R/W | Description                                                                                                                                                                                              |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 1010: Block length=210=1024 bytes<br>1011: Block length=211=2048 bytes<br>1100: Block length=212=4096 bytes<br>1101: Block length=213=8192 bytes<br>1110: Block length=214=16384 bytes<br>1111: Reserved |
| 8     | RWSTR    | R/W | Read Wait Start<br>0: Invalid<br>1: Start read wait operation                                                                                                                                            |
| 9     | RWSTOP   | R/W | Read Wait Stop Enable<br>If RWSTR is set, stop read operation can be enabled.<br>0: Disable<br>1: Enable                                                                                                 |
| 10    | RDWAIT   | R/W | Read Wait Mode<br>0: Control to stop SDIO_D2<br>1: Control to use SDIO_CK                                                                                                                                |
| 11    | SDIOF    | R/W | SD I/O Enable Functions<br>If this bit is set, DPSM will execute specific operation of SD I/O card.                                                                                                      |
| 31:12 | Reserved |     |                                                                                                                                                                                                          |

#### 25.6.10 SDIO data counter register (SDIO\_DCNT)

Offset address: 0x30

Reset value: 0x0000 0000

When DPSM enters Wait\_R or Wait\_S state from the idle state, SDIO\_DCNT loads values from SDIO\_DATALEN, and in the data transmission process, the counter will count down to 0, and then DPSM will enter the idle state and set DATAEND flag.

| Field | Name     | R/W | Description                                                            |
|-------|----------|-----|------------------------------------------------------------------------|
| 24:0  | DATA CNT | R   | Data Count Number<br>Store the number of data bytes to be transmitted. |
| 31:25 | Reserved |     |                                                                        |

Note: This register can be read only by the end of data transmission.

#### 25.6.11 SDIO state register (SDIO\_STS)

Offset address: 0x34

Reset value: 0x0000 0000

SDIO\_STS is a read-only register, and it contains two kinds of flags:

(1) Static flag (bit [23:22, 10:0]): Write SDIO interrupt clear register to clear these bits.

(2) Dynamic flag (bits [21:11]): The state of these bits changes according to the logic of corresponding part.

| Field | Name    | R/W | Description                                       |
|-------|---------|-----|---------------------------------------------------|
| 0     | COMRESP | R   | Command Response Received (CRC detection failure) |

| Field | Name     | R/W | Description                                                                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------|
| 1     | DBDR     | R   | Data Block Sent/Received (CRC detection failure)                                                                                       |
| 2     | CMDRESTO | R   | Command Response Timeout<br>Command timeout period is 64 SDIO_CLK clock cycles.                                                        |
| 3     | DATATO   | R   | Data Timeout                                                                                                                           |
| 4     | TXUDRER  | R   | Transmit FIFO Underrun Error                                                                                                           |
| 5     | RXOVRER  | R   | Received FIFO Overrun Error                                                                                                            |
| 6     | CMDRES   | R   | Command Response (CRC detection succeeded)                                                                                             |
| 7     | CMDSENT  | R   | Command Sent (No Response Required)                                                                                                    |
| 8     | DATAEND  | R   | Data end (data counter, SDIO_DCNT=0)                                                                                                   |
| 9     | SBE      | R   | Start Bit Not Detected on All Data Signals in Wide Bus Mode                                                                            |
| 10    | DBCP     | R   | Data Block Sent/Received                                                                                                               |
| 11    | CMDACT   | R   | Command Transfer in Progress                                                                                                           |
| 12    | TXACT    | R   | Data Transmit in Progress                                                                                                              |
| 13    | RXACT    | R   | Data Receive in Progress                                                                                                               |
| 14    | TXFHF    | R   | Transmit FIFO Half Empty:<br>At least 8 more words can be written in FIFO.                                                             |
| 15    | RXFHF    | R   | Receive FIFO Half Full<br>There are at least eight words in FIFO.                                                                      |
| 16    | TXFF     | R   | Transmit FIFO Full                                                                                                                     |
| 17    | RXFF     | R   | Receive FIFO Full<br>If the hardware flow control is used, the RXFF signal will become effective when the FIFO is still 2 words short. |
| 18    | TXFE     | R   | Transmit FIFO Empty<br>If the hardware flow control is used, the TXFE signal will become effective when the FIFO contains 2 words.     |
| 19    | RXFE     | R   | Receive FIFO Empty                                                                                                                     |
| 20    | TXDA     | R   | Data Available in Transmit FIFO                                                                                                        |
| 21    | RXDA     | R   | Data Available in Receive FIFO                                                                                                         |
| 22    | SDIOINT  | R   | SDIO Interrupt Received                                                                                                                |
| 23    | ATAEND   | R   | CE-ATA Command Completion Signal Received for CMD61                                                                                    |
| 31:24 | Reserved |     |                                                                                                                                        |

### 25.6.12 SDIO clear interrupt register (SDIO\_ICF)

Offset address: 0x38

Reset value: 0x0000 0000

SDIO\_ICF is a write-only register, and setting the corresponding bits will clear the bits in SDIO\_STS state register.



| Field | Name     | R/W | Description                                                           |
|-------|----------|-----|-----------------------------------------------------------------------|
| 0     | CRCE     | R/W | COMRESP Flag Clear<br>Clear COMRESP flag.<br>0: Invalid<br>1: Clear   |
| 1     | DBCE     | R/W | DBDR Flag Clear<br>Clear DBDR flag.<br>0: Invalid<br>1: Clear         |
| 2     | CRT0     | R/W | CMDRESTO Flag Clear<br>Clear CMDRESTO flag.<br>0: Invalid<br>1: Clear |
| 3     | DTO      | R/W | DATATO Flag Clear<br>Clear DATATO flag.<br>0: Invalid<br>1: Clear     |
| 4     | TXFUE    | R/W | TXUDRER Flag Clear<br>Clear TXUDRER flag.<br>0: Invalid<br>1: Clear   |
| 5     | RXFOE    | R/W | RXOVRER Flag Clear<br>Clear RXOVRER flag.<br>0: Invalid<br>1: Clear   |
| 6     | CMDRES   | R/W | CMDRES Flag Clear<br>Clear CMDRES flag.<br>0: Invalid<br>1: Clear     |
| 7     | CMDSENT  | R/W | CMDSENT Flag Clear<br>Clear CMDSENT flag.<br>0: Invalid<br>1: Clear   |
| 8     | DATAEND  | R/W | DATAEND Flag clear<br>Clear DATAEND flag.<br>0: Invalid<br>1: Clear   |
| 9     | SBE      | R/W | SBE Flag Clear<br>Clear SBE flag.<br>0: Invalid<br>1: Clear           |
| 10    | DBCP     | R/W | DBCP Flag Clear<br>Clear DBCP flag.<br>0: Invalid<br>1: Clear         |
| 21:11 | Reserved |     |                                                                       |

| Field | Name     | R/W | Description                                                           |
|-------|----------|-----|-----------------------------------------------------------------------|
| 22    | SDIOIT   | R/W | SDIOIT flag clear bit<br>Clear SDIOIT flag.<br>0: Invalid<br>1: Clear |
| 23    | ATAEND   | R/W | ATAEND flag clear bit<br>Clear ATAEND flag.<br>0: Invalid<br>1: Clear |
| 31:24 | Reserved |     |                                                                       |

### 25.6.13 SDIO interrupt mask register (SDIO\_MASK)

Offset address: 0x3C

Reset value: 0x0000 0000

Set or cleared by software.

When the corresponding bit is set to 1, SDIO\_MASK interrupt mask register decides which state bit generates an interrupt.

| Field | Name     | R/W | Description                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 0     | CCRCFAIL | R/W | Command CRC Fail Interrupt Enable<br>Enable/Disable command block CRC detection failure interrupt.<br>0: Disable<br>1: Enable |
| 1     | DCRCFAIL | R/W | Data CRC Fail Interrupt Enable<br>Enable/Disable data block CRC detection failure interrupt.<br>0: Disable<br>1: Enable       |
| 2     | CMDTO    | R/W | Command Timeout Interrupt Enable<br>Enable/Disable command timeout interrupt.<br>0: Disable<br>1: Enable                      |
| 3     | DATATO   | R/W | Data timeout interrupt enable<br>Enable/Disable data timeout interrupt.<br>0: Disable<br>1: Enable                            |
| 4     | TXURER   | R/W | Tx FIFO Underrun Error Interrupt Enable<br>Enable/Disable transmit FIFO underrun error interrupt.<br>0: Disable<br>1: Enable  |
| 5     | RXORER   | R/W | Rx FIFO Overrun Error Interrupt Enable<br>Enable/Disable receive FIFO overrun error interrupt.<br>0: Disable<br>1: Enable     |
| 6     | CMDRESRC | R/W | Command Response Received Interrupt Enable<br>Enable/Disable receiving response interrupt.<br>0: Disable<br>1: Enable         |

| Field | Name    | R/W | Description                                                                                                                                    |
|-------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------|
| 7     | CMDSENT | R/W | Command Sent Interrupt Enable<br>Enable/Disable command sent interrupt since the software has set/cleared this bit.<br>0: Disable<br>1: Enable |
| 8     | DATAEND | R/W | Data End Interrupt Enable<br>Enable/Disable data transmission end interrupt.<br>0: Disable<br>1: Enable                                        |
| 9     | STRTER  | R/W | Start Bit Error Interrupt Enable<br>Enable/Disable start bit error interrupt.<br>0: Disable<br>1: Enable                                       |
| 10    | DBEND   | R/W | Data Block End Interrupt Enable<br>Enable/Disable data block transmission end interrupt.<br>0: Disable<br>1: Enable                            |
| 11    | CMDACT  | R/W | Command Acting Interrupt Enable<br>Enable/Disable transmitting command interrupt.<br>0: Disable<br>1: Enable                                   |
| 12    | TXACT   | R/W | Data Transmit Acting Interrupt Enable<br>Enable/Disable transmitting data interrupt.<br>0: Disable<br>1: Enable                                |
| 13    | RXACT   | R/W | Data receive acting interrupt enable<br>Enable/Disable receiving data interrupt.<br>0: Disable<br>1: Enable                                    |
| 14    | TXHFERT | R/W | Tx FIFO Half Empty Interrupt Enable<br>Enable/Disable transmit FIFO half empty interrupt.<br>0: Disable<br>1: Enable                           |
| 15    | RXHFFUL | R/W | Rx FIFO Half Full Interrupt Enable<br>Enable/Disable receive FIFO half full interrupt.<br>0: Disable<br>1: Enable                              |
| 16    | TXFUL   | R/W | Tx FIFO Full Interrupt Enable<br>Enable/Disable transmit FIFO full interrupt.<br>0: Disable<br>1: Enable                                       |
| 17    | RXFUL   | R/W | Rx FIFO Full Interrupt Enable<br>Enable/Disable receive FIFO full interrupt.<br>0: Disable<br>1: Enable                                        |

| Field | Name       | R/W | Description                                                                                                                                                   |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18    | TXEPT      | R/W | Tx FIFO Empty Interrupt Enable<br>Enable/Disable transmit FIFO empty interrupt.<br>0: Disable<br>1: Enable                                                    |
| 19    | RXFEIE     | R/W | Rx FIFO Empty Interrupt Enable<br>Enable/Disable receive FIFO empty interrupt.<br>0: Disable<br>1: Enable                                                     |
| 20    | TXDAVB     | R/W | Data Available in Tx FIFO Interrupt Enable<br>Enable/Disable transmit FIFO data available interrupt.<br>0: Disable<br>1: Enable                               |
| 21    | RXDAVB     | R/W | Data Available in Rx FIFO Interrupt Enable<br>Enable/Disable receive FIFO data available interrupt.<br>0: Disable<br>1: Enable                                |
| 22    | SDIOINTREC | R/W | SDIO Mode Interrupt Received Interrupt Enable<br>Enable/Disable SDIO mode interrupt received.<br>0: Disable<br>1: Enable                                      |
| 23    | ATACLPREC  | R/W | CE-ATA Command Completion Signal Received Interrupt Enable<br>Enable/Disable receiving CE-ATA command completion signal interrupt.<br>0: Disable<br>1: Enable |
| 31:24 | Reserved   |     |                                                                                                                                                               |

#### 25.6.14 SDIO FIFO counter register (SDIO\_FIFOCNT)

Offset address: 0x48

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                          |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0  | FIFOCNT  | R   | Receive And Transmit FIFO Number<br>The number of data words to be written into FIFO or read out from FIFO.<br>Note: If the data length is not a multiple of 4, the last remaining bytes can be treated as one word. |
| 31:24 | Reserved |     |                                                                                                                                                                                                                      |

#### 25.6.15 SDIO data FIFO register (SDIO\_FIFODATA)

Offset address: 0x80

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                           |
|-------|------|-----|---------------------------------------------------------------------------------------|
| 31:0  | DATA | R/W | Receive And Transmit FIFO Data<br>Data to be written into FIFO or read out from FIFO. |

## 26 USB\_OTG

### 26.1 Introduction

This chip is embedded with three USB controllers in total.

#### OTG\_FS

OTG\_FS can support both host and slave functions to comply with the On-The-Go supplementary standard of USB 2.0 specification, and can also be configured as "Host only" or "Slave only" mode, to fully comply with USB 2.0 specification, and support host negotiation protocol (HNP) and session request protocol (SRP). In host mode, it supports full-speed (FS, 12Mb/s) and low-speed (LS, 1.5Mb/s) transmission, and in slave mode, it only supports full-speed (FS, 12Mb/s) transmission.

### 26.2 OTG\_FS global register address mapping

Table 128 OTG\_FS Global Register Address Mapping

| Register name     | Description                                              | Offset address |
|-------------------|----------------------------------------------------------|----------------|
| OTG_FS_GCTRLSTS   | Full-speed OTG control state register                    | 0x00           |
| OTG_FS_GINT       | Full-speed OTG interrupt register                        | 0x04           |
| OTG_FS_GAHBCFG    | Full-speed OTG AHB configuration register                | 0x08           |
| OTG_FS_GUSBCFG    | Full-speed OTG USB configuration register                | 0x0C           |
| OTG_FS_GRSTCTRL   | Full-speed OTG reset control register                    | 0x10           |
| OTG_FS_GCINT      | Full-speed OTG module interrupt register                 | 0x14           |
| OTG_FS_GINTMASK   | Full-speed OTG module interrupt mask register            | 0x18           |
| OTG_FS_GRXSTS     | Full-speed OTG read debug receive state register         | 0x1C           |
| OTG_FS_GRXSTSP    | Full-speed OTG state read and pop register               | 0x20           |
| OTG_FS_GRXFIFO    | Full-speed OTG receive FIFO size register                | 0x24           |
| OTG_FS_GTXFCFG    | Full-speed OTG TXFIFIO configuration register            | 0x28           |
| OTG_FS_GNPTXFQSTS | Full-speed OTG non-periodic TXFIFIO queue state register | 0x2C           |
| OTG_FS_GGCCFG     | Full-speed OTG general module configuration register     | 0x38           |
| OTG_FS_GCID       | Full-speed OTG module ID register                        | 0x3C           |
| OTG_FS_GHPTXFSIZE | Full-speed OTG host periodic TXFIFO size register        | 0x100          |
| OTG_FS_DTXFIFO1   | Full-speed OTG device IN endpoint TXFIFO size register 1 | 0x104          |

| Register name   | Description                                              | Offset address |
|-----------------|----------------------------------------------------------|----------------|
| OTG_FS_DTXFIFO2 | Full-speed OTG device IN endpoint TXFIFO size register 2 | 0x108          |
| OTG_FS_DTXFIFO3 | Full-speed OTG device In endpoint TXFIFO size register 3 | 0x10C          |

## 26.3 OTG\_FS global register functional description

### 26.3.1 Full-speed OTG control state register (OTG\_FS\_GCTRLSTS)

Offset address: 0x00

Reset value: 0x0000 0800

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | SREQSUC  | R   | Session Request Success<br>0: Session request fails<br>1: Session request succeeds<br>Note: It can be used only in device mode                                                                                                                                                                                                                                                                                                                                                                                                |
| 1     | SREQ     | R/W | Session Request<br>0: No request session<br>1: Request session<br>When HNSUCCHG bit of OTG_FS_GINT register is set, this bit will be cleared by writing 0. This bit will be cleared to 0 when HNSUCCHG is cleared to 0.<br>When USB 1.1 full-speed serial transceiver interface is used for session request, wait for V <sub>BUS</sub> to discharge to 0.2 V after the BSVD bit of the register is cleared to 0. The discharge time may be different according to different PHY.<br>Note: It can be used only in device mode. |
| 7:2   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 8     | HNSUC    | R   | Host Negotiation Success<br>This bit will be cleared to 0 when HNPREQ of this register is set to 1<br>0: Host negotiation fails<br>1: Host negotiation succeeds<br>Note: It can be used only in device mode.                                                                                                                                                                                                                                                                                                                  |
| 9     | HNPREQ   | R/W | Host Negotiation Protocol Request (HNP Request)<br>0: Not transmit HNP request<br>1: Transmit HNP request<br>When HNSUCCHG bit of OTG_FS_GINT register is set, this bit will be cleared by writing 0. This bit will be cleared to 0 when HNSUCCHG is cleared to 0.<br>Note: It can be used only in device mode.                                                                                                                                                                                                               |
| 10    | HHNPEN   | R/W | Host Set HNP Enable<br>0: Disable<br>1: Enable<br>Note: It can be used only in master mode.                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11    | DHNPEN   | R/W | Device HNP Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                           |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 0: Disable<br>1: Enable<br>Note: It can be used only in device mode.                                                                                                                                                                                                                                                  |
| 15:12 | Reserved |     |                                                                                                                                                                                                                                                                                                                       |
| 16    | CIDSTS   | R   | Connector ID Status<br>0: OTG_FS controller is in Device A mode<br>1: OTG_FS controller is in Device B mode<br>Note: It can be used in both device and master modes.                                                                                                                                                  |
| 17    | LSDEBT   | R   | Long/Short Debounce Time<br>Indicate the detected debounce time. The long debounce time is used for physical connection, and the short debounce time is used for software (program) connection.<br>0: Long debounce time (100ms+2.5μs)<br>1: Short debounce time (2.5μs)<br>Note: It can be used only in master mode. |
| 18    | ASVD     | R   | A-Session Valid<br>0: Invalid<br>1: Valid<br>Note: It can be accessed only in master mode.                                                                                                                                                                                                                            |
| 19    | BSVD     | R   | B-Session Valid<br>In OTG mode, this bit is used to confirm whether the device is in connected status.<br>0: Invalid<br>1: Valid<br>Note: It can be accessed only in device mode.                                                                                                                                     |
| 31:20 | Reserved |     |                                                                                                                                                                                                                                                                                                                       |

### 26.3.2 Full-speed OTG interrupt register (OTG\_FS\_GINT)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name       | R/W   | Description                                                                                                                   |
|-------|------------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | Reserved   |       |                                                                                                                               |
| 2     | SEFLG      | RC_W1 | Session End Flag<br>When $V_{BUS} < 0.8V$ , it means that $V_{BUS}$ is not used for B-session, and this bit will be set to 1. |
| 7:3   | Reserved   |       |                                                                                                                               |
| 8     | SREQSUCCHG | RC_W1 | Session Request Success Bit Change<br>If the value of SREQSUC bit changes, this bit will be set to 1.                         |
| 9     | HNSUCCHG   | RC_W1 | Host Negotiation Success Bit Change<br>If the value of HNSUC bit changes, this bit will be set to 1.                          |
| 16:10 | Reserved   |       |                                                                                                                               |
| 17    | HNFLG      | RC_W1 | Host Negotiation Flag<br>When USB host negotiation request is detected, this bit will be set to 1.                            |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                      |
|-------|----------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18    | ADTOFLG  | RC_W1 | A-Device Timeout Flag<br>If this bit is set to 1, it indicates timeout when A-device is waiting for B-device to connect.                                                                                                                                                                                         |
| 19    | DEBDFLG  | RC_W1 | Debounce Done Flag<br>When the equipment is connected and debounce is completed, this bit shall be set to 1; when an interrupt is generated, the USB will be reset.<br>This bit is valid only when HNPEN and SRPEN bits of OTG_FS_GUSBCFG register are set to 1.<br>Note: It can be accessed only in master mode |
| 31:20 | Reserved |       |                                                                                                                                                                                                                                                                                                                  |

### 26.3.3 Full-speed OTG AHB configuration register (OTG\_FS\_GAHBCFG)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                          |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | GINTMASK | R/W | Global Interrupt Mask<br>0: Mask global interrupt<br>1: Unmask global interrupt                                                                                                                                                                                                                                                      |
| 6:1   | Reserved |     |                                                                                                                                                                                                                                                                                                                                      |
| 7     | TXFEL    | R/W | TXFIFO Empty Level<br>In device mode:<br>0: TXFE interrupt means that IN endpoint TXFIFIO is half-empty<br>1: TXFE interrupt means that IN endpoint TXFIFIO is all-empty<br>In master mode:<br>0: NPTXFEM interrupt means that non-periodic TXFIFO is half-empty<br>1: NPTXFEM interrupt means that non-periodic TXFIFO is all-empty |
| 8     | PTXFEL   | R/W | Periodic TXFIFO Empty Level<br>0: PTXFE interrupt means that periodic TXFIFIO is half-empty<br>1: PTXFE interrupt means that periodic TXFIFIO is all-empty<br>Note: It can be accessed only in master mode                                                                                                                           |
| 31:9  | Reserved |     |                                                                                                                                                                                                                                                                                                                                      |

### 26.3.4 Full-speed OTG USB configuration register (OTG\_FS\_GUSBCFG)

Offset address: 0x0C

Reset value: 0x0000 0A00

| Field | Name     | R/W | Description                                                                                                                                                                                                                  |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | SEFLG    | R/W | FS Timeout Calibrate<br>The additional delay of PHY includes the number of PHY clocks and FS timeout interval. The status of data line may be different for different PHY.<br>The timeout value of OTG_FS is 16~18-bit time. |
| 5:3   | Reserved |     |                                                                                                                                                                                                                              |



| Field | Name     | R/W | Description                                                                                                                                                                         |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6     | FSSTSEL  | W   | Full-Speed Serial Transceiver Select<br>0: USB2.0 full-speed ULPI PHY<br>1: USB1.1 full-speed serial transceiver<br>This bit is always 1.                                           |
| 7     | Reserved |     |                                                                                                                                                                                     |
| 8     | SRPEN    | R/W | SRP Enable<br>0: Disable<br>1: Enable<br>If the SRP function is disabled, connecting the device cannot be requested to activate V <sub>BUS</sub> and the session cannot be started. |
| 9     | HNPEN    | R/W | HNP Enable<br>0: Disable<br>1: Enable                                                                                                                                               |
| 13:10 | TRTIM    | R/W | USB Turnaround Time<br>$f_{PHYCLK}=48MHz$ , in $f_{PHYCLK}$ .<br>$TRTIM=4 \times f_{AHBCLK} + f_{PHYCLK}$<br>Example:<br>When $f_{AHBCLK}=72MHz$ , TRTIM will be set to 7.          |
| 28:14 | Reserved |     |                                                                                                                                                                                     |
| 29    | FHMODE   | R/W | Forced Host Mode<br>0: Normal mode<br>1: Master mode                                                                                                                                |
| 30    | FDMODE   | R/W | Forced Device Mode<br>0: Normal mode<br>1: Device mode                                                                                                                              |
| 31    | CTXP     | R/W | Corrupt TX Packet<br>Debug bit, which cannot be set to 1.<br>Note: It can be accessed in both device and master mode.                                                               |

### 26.3.5 Full-speed OTG reset register (OTG\_FS\_GRSTCTRL)

Offset address: 0x10

Reset value: 0x2000 0000

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CSRST | R/S | Core Soft Reset<br>This bit controls HCLK and PCLK reset<br>Clear each interrupt and all control state register bits to 0 except the followings:<br>- GCLK bit in OTG_FS_PCGCTRL<br>- PCLKSTOP bit in OTG_FS_PCGCTRL<br>- PHYCLKSEL bit in OTG_FS_HCFG<br>- DSPDSEL bit in OTG_FS_DCFG<br>Reset the AHB slave to the idle state and clear TXFIFO and RXFIFO. When the AHB transmission ends, all transactions of AHB shall be terminated as soon as possible and all transactions on USB shall be terminated immediately. |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | <p>Software reset is used generally in either of the following situations:</p> <ul style="list-style-type: none"> <li>● Software development period.</li> <li>● After the user dynamically changes the PHY selection bit in the USB configuration register listed above. When the user changes the PHY, the corresponding clock will be selected for the PHY and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset so as to ensure normal operation.</li> </ul> |
| 1     | HSRST    | R/S | <p>HCLK Soft Reset</p> <p>This bit is used to refresh the control logic of AHB clock domain.</p> <p>When clearing this interrupt, the corresponding mask interrupt state control bit shall be cleared; when the interrupt state bit is not cleared to zero, the event state after this bit is set to 1 can be read.</p>                                                                                                                                                                          |
| 2     | HFCNTRST | R/S | <p>Host Frame Counter Reset</p> <p>Reset the frame counter in the host by writing this bit, and the SOF frame number transmitted subsequently is 0.</p> <p>Note: It can be accessed only in master mode.</p>                                                                                                                                                                                                                                                                                     |
| 3     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 4     | RXFFLU   | R/S | <p>RXFIFO Flush</p> <p>This bit is used to refresh the whole RXFIFO. Before writing to this bit, it is required to ensure that the module does not perform read and write operation to RXFIFO.</p> <p>Only after this bit is cleared to 0, can other operations be performed (usually need to wait for 8 clock cycles).</p>                                                                                                                                                                      |
| 5     | TXFFLU   | R/S | <p>TXFIFO Flush</p> <p>This bit is used to refresh one or the whole TXFIFO. Before writing to this bit, it is required to ensure that the module does not perform read and write operation to TXFIFO.</p>                                                                                                                                                                                                                                                                                        |
| 10:6  | TXFNUM   | R/W | <p>TXFIFO Number</p> <p>Refresh the FIFO number with TXFIFO refresh bits, and these bits can only be changed after the refresh TXFFIO is cleared to 0.</p> <p>In master mode:</p> <p>00000: Refresh non-periodic TXFIFO</p> <p>00001: Refresh periodic TXFIFO</p> <p>10000: Refresh all TXFIFO</p> <p>In device mode:</p> <p>00000: Refresh TXFIFO 0</p> <p>00001: Refresh TXFIFO 1</p> <p>.....</p> <p>00101: Refresh TXFIFO 15</p> <p>10000: Refresh all TXFIFO</p>                            |
| 30:11 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 31    | AHBMIDL  | R   | <p>AHB Master Idle</p> <p>This bit indicates whether the AHB master device is idle.</p>                                                                                                                                                                                                                                                                                                                                                                                                          |

### 26.3.6 Full-speed OTG module interrupt register (OTG\_FS\_GCINT)

Offset address: 0x14

Reset value: 0x0400 0020

In order to avoid generating interrupts before initialization, the software must clear this register to zero before enabling the interrupt bit.

| Field | Name      | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CURMOSEL  | R     | Current Mode of Operation Select<br>0: Device mode<br>1: Master mode                                                                                                                                                                                                                                                                                                                                               |
| 1     | MMIS      | RC_W1 | Mode Mismatch Interrupt<br>This bit will be set to 1 when accessing the following registers:<br><ul style="list-style-type: none"> <li>Access the master mode register in device mode</li> <li>Access the device mode register in master mode</li> </ul>                                                                                                                                                           |
| 2     | OTG       | R     | OTG Interrupt<br>When this bit is set to 1, it indicates that an OTG protocol event has occurred.<br>By reading OTG_FS_GINT register, determine the event that causes the OTG interrupt. This bit can be cleared to zero only after the corresponding bit of the register is cleared.                                                                                                                              |
| 3     | SOF       | RC_W1 | Start of Frame Interrupt<br>When this bit is set:<br><ul style="list-style-type: none"> <li>In master mode, it indicates that USB has transmitted one SOF (FS) or Keep-Alive (LS);</li> <li>In device mode, it indicates that USB has received one SOF, and the current frame number can be obtained by reading the device state register. An interrupt will be generated only when running in FS mode.</li> </ul> |
| 4     | RXFNONE   | R     | RXFIFO Non-empty Interrupt<br>This bit indicates that there are still packets in RXFIFO that have not been read.                                                                                                                                                                                                                                                                                                   |
| 5     | NPTXFEM   | R     | Non-periodic TXFIFO Empty Interrupt<br>This interrupt will be triggered when the non-periodic TXFIFO is not empty and there is space for writable entries in the request queue.<br>Note: It can be accessed only in master mode                                                                                                                                                                                    |
| 6     | GINNPNAKE | R     | Global IN Non-periodic NAK Effective Interrupt<br>This bit indicates that GINAKSET bit of OTG_FS_DCTRL register is valid; this bit can be cleared by clearing GINAKCLR bit of OTG_FS_DCTRL register.<br>As the priority of STALL is higher than that of NAK bit, generation of this interrupt cannot mean that USB has sent NAK signal.<br>Note: It can be accessed only in device mode                            |
| 7     | GONAKE    | R     | Global OUT NAK Effective Interrupt<br>This bit indicates that GONAKSET bit of OTG_FS_DCTRL register is valid; this bit can be cleared by clearing GONALCLR bit of OTG_FS_DCTRL.<br>Note: It can be accessed only in device mode                                                                                                                                                                                    |
| 9:8   | Reserved  |       |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 10    | ESUS      | RC_W1 | Early Suspend Interrupt<br>When USB has been idle for 3ms, this bit will be set to 1.<br>Note: It can be accessed only in device mode                                                                                                                                                                                                                                                                              |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11    | USBSUS   | RC_W1 | USB Suspend Interrupt<br>When USB suspending is detected, this bit will be set to 1; when USB has been idle for 3ms, it will enter pending state.<br>Note: It can be accessed only in device mode                                                                                                                                                                                                                                          |
| 12    | USBRST   | RC_W1 | USB Reset Interrupt<br>This bit will be set to 1 when reset is detected on USB.<br>Note: It can be accessed only in device mode                                                                                                                                                                                                                                                                                                            |
| 13    | ENUMD    | RC_W1 | Enumeration Done Interrupt<br>This bit will be set to 1 when speed enumeration is completed.<br>Note: It can be accessed only in device mode                                                                                                                                                                                                                                                                                               |
| 14    | ISOPD    | RC_W1 | Isochronous OUT Packet Dropped Interrupt<br>When the RXFIFO space is insufficient and the module cannot write synchronous OUT data packet to RXFIFO, this bit will be set to 1.<br>Note: It can be accessed only in device mode                                                                                                                                                                                                            |
| 15    | EOPF     | RC_W1 | End of Periodic Frame Interrupt<br>This bit indicates that the current frame has reached the period specified by PFITV bit of OTG_FS_DCFG register.<br>Note: It can be accessed only in device mode                                                                                                                                                                                                                                        |
| 17:16 | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 18    | INEP     | R     | IN Endpoint Interrupt<br>This bit will be set to 1 when a pending interrupt occurs to one IN endpoint<br>Determine the number of IN endpoint to which an interrupt occurs by reading OTG_FS_DAEPINT register, and determine the causes of the interrupt by reading OTG_FS_DIEPINTx register.<br>To clear this bit, first clear the corresponding state bit of OTG_FS_DIEPINTx register.<br>Note: It can be accessed only in device mode    |
| 19    | ONEP     | R     | OUT Endpoint Interrupt<br>This bit will be set to 1 when a pending interrupt occurs to one OUT endpoint<br>Determine the number of OUT endpoint to which an interrupt occurs by reading OTG_FS_DAEPINT register, and determine the causes of the interrupt by reading OTG_FS_DOEPINTx register.<br>To clear this bit, first clear the corresponding state bit of OTG_FS_DOEPINTx register.<br>Note: It can be accessed only in device mode |
| 20    | IIINTX   | RC_W1 | Incomplete Isochronous IN Transfer Interrupt<br>This bit will be set to 1 when the transmission on at least one synchronous IN endpoint in the current frame is not completed.<br>This interrupt is triggered at the same time with EOPF.<br>Note: It can be accessed only in device mode                                                                                                                                                  |

| Field | Name      | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-----------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21    | IP_OUTTX  | RC_W1 | <p>Incomplete Periodic Transfer Interrupt</p> <p>When this bit is set to 1, the interrupts indicated by it are different in different modes.</p> <p>In the master mode, if the periodic transaction scheduled to be completed in the current frame is still pending (i.e. incomplete), the incomplete periodic transmission interrupt will be triggered.</p> <p>In device mode, when the transmission on at least one synchronous OUT endpoint in the current frame is not completed, interrupt of incomplete OUT synchronous transmission will be triggered, and this interrupt will be triggered at the same time with EOPF.</p> |
| 23:22 | Reserved  |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 24    | HPORT     | R     | <p>Host Port Interrupt</p> <p>This bit will be set to 1 when the state of full-speed OTG controller port changes in master mode.</p> <p>Note: It can be accessed only in master mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 25    | HCHAN     | R     | <p>Host Channels Interrupt</p> <p>This bit will be set to 1 when a suspended interrupt is generated on host channel.</p> <p>Note: It can be accessed only in master mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 26    | PTXFE     | R     | <p>Periodic TXFIFO Empty Interrupt</p> <p>This interrupt will be triggered when the periodic TXFIFO is empty and there is space for writable entries in the request queue. Note: It can be accessed only in master mode</p>                                                                                                                                                                                                                                                                                                                                                                                                        |
| 27    | Reserved  |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 28    | CINSTSCHG | RC_W1 | <p>Connector ID Status Change Interrupt</p> <p>This bit will be set to 1 when the state of connector ID line changes.</p> <p>Note: It can be accessed in both master and device mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 29    | DEDIS     | RC_W1 | <p>Device Disconnect Interrupt</p> <p>This bit will be set to 1 when device disconnection is detected.</p> <p>Note: It can be accessed only in master mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 30    | SREQ      | RC_W1 | <p>Session Request/New Session Interrupt</p> <p>In different modes, the conditions for triggering this interrupt are:</p> <ul style="list-style-type: none"> <li>● Session request is detected in master mode</li> <li>● In device mode, <math>V_{BUS}</math> is within the range of B-device</li> </ul>                                                                                                                                                                                                                                                                                                                           |
| 31    | RWAKE     | RC_W1 | <p>Resume/Remote Wakeup Interrupt</p> <p>In different modes, the conditions for triggering this interrupt are:</p> <ul style="list-style-type: none"> <li>● Remote wakeup signal is detected on USB in master mode</li> <li>● Resume signal is detected on USB bus in device mode</li> </ul>                                                                                                                                                                                                                                                                                                                                       |

### 26.3.7 Full-speed OTG module interrupt mask register (OTG\_FS\_GINTMASK)

Offset address: 0x18

Reset value: 0x0000 0000

This register is used to mask the interrupt, but the corresponding bit of the interrupt register will still be set to 1.

| Field | Name       | R/W | Description                                                                                                                  |
|-------|------------|-----|------------------------------------------------------------------------------------------------------------------------------|
| 0     | Reserved   |     |                                                                                                                              |
| 1     | MMISM      | R/W | Mode Mismatch Interrupt Mask<br>0: Mask<br>1: Not mask                                                                       |
| 2     | OTGM       | R/W | OTG Interrupt Mask<br>0: Mask<br>1: Not mask                                                                                 |
| 3     | SOFM       | R/W | Frame Start Interrupt Mask<br>0: Mask<br>1: Not mask                                                                         |
| 4     | RXFNONEM   | R/W | RXFIFO Nonempty Interrupt Mask<br>0: Mask<br>1: Not mask                                                                     |
| 5     | NPTXFEMM   | R/W | Nonperiodic TXFIFO Empty Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in master mode            |
| 6     | GINNPNAKEM | R/W | Global IN Nonperiodic NAK Effective Interrupt Make<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode |
| 7     | GONAKEM    | R/W | Global OUT NAK Effective Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode            |
| 9:8   | Reserved   |     |                                                                                                                              |
| 10    | ESUSM      | R/W | Early Suspend Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                       |
| 11    | USBSUSM    | R/W | USB Suspend Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                         |
| 12    | USBRSTM    | R/W | USB Reset Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                           |
| 13    | ENUMDM     | R/W | Enumeration Done Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                    |
| 14    | ISOPDM     | R/W | Isochronous OUT Packet Dropped Interrupt Mask<br>0: Mask                                                                     |

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                        |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |           |     | 1: Not mask<br>Note: It can be accessed only in device mode                                                                                                                                                                                                                        |
| 15    | EOPFM     | R/W | End of Periodic Frame Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                                                                                                                                                                     |
| 16    | Reserved  |     |                                                                                                                                                                                                                                                                                    |
| 17    | EPMISM    | R/W | Endpoint Mismatch Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                                                                                                                                                                         |
| 18    | INEPM     | R/W | IN Endpoint Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                                                                                                                                                                               |
| 19    | OUTEPM    | R/W | OUT Endpoint Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                                                                                                                                                                              |
| 20    | IIINTXM   | R/W | Incomplete Isochronous IN Transfer Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                                                                                                                                                        |
| 21    | IP_OUTTXM | R/W | Incomplete Periodic Transfer Interrupt Mask<br>In master mode, this bit controls whether to mask incomplete periodic transmission interrupt.<br>In device mode, this bit controls whether to mask the incomplete OUT synchronous transmission interrupt.<br>0: Mask<br>1: Not mask |
| 23:22 | Reserved  |     |                                                                                                                                                                                                                                                                                    |
| 24    | HPORTM    | R/W | Host Port Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in master mode                                                                                                                                                                                 |
| 25    | HCHM      | R/W | Host Channels Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in master mode                                                                                                                                                                             |
| 26    | PTXFEM    | R/W | Periodic TXFIFO Empty Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in master mode                                                                                                                                                                     |
| 27    | Reserved  |     |                                                                                                                                                                                                                                                                                    |

| Field | Name     | R/W | Description                                                                                                                    |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------|
| 28    | CIDSTSCM | R/W | Connector ID Status Change Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed in both master and device mode |
| 29    | DEDISM   | R/W | Device Disconnect Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed only in device mode                     |
| 30    | SREQM    | R/W | Session Request/New Session Interrupt Mask<br>0: Mask<br>1: Not mask                                                           |
| 31    | RWAKEM   | R/W | Resume/Remote Wakeup Interrupt Mask<br>0: Mask<br>1: Not mask<br>Note: It can be accessed in both master and device mode       |

### 26.3.8 Full-speed OTG read debug receive state register/full-speed OTG state read and pop register (OTG\_FS\_GRXSTS/OTG\_FS\_GRXSTSP)

Read offset address: 0x1C

Pop offset address: 0x20

Reset value: 0x0000 0000

#### Master mode

| Field | Name     | R/W | Description                                                                                                                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | CHNUM    | R   | Channel Number<br>This bit indicates the received data is transmitted by which channel.                                                                                                                                       |
| 14:4  | BCNT     | R   | Byte Count<br>This bit indicates the byte count of received IN data packet.                                                                                                                                                   |
| 16:15 | DPID     | R   | Data Packet ID<br>This bit indicates the received data packet ID (PID)<br>00: DATA0<br>10: DATA1<br>01: DATA2<br>11: MDATA                                                                                                    |
| 20:17 | PSTS     | R   | Packet Status<br>This bit indicates the status of the received data packet.<br>0010: Received IN data packet<br>0011: IN transmission completed<br>0101: Data synchronization error<br>0111: Channel stop<br>Others: Reserved |
| 31:21 | Reserved |     |                                                                                                                                                                                                                               |

#### Device mode



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                 |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | EPNUM    | R   | Endpoint Number<br>This bit indicates the received data is transmitted by which endpoint.                                                                                                                                                                   |
| 14:4  | BCNT     | R   | Byte Count<br>This bit indicates the byte count of received data packet                                                                                                                                                                                     |
| 16:15 | DPID     | R   | Data PID<br>This bit indicates the received data packet ID (PID)<br>00: DATA0<br>10: DATA1<br>01: DATA2<br>11: MDATA                                                                                                                                        |
| 20:17 | PSTS     | R   | Packet Status<br>This bit indicates the status of received data packet<br>0001: Global OUT NAK<br>0010: Received OUT data packet<br>0011: OUT transmission completed<br>0100: SETUP event completed<br>0110: Received SETUP data packet<br>Others: Reserved |
| 24:21 | FNUM     | R   | Frame Number<br>These bits are valid when synchronous OUT endpoint is supported.<br>These bits are the 4 least significant bits of the packet frame number received on the USB                                                                              |
| 31:25 | Reserved |     |                                                                                                                                                                                                                                                             |

### 26.3.9 Full-speed OTG receive FIFO size register (OTG\_FS\_GRXFIFO)

Offset address: 0x24

Reset value: 0x0000 0200

| Field | Name     | R/W | Description                                                        |
|-------|----------|-----|--------------------------------------------------------------------|
| 15:0  | RXFDEP   | R/W | RXFIFO Depth<br>RXFIFO is in word, and the depth range is: 16~256. |
| 31:16 | Reserved |     |                                                                    |

### 26.3.10 Full-speed OTG TXFIFO configuration register (OTG\_FS\_GTXFCFG)

Offset address: 0x28

Reset value: 0x0000 0200

#### Master mode

| Field | Name     | R/W | Description                                                                                              |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------|
| 15:0  | NPTXSA   | R/W | Nonperiodic TXFIFO RAM Start Address<br>This bit indicates the start address of non-periodic TXFIFO RAM. |
| 31:16 | NPTXFDEP | R/W | Nonperiodic TXFIFO Depth<br>TXFIFO is in word, and the depth range is: 16~256.                           |

### Device mode

| Field | Name     | R/W | Description                                                                                             |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------|
| 15:0  | EPTXSA   | R/W | Endpoint0 TXFIFO RAM Start Address<br>This bit indicates the start address of TXFIFO RAM of endpoint 0. |
| 31:16 | EPTXFDEP | R/W | Endpoint0 TXFIFO Depth<br>TXFIFO is in word, and the depth range is: 16~256.                            |

### 26.3.11 Full-speed OTG non-periodic TXFIFO queue state register (OTG\_FS\_GNPTXFQSTS)

Offset address: 0x2C

Reset value: 0x0008 0200

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | NPTXFSA  | R   | Nonperiodic TXFFIO Space Available<br>These bits indicate the size of available space of non-periodic TXFIFO. (In 32-bit words) 0x0: Non-periodic TXFIFO is full<br>0x1: 1 word<br>0x2: 2 words<br>.....<br>0xn: n words are available (0≤n≤256)<br>Others: Reserved                                                                                                 |
| 23:16 | NPTXRSA  | R   | Non-periodic Transmit Request Space Available<br>This bit indicates the available space size of non-periodic transmit request queue.<br>In master mode: Save IN and OUT requests<br>In device mode: There is only IN request<br>0x0: The queue is full<br>0x0: 1 position<br>0x2: 2 positions<br>.....<br>0xn: n positions are available (0≤n≤8)<br>Others: Reserved |
| 30:24 | NPTXRQ   | R   | Nonperiodic Transmit Request Queue<br>Bit 24: Terminate (last data selected for channel/endpoint)<br>Bit [26:25]:<br>00: IN/OUT token<br>01: The transmit data packet length is 0 (IN in device mode/OUT in master mode)<br>10: PING/CPLIT token<br>11: Stop channel instruction<br>Bit [30:27]: Channel/endpoint number                                             |
| 31    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                      |

### 26.3.12 Full-speed OTG general module configuration register (OTG\_FS\_GGCCFG)

Offset address: 0x38

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                              |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | Reserved |     |                                                                                                                                                          |
| 16    | PWEN     | R/W | Power Down Enable<br>This bit is used to activate the transceiver.<br>0: Power down is activated<br>1: Power down inactivated (activate the transceiver) |
| 17    | Reserved |     |                                                                                                                                                          |
| 18    | ADVBSSEN | R/W | A Device V <sub>BUS</sub> Sensing Enable<br>0: Disable<br>1: Enable                                                                                      |
| 19    | BDVBSSEN | R/W | B Device V <sub>BUS</sub> Sensing Enable<br>0: Disable<br>1: Enable                                                                                      |
| 20    | SOFPOUT  | R/W | SOF Pulse Available on PAD Output<br>This bit selects whether SOF pulse can be output from PAD.<br>0: No<br>1: Yes                                       |
| 21    | VBSDIS   | R/W | V <sub>BUS</sub> Sensing Disable<br>0: Enable V <sub>BUS</sub> sensing<br>1: Disable V <sub>BUS</sub> sensing                                            |
| 31:22 | Reserved |     |                                                                                                                                                          |

### 26.3.13 Full-speed OTG module ID register (OTG\_FS\_GCID)

Offset address: 0x3C

Reset value: 0x0000 1100

| Field | Name | R/W | Description                                             |
|-------|------|-----|---------------------------------------------------------|
| 31:0  | PID  | R/W | Product ID<br>Product ID can be programmed by this bit. |

### 26.3.14 Full-speed OTG host periodic TXFIFO size register (OTG\_FS\_GHPTXFSIZE)

Offset address: 0x100

Reset value: 0x0200 0600

| Field | Name     | R/W | Description                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------|
| 15:0  | HPDXTXFS | R/W | Host Periodic TXFIFO Start Address                                            |
| 31:16 | HPDXTXFD | R/W | Host Periodic TXFIFO Depth<br>TXFIFO is in word, and the minimum value is 16. |

### 26.3.15 Full-speed OTG device IN endpoint TXFIFO size register x (OTG\_FS\_DIEPTXFIFOx) (x=1~3)

Offset address: 0x104+4(x-1)

Reset value: 0x0200 0400

x is FIFO number.

| Field | Name       | R/W | Description                                                                                                                                                           |
|-------|------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | INEPTXFRSA | R/W | IN Endpoint TXFIFOx Transmit RAM Start Address<br>These bits indicate the start address of the IN endpoint TXFIFOx RAM and need to be aligned with the 32-bit memory. |
| 31:16 | INEPTXFDEP | R/W | IN Endpoint TXFIFO Depth<br>TXFIFO is in word, and the minimum value is 16.                                                                                           |

## 26.4 OTG\_FS host mode register address mapping

Table 129 OTG\_FS Host Mode Register Address Mapping

| Register name    | Description                                                        | Offset address |
|------------------|--------------------------------------------------------------------|----------------|
| OTG_FS_HCFG      | Full-speed OTG host configuration register                         | 0x400          |
| OTG_FS_HFIVL     | Full-speed OTG host frame interval register                        | 0x404          |
| OTG_FS_HFIFM     | Full-speed OTG host frame information register                     | 0x408          |
| OTG_FS_HPTXSTS   | Full-speed OTG host periodic transmission state register           | 0x410          |
| OTG_FS_HACHINT   | Full-speed OTG host all-channel interrupt register                 | 0x414          |
| OTG_FS_HACHIMASK | Full-speed OTG host all-channel interrupt mask register            | 0x418          |
| OTG_FS_HPORTCSTS | Full-speed OTG host port control state register                    | 0x440          |
| OTG_FS_HCHX      | Full-speed OTG host channel-X characteristics register (X=0...7)   | 0x500+20*X     |
| OTG_FS_HCHINTX   | Full-speed OTG host channel-X interrupt register (X=0...7)         | 0x508+20*X     |
| OTG_FS_HCHIMASKX | Full-speed OTG host channel-X interrupt mask register (X=0...7)    | 0x50C+20*X     |
| OTG_FS_HCHTSIZEX | Full-speed OTG host channel-X transmission size register (X=0...7) | 0x510+20*X     |

## 26.5 OTG\_FS host mode register functional description

### 26.5.1 Full-speed OTG host configuration register (OTG\_FS\_HCFG)

Offset address: 0x400

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | PHYCLKSEL | R/W | FS/LS PHY Clock Select <ul style="list-style-type: none"> <li>In FS mode:               <ul style="list-style-type: none"> <li>01: PHY clock is 48MHz</li> <li>Others: Reserved</li> </ul> </li> <li>In LS mode:               <ul style="list-style-type: none"> <li>00: Reserved</li> <li>01: PHY clock is 48MHz</li> <li>10: PHY clock is 6MHz</li> <li>11: Reserved</li> </ul> </li> </ul> Note: Software reset is required after the value of this bit is changed. |
| 2     | FSSPT     | R   | FS Support<br>After the host is connected to the device, select whether the host follows the maximum speed supported by the device. If this bit is set to 1, even if the device supports HS mode, the host supports FS at most.<br>0: The host can support HS/FS/LS<br>1: The host only supports FS/LS                                                                                                                                                                  |
| 31:3  | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

### 26.5.2 Full-speed OTG host frame interval register (OTG\_FS\_HFIVL)

Offset address: 0x404

Reset value: 0x0000 EA60

This register can be edited only after the port (PEN bit of OTG\_FS\_HPORTCSTS register is set to 1) is enabled.

| Field | Name     | R/W | Description                                                                                                                                                                     |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | FIVL     | R/W | Frame Interval<br>This bit is used to control the time interval between two continuous SOF (FS), micro-SOF (HS), and Keep-Alive (LS).<br>Time interval=frame duration×PHY clock |
| 31:16 | Reserved |     |                                                                                                                                                                                 |

### 26.5.3 Full-speed OTG host frame information register (OTG\_FS\_HFIFM)

Offset address: 0x408

Reset value: 0x0000 3FFF

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                      |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | FNUM   | R   | Frame Number<br>This bit is used to indicate the current frame number. This bit will be cleared to zero when reaching 0x3FFF.                                                                                                                                                                    |
| 31:16 | FRTIME | R   | Frame Remaining Time<br>This bit is used to indicate the current remaining time of frame. The initial value is the value of OTG_FS_HFIVL, and every time passing one PHY clock, the value of this bit will decrease by 1, and when reaching 0, this bit will reload the value of frame interval. |

## 26.5.4 Full-speed OTG host periodic transmission state register (OTG\_FS\_HPTXSTS)

Offset address: 0x410

Reset value: 0x0008 0100

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                 |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | FSPACE | R/W | Periodic Transmit Data FIFO Available Space<br>This bit indicates the idle space of periodic TXFIFO (in 32-bit word).<br>0x0: TXFIFO is full<br>0x1: 1 word<br>0x2: 2 words<br>0xn: n words are available (0<n<512)<br>Others: Reserved                                                                                                     |
| 23:16 | QSPACE | R   | Periodic Transmit Request Queue Available Space<br>This bit indicates the available space of periodic transmit request queue.<br>0x0: The queue is full<br>0x1: 1 position<br>0x2: 2 positions<br>0xn: n positions are available (0<n<8)<br>Others: Reserved                                                                                |
| 31:24 | QTOP   | R   | Top of the Periodic Transmit Request Queue<br>This bit indicates the transaction being processed in periodic transmit request queue.<br>[24]: End<br>[26:25]: Type<br>00: IN/OUT<br>01: Zero-length data packet<br>11: Disable channel command<br>[30:27]: Channel/endpoint number<br>[31]: Odd/even frame<br>0: Even frame<br>1: Odd frame |

## 26.5.5 Full-speed OTG host all-channel interrupt register (OTG\_FS\_HACHINT)

Offset address: 0x414

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                |
|-------|----------|-----|--------------------------------------------------------------------------------------------|
| 15:0  | ACHINT   | R   | All Channels Interrupts<br>No. X bit represents interrupt of Channel X. Up to 16 channels. |
| 31:16 | Reserved |     |                                                                                            |

## 26.5.6 Full-speed OTG host all-channel interrupt mask register (OTG\_FS\_HACHIMASK)

Offset address: 0x418

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                    |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | ACHIMASK | R/W | All Channels Interrupts Mask<br>No. X bit represents interrupt mask of Channel X. Up to 16 channels.<br>0: Mask<br>1: Not mask |
| 31:16 | Reserved |     |                                                                                                                                |

### 26.5.7 Full-speed OTG host port control state register (OTG\_FS\_HPORTCSTS)

Offset address: 0x440

Reset value: 0x0000 0000

| Field | Name     | R/W   | Description                                                                                                                                                                                                                     |
|-------|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PCNNTFLG | R     | Port Connect Flag<br>0: The port is not connected<br>1: Port connected                                                                                                                                                          |
| 1     | PCINTFLG | RC_W1 | Port Connect Interrupt Flag<br>This bit will be set to 1 when the port is connected to the device.                                                                                                                              |
| 2     | PEN      | RC_W0 | Port Enable<br>After the port resets the sequence, the program cannot write to this bit, and can only enable the port through the module. If this bit is cleared to zero, the port will be disabled.<br>0: Disable<br>1: Enable |
| 3     | PENCHG   | RC_W1 | PEN Bit Change<br>This bit will be set to 1 when PEN bit of this register changes.                                                                                                                                              |
| 4     | POVC     | R     | Port Overcurrent<br>This bit indicates whether this port is overloaded.<br>0: No overload<br>1: Overload                                                                                                                        |
| 5     | POVCCHG  | RC_W1 | POVC Bit Change<br>This bit will be set to 1 when POVC bit changes.                                                                                                                                                             |
| 6     | PRS      | R/W   | Port Resume<br>0: Resume signal is not driven<br>1: Resume signal is driven                                                                                                                                                     |
| 7     | PSUS     | R/S   | Port Suspend<br>0: Port is not suspended<br>1: Port is suspended                                                                                                                                                                |
| 8     | PRST     | R/W   | Port Reset<br>The port can start reset only when this bit is set to 1 for over 10ms.<br>0: Not in reset state<br>1: In reset state                                                                                              |
| 9     | Reserved |       |                                                                                                                                                                                                                                 |

| Field | Name     | R/W | Description                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:10 | PDLSTS   | R   | Port Data Line Status<br>This bit indicates the logic level of the USB data line at this time.<br>[10] bit means OTG_FS_FS_DP<br>[11] bit means OTG_FS_FS_DM              |
| 12    | PP       | R/W | Port Power<br>This bit controls the power-on of the port. If there is overload, the port will power down (clear 0).<br>0: Power down<br>1: Power on                       |
| 16:13 | PTSEL    | R/W | Port Test Mode Select<br>0000: Test is disabled<br>0001: Test_J<br>0010: Test_K<br>0011: Test_SE0_NAK<br>0100: Test_Packet<br>0101: Test_Force_Enable<br>Others: Reserved |
| 18:17 | PSPDSEL  | R   | Port Speed Select<br>01: Full speed<br>10: Low speed<br>11: Reserved                                                                                                      |
| 31:19 | Reserved |     |                                                                                                                                                                           |

### 26.5.8 Full-speed OTG host channel-X characteristics register (OTG\_FS\_HCHX) (X=0...7)

Offset address: 0x500+20\*X

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 10:0  | MAXPSIZE | R/W | Maximum Data Packet Size<br>This bit indicates the maximum data packet size of the device endpoint connected to the host.     |
| 14:11 | EDPNUM   | R/W | Endpoint Number<br>This bit indicates the number of the device endpoint connected to the host.                                |
| 15    | EDPDRT   | R/W | Endpoint Direction<br>0: OUT<br>1: IN                                                                                         |
| 16    | Reserved |     |                                                                                                                               |
| 17    | LSDV     | R/W | Low-speed Device<br>This bit indicates the low-speed device is connected.                                                     |
| 19:18 | EDPTYP   | R/W | Endpoint Type<br>This bit is used to select the transmission type of endpoint.<br>00: Control<br>01: Synchronous<br>10: Batch |



| Field | Name   | R/W | Description                                                                                                                                                                                                  |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |        |     | 11: Interrupt                                                                                                                                                                                                |
| 21:20 | CNTSEL | R/W | Count Function Select<br>In this register, this bit is only used to indicate the number of transactions that must be executed by the periodic endpoint per frame.<br>00: Reserved<br>01: 1<br>10: 2<br>11: 3 |
| 28:22 | DVADDR | R/W | Device Address<br>This bit indicates the device address connected to the host.                                                                                                                               |
| 29    | ODDF   | R/W | Odd Frame<br>This bit controls whether the OTG host transmits in odd frame.<br>0: Even frame<br>1: Odd frame<br>Note: It applies only to periodic transactions.                                              |
| 30    | CHINT  | R/S | Channel Interrupt<br>0: Not interrupt<br>1: Stop transmitting data through the channel                                                                                                                       |
| 31    | CHEN   | R/S | Channel Enable<br>0: Disable<br>1: Enable                                                                                                                                                                    |

### 26.5.9 Full-speed OTG host channel-X interrupt register (OTG\_FS\_HCHINTX) (X=0...7)

Offset address: 0x508+20\*X

Reset value: 0x0000 0000

| Field | Name     | R/W   | Description                                                                                                                         |
|-------|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TSFCMPN  | RC_W1 | Transfer Complete Normally                                                                                                          |
| 1     | TSFCMPAN | RC_W1 | Transfer Complete Abnormally                                                                                                        |
| 2     | Reserved |       |                                                                                                                                     |
| 3     | RXSTALL  | RC_W1 | STALL Response Received Interrupt                                                                                                   |
| 4     | RXNAK    | RC_W1 | NAK Response Received Interrupt                                                                                                     |
| 5     | RXTXACK  | RC_W1 | ACK Response Received/Transmitted Interrupt                                                                                         |
| 6     | Reserved |       |                                                                                                                                     |
| 7     | TERR     | RC_W1 | Transaction Error<br>Indicate that one of the following errors occurs:<br>CRC failure<br>Timeout<br>Bit stuffing error<br>EOP error |
| 8     | BABBLE   | RC_W1 | Babble Error                                                                                                                        |

| Field | Name     | R/W   | Description         |
|-------|----------|-------|---------------------|
| 9     | FOVR     | RC_W1 | Frame Overrun Error |
| 10    | DTOG     | RC_W1 | Data Toggle Error   |
| 31:11 | Reserved |       |                     |

## 26.5.10 Full-speed OTG host channel-X interrupt mask register (OTG\_FS\_HCHIMASKX) (X=0...7)

Offset address: 0x50C+20\*X

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                           |
|-------|-----------|-----|-----------------------------------------------------------------------|
| 0     | TSFCMPNM  | R/W | Transfer Complete Normally Mask<br>0: Mask<br>1: Not mask             |
| 1     | TSFCMPANM | R/W | Transfer Complete Abnormally Mask<br>0: Mask<br>1: Not mask           |
| 2     | Reserved  |     |                                                                       |
| 3     | RXSTALLM  | R/W | STALL Response Received Interrupt Mask<br>0: Mask<br>1: Not mask      |
| 4     | RXNAKM    | R/W | NAK Response Received Interrupt Mask<br>0: Mask<br>1: Not mask        |
| 5     | RXTXACKM  | R/W | ACK Response Received/Transmitted Interrupt<br>0: Mask<br>1: Not mask |
| 6     | RXNYETM   | R/W | NYET Response Received Interrupt Mask<br>0: Mask<br>1: Not mask       |
| 7     | TERRM     | R/W | Transaction Error Mask<br>0: Mask<br>1: Not mask                      |
| 8     | BABBLEM   | R/W | Babble Error Mask<br>0: Mask<br>1: Not mask                           |
| 9     | FOVRM     | R/W | Frame Overrun Error Mask<br>0: Mask<br>1: Not mask                    |
| 10    | DTOGM     | R/W | Data Toggle Error Mask<br>0: Mask<br>1: Not mask                      |
| 31:11 | Reserved  |     |                                                                       |

### 26.5.11 Full-speed OTG host channel-X transmission size register (OTG\_FS\_HCHTSIZEX) (X=0...7)

Offset address: 0x510+20\*X

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                              |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18:0  | TSFSIZE  | R/W | Transfer Size <ul style="list-style-type: none"> <li>For IN: The value of this bit is the size reserved for the transmission buffer, which is generally an integer multiple of the maximum data packet.</li> <li>For OUT: The value of this bit determines the number of bytes to be transmitted by the host.</li> </ul> |
| 28:19 | PCKTCNT  | R/W | Packet Count<br>This bit indicates the value of the transmitted or received data packet. For each data packet transmitted, the value of this bit decreases by 1. When it decreases to 0, it means that the transmission is completed.                                                                                    |
| 30:29 | DATAPID  | R/W | Data PID<br>This bit is initial PID of data communication.<br>00: DATA0<br>01: DATA2<br>10: DATA1<br>11: MDATA (controlled transmission)/SETUP (uncontrolled transmission)                                                                                                                                               |
| 31    | Reserved |     |                                                                                                                                                                                                                                                                                                                          |

## 26.6 OTG\_FS device mode register address mapping

Table 130 OTG\_FS Device Mode Register Address Mapping

| Register name    | Description                                                          | Offset address |
|------------------|----------------------------------------------------------------------|----------------|
| OTG_FS_DCFG      | Full-speed OTG device configuration register                         | 0x800          |
| OTG_FS_DCTRL     | Full-speed OTG device control register                               | 0x804          |
| OTG_FS_DSTS      | Full-speed OTG device state register                                 | 0x808          |
| OTG_FS_DINIMASK  | Full-speed OTG device IN endpoint interrupt mask register            | 0x810          |
| OTG_FS_DOUTIMASK | Full-speed OTG device OUT endpoint interrupt mask register           | 0x814          |
| OTG_FS_DAEPINT   | Full-speed OTG device all-endpoint interrupt register                | 0x818          |
| OTG_FS_DAEPIMASK | Full-speed OTG device all-endpoint interrupt mask register           | 0x81C          |
| OTG_FS_DVBUSDTIM | Full-speed OTG device VBUS release time register                     | 0x828          |
| OTG_FS_DVBUSPTIM | Full-speed OTG device VBUS pulse time register                       | 0x82C          |
| OTG_FS_DIEIMASK  | Full-speed OTG device IN endpoint FIFO empty interrupt mask register | 0x834          |

| Register name    | Description                                                               | Offset address |
|------------------|---------------------------------------------------------------------------|----------------|
| OTG_FS_DIEPCTRL0 | Full-speed OTG device IN endpoint 0 control register                      | 0x900          |
| OTG_FS_DIEPCTRLx | Full-speed OTG device IN endpoint x control register                      | 0x900+20x      |
| OTG_FS_DIEPINTx  | Full-speed OTG device IN endpoint x interrupt register<br>(x=0...3)       | 0x908+20x      |
| OTG_FS_DIEPTRS0  | Full-speed OTG device IN endpoint 0 transmission size register            | 0x910          |
| OTG_FS_DIEPTRSx  | Full-speed OTG device IN endpoint x transmission size register (x=1...3)  | 0x910+20x      |
| OTG_FS_DITXFSTSx | Full-speed OTG device IN endpoint x TXFIFO state register (x=0...3)       | 0x918+20x      |
| OTG_FS_DOEPCTRL0 | Full-speed OTG device OUT endpoint 0 control register                     | 0xB00          |
| OTG_FS_DOEPCTRLx | Full-speed OTG device OUT endpoint x control register<br>(x=1...3)        | 0xB00+20x      |
| OTG_FS_DOEPINTx  | Full-speed OTG device OUT endpoint x interrupt register (x=0...3)         | 0xB08+20x      |
| OTG_FS_DOEPTRS0  | Full-speed OTG device OUT endpoint 0 transmission size register           | 0xB10          |
| OTG_FS_DOEPTRSx  | Full-speed OTG device OUT endpoint x transmission size register (x=1...3) | 0xB10+20x      |
| OTG_FS_PCGCTRL   | Full-speed OTG power and clock gating control register                    | 0xE00          |

## 26.7 OTG\_FS device mode register functional description

### 26.7.1 Full-speed OTG device configuration register (OTG\_FS\_DCFG)

Offset address: 0x800

Reset value: 0x0220 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | DSPDSEL  | R/W | Device Speed Select<br>This bit selects the maximum enumeration speed of the device connected to the host,<br>11: FS (48MHz)<br>Others: Reserved                                                                                                                                                                                           |
| 2     | SENDOUT  | R/W | Transmit the Received OUT Packet on Nonzero-length Status<br>0: After receiving the OUT data packet, transmit the data packet to the application program, and reply the handshake signal according to the NAK and STALL bits of the endpoint<br>1: After receiving the OUT data packet (non-zero length), reply the STALL handshake signal |
| 3     | Reserved |     |                                                                                                                                                                                                                                                                                                                                            |
| 10:4  | DADDR    | R/W | Device Address<br>This bit is the address of storage device, and the parameters are from SetAddress command.                                                                                                                                                                                                                               |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12:11 | PFITV    | R/W | <p>Periodic (Micro) Frame Interval</p> <p>This bit is configured to determine the time point of the periodic frame interrupt program, and can determine whether the synchronous communication of the frame is completed.</p> <p>00: 80% of frame interval<br/> 01: 85% of frame interval<br/> 10: 90% of frame interval<br/> 11: 95% of frame interval</p> |
| 31:13 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                            |

## 26.7.2 Full-speed OTG device control register (OTG\_FS\_DCTRL)

Offset address: 0x804

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                 |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | RWKUPS   | R/W | <p>Remote Wakeup Signaling</p> <p>The program wakes up the USB host by setting this bit to 1 to make the module exit the suspended state.</p> <p>Note: According to the agreement, after this bit is set to 1, it should be cleared to 0 within 1~15ms.</p> |
| 1     | SDCNNT   | R/W | <p>Soft Disconnect</p> <p>Soft disconnect means that the host cannot receive the signal of "Device connected", and the device cannot receive the signal.</p> <p>0: Normal. The host can receive device connection event<br/> 1: Soft disconnection</p>      |
| 2     | GINAKSTS | R   | <p>Global IN NAK Status</p> <p>This bit determines whether to reply the handshake signal according to the data availability in TXFIFO.</p> <p>0: Yes<br/> 1: No, all non-periodic IN endpoints reply handshake signal</p>                                   |
| 3     | GONAKSTS | R   | <p>Global OUT NAK Status</p> <p>0: Transmit the handshake signal according to FIFO state and NAK and STALL bit state<br/> 1: No data is received, and all data packets except the SETUP transaction reply the NAK signal</p>                                |
| 6:4   | TESTSEL  | R/W | <p>Test Mode Select</p> <p>000: Disable the test<br/> 001: Test_J<br/> 010: Test_K<br/> 011: Test_SE0_NAK<br/> 100: Test_Packet<br/> 101: Test_Force_Enable<br/> Others: Reserved</p>                                                                       |
| 7     | GINAKSET | W   | <p>Global IN NAK Setup</p> <p>Set the global non-periodic IN NAK to 1 to make the non-periodic IN endpoint transmit NAK signal.</p> <p>This bit can be set to 1 only when GINNPNAKE bit of OTG_FS_GCINT register is cleared to 0.</p>                       |

| Field | Name      | R/W | Description                                                                                                                                                                              |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8     | GINAKCLR  | W   | Global IN NAK Clear<br>Clear the global non-periodic IN NAK to 0.                                                                                                                        |
| 9     | GONAKSET  | W   | Global OUT NAK Setup<br>Set the global OUT NAK to 1 to make OUT endpoint transmit NAK signal.<br>This bit can be set to 1 only when GONAKE bit of OTG_FS_GCINT register is cleared to 0. |
| 10    | GONAKCLR  | W   | Global OUT NAK Clear<br>Clear the global OUT NAK to 0.                                                                                                                                   |
| 11    | POPROGCMP | R/W | Power-on Programming Complete<br>This bit indicates that the programming operation is completed after the register is awakened.                                                          |
| 31:12 | Reserved  |     |                                                                                                                                                                                          |

### 26.7.3 Full-speed OTG device state register (OTG\_FS\_DSTS)

Offset address: 0x808

Reset value: 0x0000 0010

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                       |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | SUSSTS   | R   | Suspend Status<br>When the USB bus has been idle for more than 3ms, the module will enter the suspended state, and this bit will be set to 1. When there is an activity on the USB line or the module receives a remote wake-up signal, the module will exit the suspended state. |
| 2:1   | ENUMSPD  | R   | Enumerated Speed<br>Enumeration speed of full-speed OTG after chirp sequence detection.<br>11: Full speed (48MHz)<br>Others: Reserved                                                                                                                                             |
| 3     | ERTERR   | R   | Erratic Error<br>If any irregular error occurs, this bit will be set to 1. At this time, communication can be resumed only by performing soft disconnection.                                                                                                                      |
| 7:4   | Reserved |     |                                                                                                                                                                                                                                                                                   |
| 21:8  | SOFNUM   | R   | Frame Number of the Received SOF                                                                                                                                                                                                                                                  |
| 31:22 | Reserved |     |                                                                                                                                                                                                                                                                                   |

### 26.7.4 Full-speed OTG device IN endpoint interrupt mask register (OTG\_FS\_DINIMASK)

Offset address: 0x810

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                 |
|-------|---------|-----|-------------------------------------------------------------|
| 0     | TSFCMPM | R/W | Transfer Completed Interrupt Mask<br>0: Mask<br>1: Not mask |

| Field | Name     | R/W | Description                                                             |
|-------|----------|-----|-------------------------------------------------------------------------|
| 1     | EPDISM   | R/W | Endpoint Disable Interrupt Mask<br>0: Mask<br>1: Not mask               |
| 2     | Reserved |     |                                                                         |
| 3     | TOM      | R/W | Timeout Interrupt Mask<br>0: Mask<br>1: Not mask                        |
| 4     | ITXEMPM  | R/W | IN Token Received when Tx FIFO Empty Mask<br>0: Mask<br>1: Not mask     |
| 5     | IEPMMM   | R/W | IN Token Received with Endpoint Mismatch Mask<br>0: Mask<br>1: Not mask |
| 6     | IEPNAKEM | R/W | IN Endpoint NAK Effective Mask<br>0: Mask<br>1: Not mask                |
| 31:7  | Reserved |     |                                                                         |

### 26.7.5 Full-speed OTG device OUT endpoint interrupt mask register (OTG\_FS\_DOUTIMASK)

Offset address: 0x814

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                              |
|-------|----------|-----|--------------------------------------------------------------------------|
| 0     | TSFCMPM  | R/W | Transfer Completed Interrupt Mask<br>0: Mask<br>1: Not mask              |
| 1     | EPDISM   | R/W | Endpoint Disable Interrupt Mask<br>0: Mask<br>1: Not mask                |
| 2     | Reserved |     |                                                                          |
| 3     | SETPCMPM | R/W | SETUP Phase Complete Mask<br>0: Mask<br>1: Not mask                      |
| 4     | OTXEMPM  | R/W | OUT Token Received when Endpoint Disabled Mask<br>0: Mask<br>1: Not mask |
| 31:5  | Reserved |     |                                                                          |

### 26.7.6 Full-speed OTG device all-endpoint interrupt register (OTG\_FS\_DAEPINT)

Offset address: 0x818

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                  |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------|
| 15:0  | INEPINT  | R   | All IN Endpoint Interrupts<br>No. X bit indicates interrupt of IN endpoint X. Up to 16 IN endpoints.         |
| 31:16 | OUTEPINT | R   | All OUT Endpoint Interrupts<br>No. X bit indicates interrupt of OUT endpoint (X-16). Up to 16 OUT endpoints. |

### 26.7.7 Full-speed OTG device all-endpoint interrupt mask register (OTG\_FS\_DAEPIMASK)

Offset address: 0x81C

Reset value: 0x0000 0000

| Field | Name  | R/W | Description                                                                                                                                      |
|-------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | AINM  | R/W | All IN Endpoint Interrupts Mask<br>No. X bit indicates interrupt mask of IN endpoint X. Up to 16 IN endpoints.<br>0: Mask<br>1: Not mask         |
| 31:16 | AOUTM | R/W | All OUT Endpoint Interrupts Mask<br>No. X bit indicates interrupt mask of OUT endpoint (X-16). Up to 16 OUT endpoints.<br>0: Mask<br>1: Not mask |

### 26.7.8 Full-speed OTG device V<sub>BUS</sub> release time register (OTG\_FS\_DVBUSDTIM)

Offset address: 0x828

Reset value: 0x0000 17D7

| Field | Name     | R/W | Description                                                                                                                                                    |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | VBUSDTIM | R/W | Device V <sub>BUS</sub> Discharge Time<br>Discharge time after V <sub>BUS</sub> impulses during SRP period.<br>Value=Discharge time (number of PHY clock)/1024 |
| 31:16 | Reserved |     |                                                                                                                                                                |

### 26.7.9 Full-speed OTG device V<sub>BUS</sub> pulse time register (OTG\_FS\_DVBUSPTIM)

Offset address: 0x82C

Reset value: 0x0000 05B8

| Field | Name     | R/W | Description                                                                                                                    |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------|
| 11:0  | VBUSPTIM | R/W | Device V <sub>BUS</sub> Pulsing Time<br>V <sub>BUS</sub> pulse time during SRP.<br>Value=Pulse time (number of PHY clock)/1024 |
| 31:12 | Reserved |     |                                                                                                                                |



### 26.7.10 Full-speed OTG device IN endpoint FIFO empty interrupt mask register (OTG\_FS\_DIEIMASK)

Offset address: 0x834

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                            |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | INEM     | R/W | IN Endpoint Tx FIFO Empty Interrupt Mask<br>No. X bit indicates TXFE interrupt mask of IN endpoint X. Up to 16 IN endpoints.<br>0: Mask<br>1: Not mask |
| 31:16 | Reserved |     |                                                                                                                                                        |

### 26.7.11 Full-speed OTG device IN endpoint 0 control register (OTG\_FS\_DIEPCTRL0)

Offset address: 0x900

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | MAXPS    | R/W | Maximum Packet Size<br>This bit configures the maximum data packet size of endpoint.<br>00: 64 bytes<br>01: 32 bytes<br>10: 16 bytes<br>11: 8 bytes                                                                                                        |
| 14:2  | Reserved |     |                                                                                                                                                                                                                                                            |
| 15    | USBAEP   | R   | USB Active Endpoint<br>This bit indicates whether the endpoint is activated in the current configuration and interface.<br>This bit is always set to 1.                                                                                                    |
| 16    | Reserved |     |                                                                                                                                                                                                                                                            |
| 17    | NAKSTS   | R   | NAK Status<br>0: The module replies non-NAK handshake signal according to the FIFO state<br>1: The module replies the NAK handshake signal on this endpoint. At this time, even if there is space in TXFIFO, the module will still stop transmitting data. |
| 19:18 | EPTYPE   | R   | Endpoint Type<br>This bit is set to 00 by hardware, indicating control type of the endpoint.                                                                                                                                                               |
| 20    | Reserved |     |                                                                                                                                                                                                                                                            |
| 21    | STALLH   | R/S | STALL Handshake<br>The program can only set this bit to 1 and when the endpoint receives the SETUP token, this bit will be cleared to 0. The priority of STALL is higher than that of NAK.                                                                 |
| 25:22 | TXFNUM   | R/W | TXFIFO Number<br>Set a separate FIFO number for IN endpoint 0.                                                                                                                                                                                             |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                        |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26    | NAKCLR   | W   | NAK Clear<br>When performing write operation to this bit, the NAK bit of the endpoint 0 will be cleared to 0.                                                                                                                                                                                                      |
| 27    | NAKSET   | W   | NAK Set<br>When performing write operation to this bit, the NAK bit will be set to 1.                                                                                                                                                                                                                              |
| 29:28 | Reserved |     |                                                                                                                                                                                                                                                                                                                    |
| 30    | EPDIS    | R   | Endpoint Disable<br>Data transmission on the endpoint can be stopped by setting this bit to 1.<br>This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.                                                                   |
| 31    | EPEN     | R   | Endpoint Enable<br>After this bit is set to 1, the endpoint will start to transmit data.<br>When any of the following interrupts is triggered, this bit will be cleared to 0:<br><ul style="list-style-type: none"> <li>● SETUP completed</li> <li>● Disable endpoint</li> <li>● Transmission completed</li> </ul> |

### 26.7.12 Full-speed OTG device IN endpoint x control register (OTG\_FS\_DIEPCTRLx) (x=1~3, endpoint number)

Offset address: 0x900+0x20\*x; x=1~3

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10:0  | MAXPS    | R/W | Maximum Packet Size<br>This bit configures the maximum data packet size of endpoint (in byte).                                                                                                                                                                                                                                                  |
| 14:11 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                 |
| 15    | USBAEP   | R/W | USB Active Endpoint<br>This bit indicates whether the endpoint is activated in the current configuration and interface.<br>After USB is reset, this bit will be cleared to 0 (except endpoint 0).                                                                                                                                               |
| 16    | EOF_PID  | R   | Even Odd Frame<br>This bit is used to indicate the frame number transmitted/received by the endpoint (for synchronization IN) or the PID of data packet (for interrupt/batch IN).<br>Used for synchronous IN endpoints:<br>0: Even frame<br>1: Odd frame<br>Endpoint Data PID<br>Used for interrupt/batch IN endpoints:<br>0: DATA0<br>1: DATA1 |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17    | NAKSTS   | R     | <p>NAK Status</p> <p>0: The module replies non-NAK handshake signal according to the FIFO state</p> <p>1: The module replies to the NAK handshake signal on this endpoint; at this time, for asynchronous IN: even if there is data available in TXFIFO, the module will still stop transmitting data; for synchronous IN, the module will transmit zero-length data packet even if there is data available in TXFIFO</p> <p>Note: The module always responds to the SETUP data packet through ACK handshake.</p> |
| 19:18 | EPTYPE   | R/W   | <p>Endpoint Type</p> <p>00: Control</p> <p>01: Synchronous</p> <p>10: Batch</p> <p>11: Interrupt</p>                                                                                                                                                                                                                                                                                                                                                                                                              |
| 20    | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 21    | STALLH   | RW/RS | <p>STALL Handshake</p> <ul style="list-style-type: none"> <li>For uncontrolled and non-synchronous IN endpoints (read/write mode is R/W):<br/>When this bit is set to 1, the device will reply STALL to all tokens from the USB host. This bit can only be cleared to 0 by software.</li> <li>Used for control endpoints (read/write mode is R/W):<br/>When this bit is set to 1, it means that the module receives SETUP token.</li> </ul>                                                                       |
| 25:22 | TXFNUM   | R/W   | <p>TXFIFO Number</p> <p>These bits indicate the FIFO number associated with the endpoint, and a separate FIFO number needs to be set for each valid IN endpoint</p>                                                                                                                                                                                                                                                                                                                                               |
| 26    | NAKCLR   | W     | <p>NAK Clear</p> <p>When performing write operation to this bit, the NAK bit of the endpoint will be cleared to 0.</p>                                                                                                                                                                                                                                                                                                                                                                                            |
| 27    | NAKSET   | W     | <p>NAK Set</p> <p>When performing write operation to this bit, the NAK bit of the endpoint will be set to 1.</p> <p>This bit can control the transmission of NAK handshake signal.</p>                                                                                                                                                                                                                                                                                                                            |
| 28    | DPIDSET  | W     | <p>DATA0 PID Set</p> <ul style="list-style-type: none"> <li>Used for interrupt/batch IN endpoints:<br/>When performing write operation to this bit, PID will be set to DATA0.</li> </ul> <p>Even Frame Set</p> <ul style="list-style-type: none"> <li>Used for synchronous IN endpoints:<br/>When performing write operation to this bit, EOF_PID will be set to even frame.</li> </ul>                                                                                                                           |
| 29    | OFFSET   | W     | <p>Odd Frame Set</p> <p>It is used for synchronous IN endpoints. When performing write operation to this bit, EOF_PID will be set to odd frame.</p>                                                                                                                                                                                                                                                                                                                                                               |

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                        |
|-------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30    | EPDIS | R/S | Endpoint Disable<br>Data transmission on the endpoint can be stopped by setting this bit to 1.<br>This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.                                                                   |
| 31    | EPEN  | R/S | Endpoint Enable<br>After this bit is set to 1, the endpoint will start to transmit data.<br>When any of the following interrupts is triggered, this bit will be cleared to 0:<br><ul style="list-style-type: none"> <li>• SETUP completed</li> <li>• Disable endpoint</li> <li>• Transmission completed</li> </ul> |

### 26.7.13 Full-speed OTG device IN endpoint x interrupt register (OTG\_FS\_DIEPINTx) (x=0~3, endpoint number)

Offset address: 0x908+0x20\*x; x=0~3

Reset value: 0x0000 0080

Read this register when ONEP bit of OTG\_FS\_GCINT register is set to 1;

Read OTG\_FS\_DAEPIINT register to obtain the accurate endpoint number of the device endpoint x interrupt register, and then read the register; only when the corresponding bit of the register is cleared to 0, can the corresponding bit of OTG\_FS\_DAEPIINT register and OTG\_FS\_GCINT register be cleared to 0.

| Field | Name     | R/W   | Description                                                                                                                                                                                                                     |
|-------|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TSFCMP   | RC_W1 | Transfer Complete Interrupt<br>This bit indicates that the transmission on the endpoint has been completed.                                                                                                                     |
| 1     | EPDIS    | RC_W1 | Endpoint Interrupt Disable<br>This bit means that the endpoint is disabled.                                                                                                                                                     |
| 2     | Reserved |       |                                                                                                                                                                                                                                 |
| 3     | TO       | RC_W1 | Timeout Interrupt<br>This bit is only applicable to the control IN endpoints, indicating that the response to the recently received IN token has timed out.                                                                     |
| 4     | ITXEMP   | RC_W1 | Receive IN Token Interrupt when FIFO is empty<br>This bit is only applicable to non-periodic IN endpoints, indicating that IN token is received when the corresponding TXFIFO of the endpoint is empty.                         |
| 5     | Reserved |       |                                                                                                                                                                                                                                 |
| 6     | IEPNAKE  | RC_W1 | IN Endpoint NAK Effective<br>This bit indicates that the module samples NAK, namely, the NAK bit of the IN endpoint has taken effect.<br>This bit will be cleared to 0 when NAKCLR bit of OTG_FS_DIEPCTRLx register is written. |
| 7     | TXFE     | R     | TXFIFO Empty Interrupt<br>The interrupt will be generated when TXFIFO of this endpoint is empty.                                                                                                                                |

| Field | Name | R/W | Description |
|-------|------|-----|-------------|
| 31:8  |      |     | Reserved    |

#### 26.7.14 Full-speed OTG device IN endpoint 0 transmission size register (OTG\_FS\_DIEPTRS0)

Offset address: 0x910

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG\_FS\_DIEPCTRLx register is set to 1; this register can be read only when EPEN bit of OTG\_FS\_DIEPCTRLx register is cleared to 0

| Field | Name   | R/W | Description                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------|
| 6:0   | EPTRS  | R/W | Endpoint Transfer Size<br>This bit indicates the data size contained by endpoint 0 in one data transmission.             |
| 18:7  |        |     | Reserved                                                                                                                 |
| 20:19 | EPPCNT | R/W | Endpoint Packet Count<br>This bit indicates the number of data packets contained by endpoint 0 in one data transmission. |
| 31:21 |        |     | Reserved                                                                                                                 |

#### 26.7.15 Full-speed OTG device IN endpoint x transmission size register (OTG\_FS\_DIEPTRSx) (x=1~3, endpoint number)

Offset address: 0x910+0x20\*x; x=1~3

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG\_FS\_DIEPCTRLx register is set to 1; this register can be read only when EPEN bit of OTG\_FS\_DIEPCTRLx register is cleared to 0

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                     |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18:0  | EPTRS  | R/W | Endpoint Transfer Size<br>This bit indicates the data size contained by endpoint x in one data transmission (in byte).                                                                                                                                                                                                          |
| 28:19 | EPPCNT | R/W | Endpoint Packet Count<br>This bit indicates the number of data packets contained by endpoint x in one data transmission.                                                                                                                                                                                                        |
| 30:29 | TXDCNT | R/W | Transmit Packet Count <ul style="list-style-type: none"> <li>For periodic IN endpoints, this bit indicates the number of data packets that must be transmitted per frame on USB.</li> <li>For the calculation synchronization IN endpoint, this bit calculates the data PID of the endpoint.</li> </ul> 01: 1<br>10: 2<br>11: 3 |
| 31    |        |     | Reserved                                                                                                                                                                                                                                                                                                                        |

### 26.7.16 Full-speed OTG device IN endpoint x TXFIFO state register (OTG\_FS\_DITXFSTx) (x=0~3, endpoint number)

Offset address: 0x918+0x20\*x; x=0~3

| Field | Name      | R/W | Description                                                                                                                                                                                                                                          |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | INEPTXFSA | R   | IN Endpoint TXFIFO Space Available<br>This bit indicates the available space of the IN endpoint TXFIFO (in word).<br>0x0: IN endpoint TXFIFO is full<br>0x1: 1 byte<br>0x2: 2 bytes<br>0xn: n bytes are available (0<n<512)<br>Other value: Reserved |
| 31:16 | Reserved  |     |                                                                                                                                                                                                                                                      |

### 26.7.17 Full-speed OTG device OUT endpoint 0 control register (OTG\_FS\_DOEPCTRL0)

Offset address: 0xB00

Reset value: 0x0000 8000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                             |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | MAXPS    | R   | Maximum Packet Size<br>This bit configures the maximum data packet size of endpoint.<br>00: 64 bytes<br>01: 32 bytes<br>10: 16 bytes<br>11: 8 bytes                                                                                                     |
| 14:2  | Reserved |     |                                                                                                                                                                                                                                                         |
| 15    | USBAEP   | R   | USB Active Endpoint<br>This bit indicates whether the endpoint is activated in the current configuration and interface.<br>This bit is always set to 1.                                                                                                 |
| 16    | Reserved |     |                                                                                                                                                                                                                                                         |
| 17    | NAKSTS   | R   | NAK Status<br>0: The module replies non-NAK handshake signal according to the FIFO state<br>1: The module replies the NAK handshake signal on this endpoint. At this time, even if there is space in RXFIFO, the module will still stop receiving data. |
| 19:18 | EPTYPE   | R   | Endpoint Type<br>This bit is set to 00 by hardware, indicating control type of the endpoint.                                                                                                                                                            |
| 20    | SNMEN    | R/W | Snoop Mode Enable<br>In snoop mode, the correctness of OUT data packets is not checked before they are transmitted to the storage area.                                                                                                                 |
| 21    | STALLH   | R/S | STALL Handshake<br>The program can only set this bit to 1 and when the endpoint receives the SETUP token, this bit will be cleared to 0. The priority of STALL is higher than that of NAK.                                                              |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:22 | Reserved |     |                                                                                                                                                                                                                                                                                                                 |
| 26    | NAKCLR   | W   | NAK Clear<br>When performing write operation to this bit, the NAK bit of the endpoint 0 will be cleared to 0.                                                                                                                                                                                                   |
| 27    | NAKSET   | W   | NAK Set<br>When performing write operation to this bit, the NAK bit will be set to 1.                                                                                                                                                                                                                           |
| 29:28 | Reserved |     |                                                                                                                                                                                                                                                                                                                 |
| 30    | EPDIS    | R   | Endpoint Disable<br>Data transmission on the endpoint can be stopped by setting this bit to 1. This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.                                                                   |
| 31    | EPEN     | W   | Endpoint Enable<br>After this bit is set to 1, the endpoint will start to transmit data. When any of the following interrupts is triggered, this bit will be cleared to 0:<br><ul style="list-style-type: none"> <li>● SETUP completed</li> <li>● Disable endpoint</li> <li>● Transmission completed</li> </ul> |

### 26.7.18 Full-speed OTG device OUT endpoint x control register (OTG\_FS\_DOEPCTRLx) (x=1~3, endpoint number)

Offset address: 0xB00+0x20\*x; x=1~3

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10:0  | MAXPS    | R/W | Maximum Packet Size<br>This bit configures the maximum data packet size of endpoint. (in byte).                                                                                                                                                                                                                                                 |
| 14:11 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                 |
| 15    | USBAEP   | R/W | USB Active Endpoint<br>This bit indicates whether the endpoint is activated in the current configuration and interface.<br>After USB is reset, this bit will be cleared to 0 (except endpoint 0).                                                                                                                                               |
| 16    | EOF_PID  | R   | Even Odd Frame<br>This bit is used to indicate the frame number transmitted/received by the endpoint (for synchronization IN) or the PID of data packet (for interrupt/batch IN).<br>Used for synchronous IN endpoints:<br>0: Even frame<br>1: Odd frame<br>Endpoint Data PID<br>Used for interrupt/batch IN endpoints:<br>0: DATA0<br>1: DATA1 |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17    | NAKSTS   | R     | <p>NAK Status</p> <p>0: The module replies non-NAK handshake signal according to the FIFO state</p> <p>1: The module replies the NAK handshake signal on this endpoint. At this time, for OUT endpoint, even if there is remaining space in RXFIFO, the module will still stop receiving data</p> <p>Note: The module always responds to the SETUP data packet through ACK handshake.</p>                                                                                                  |
| 19:18 | EPTYPE   | R/W   | <p>Endpoint Type</p> <p>00: Control</p> <p>01: Synchronous</p> <p>10: Batch</p> <p>11: Interrupt</p>                                                                                                                                                                                                                                                                                                                                                                                       |
| 20    | SNMEN    | R/W   | <p>Snoop Mode Enable</p> <p>In snoop mode, the correctness of OUT data packets is not checked before they are transmitted to the storage area.</p>                                                                                                                                                                                                                                                                                                                                         |
| 21    | STALLH   | RW/RS | <p>STALL Handshake</p> <ul style="list-style-type: none"> <li>For uncontrolled and non-synchronous IN endpoints (read/write mode is R/W):</li> </ul> <p>When this bit is set to 1, the device will reply STALL to all tokens from the USB host. This bit can only be cleared to 0 by software.</p> <ul style="list-style-type: none"> <li>Used for control endpoints (read/write mode is R/W):</li> </ul> <p>When this bit is set to 1, it means that the module receives SETUP token.</p> |
| 25:22 | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 26    | NAKCLR   | W     | <p>NAK Clear</p> <p>When performing write operation to this bit, the NAK bit of the endpoint will be cleared to 0.</p>                                                                                                                                                                                                                                                                                                                                                                     |
| 27    | NAKSET   | W     | <p>NAK Set</p> <p>When performing write operation to this bit, the NAK bit of the endpoint will be set to 1.</p> <p>This bit can control the transmission of NAK handshake signal.</p>                                                                                                                                                                                                                                                                                                     |
| 28    | DPIDSET  | W     | <p>DATA0 PID Set</p> <ul style="list-style-type: none"> <li>Used for interrupt/batch IN endpoints:</li> </ul> <p>When performing write operation to this bit, PID will be set to DATA0.</p> <p>Even Frame Set</p> <ul style="list-style-type: none"> <li>Used for synchronous IN endpoints:</li> </ul> <p>When performing write operation to this bit, EOF_PID will be set to even frame.</p>                                                                                              |



| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                        |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | OFFSET | W   | Odd Frame Set <ul style="list-style-type: none"> <li>Used for synchronous OUT endpoints:<br/>When performing write operation to this bit, EOF_PID will be set to odd frame.</li> <li>Used for interrupt/batch OUT endpoints:<br/>When performing write operation to this bit, PID will be set to DATA1.</li> </ul> |
| 30    | EPDIS  | R/S | Endpoint Disable<br>Data transmission on the endpoint can be stopped by setting this bit to 1.<br>This bit needs to be cleared to 0 before the endpoint disable interrupt bit is set to 1; this bit can only be set to 1 after EPEN is set to 1.                                                                   |
| 31    | EPEN   | R/S | Endpoint Enable<br>After this bit is set to 1, the endpoint will start to transmit data.<br>When any of the following interrupts is triggered, this bit will be cleared to 0: <ul style="list-style-type: none"> <li>SETUP completed</li> <li>Disable endpoint</li> <li>Transmission completed</li> </ul>          |

### 26.7.19 Full-speed OTG device OUT endpoint x interrupt register (OTG\_FS\_DOEPINTx) (x=0~3, endpoint number)

Offset address: 0xB08+0x20\*x; x=0~3

Reset value: 0x0000 0080

Read this register when ONEP bit of OTG\_FS\_GCINT register is set to 1;

Read OTG\_FS\_DAEPINTx register to obtain the accurate endpoint number of the device endpoint x interrupt register, and then read the register; only when the corresponding bit of the register is cleared to 0, can the corresponding bit of OTG\_FS\_DAEPINT register and OTG\_FS\_GCINT register be cleared to 0.

| Field | Name     | R/W   | Description                                                                                                                                                                                                             |
|-------|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TSFCMP   | RC_W1 | Transfer Complete Interrupt<br>This bit indicates that the transmission on the endpoint has been completed.                                                                                                             |
| 1     | EPDIS    | RC_W1 | Endpoint Interrupt Disable<br>This bit means that the endpoint is disabled.                                                                                                                                             |
| 2     | Reserved |       |                                                                                                                                                                                                                         |
| 3     | SETPCMP  | RC_W1 | SETUP Phase Complete Interrupt<br>This bit is only applicable to the control OUT endpoint, indicating that the SETUP phase has been completed. After an interrupt is generated, the received SETUP data can be decoded. |
| 4     | RXOTDIS  | RC_W1 | Receive OUT Token When Disable Interrupt<br>This bit is only applicable to the control OUT endpoint, indicating that the OUT token is received without enabling the endpoint.                                           |

| Field | Name     | R/W   | Description                                                                                                                                                                                       |
|-------|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5     | Reserved |       |                                                                                                                                                                                                   |
| 6     | RXBSP    | RC_W1 | Receive Back-to-Back SETUP Packet Interrupt<br>This bit is only applicable to the control OUT endpoint, indicating that the endpoint has received more than three consecutive SETUP data packets. |
| 31:7  | Reserved |       |                                                                                                                                                                                                   |

### 26.7.20 Full-speed OTG device OUT endpoint 0 transmission size register (OTG\_FS\_DOEPTRS0)

Offset address: 0xB10

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG\_FS\_DOEPTCTRLx register is set to 1; this register can be read only after EPEN bit of OTG\_FS\_DOEPTCTRLx register is cleared to 0

| Field | Name     | R/W | Description                                                                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------|
| 6:0   | EPTRS    | R/W | Endpoint Transfer Size<br>This bit indicates the data size contained by endpoint 0 in one data transmission (in byte).                 |
| 18:7  | Reserved |     |                                                                                                                                        |
| 19    | EPPCNT   | R/W | Endpoint Packet Count<br>This bit will decrease to 0 after RXFIFO is written to a data packet.                                         |
| 28:20 | Reserved |     |                                                                                                                                        |
| 30:29 | SPCNT    | R/W | SETUP Packet Count<br>These bits indicate the number of SETUP dat packets that can be received continuously<br>01: 1<br>10: 2<br>11: 3 |
| 31    | Reserved |     |                                                                                                                                        |

### 26.7.21 Full-speed OTG device OUT endpoint x transmission size register (OTG\_FS\_DOEPTRS) (x=1~3, endpoint number)

Offset address: 0xB10+0x20\*x; x=1~3

Reset value: 0x0000 0000

This register can be modified only after EPEN bit of OTG\_FS\_DOEPTCTRLx register is set to 1; this register can be read only after EPEN bit of OTG\_FS\_DOEPTCTRLx register is cleared to 0

| Field | Name  | R/W | Description                                                                                                            |
|-------|-------|-----|------------------------------------------------------------------------------------------------------------------------|
| 18:0  | EPTRS | R/W | Endpoint Transfer Size<br>This bit indicates the data size contained by endpoint x in one data transmission (in byte). |

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28:19 | EPPCNT    | R/W | Endpoint Packet Count<br>This bit indicates the number of data packets contained by endpoint x in one data transmission.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 30:29 | PID_SPCNT | R/W | Receive Data PID or SETUP Packet Count <ul style="list-style-type: none"> <li>For synchronous OUT endpoints, this bit indicates the PID of the last received data packet. <ul style="list-style-type: none"> <li>00: DATA0</li> <li>01: DATA2</li> <li>10: DATA1</li> <li>11: MDATA</li> </ul> </li> <li>For the control OUT endpoint, this bit indicates the number of SETUP data packets that the endpoint can continuously receive. <ul style="list-style-type: none"> <li>01: 1</li> <li>10: 2</li> <li>11: 3</li> </ul> </li> </ul> |
| 31    | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

## 26.7.22 Full-speed OTG power and clock gating control register (OTG\_FS\_PCGCTRL)

Offset address: 0xE00

Reset value: 0x0000 0000

This register is applicable to both master mode and device mode.

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PCLKSTOP | R/W | PHY Clock Stop<br>0: The PHY clock is enabled to start when the USB communication is restored or the session is restarted<br>1: Stop the PHY clock when USB communication is suspended, the session is invalid, or the device is disconnected                                                                                                                                            |
| 1     | GCLK     | R/W | Gate HCLK<br>0: When the USB communication is restored or the session is restarted, it is allowed to stop providing the clock to modules other than AHB bus slave interface, main interface and wake-up<br>1: When the USB communication is suspended or the session is invalid, stop providing the clock for the modules other than AHB bus slave interface, main interface and wake-up |
| 3:2   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                          |
| 4     | PHYSUS   | R/W | PHY Suspend<br>This bit means that PHY is suspended.                                                                                                                                                                                                                                                                                                                                     |
| 31:5  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                          |

## 27 Ethernet

Note: Only APM32F425xG\_F427xG series products have such module.

### 27.1 Introduction

Ethernet provides configurable and flexible peripherals to meet various application requirements of customers. It supports two industry standard interfaces connected to the external physical layer: MII and RMI are used by default, and MII is only defined in IEEE 802.3 specification. It has many application fields, such as switch, network interface card and so on. Ethernet can transmit and receive data according to IEEE 802.3-2002 standard with the help of peripherals.

Ethernet complies with the following standards:

- IEEE802.3-2002 for Ethernet MAC
- IEEE1588-2008 standards which specify synchronization precision of networked clock
- AMBA 2.0 for AHB master/slave ports
- RMII specification of RMII Alliance

### 27.2 Main characteristics of Ethernet

#### 27.2.1 Main characteristics of MAC

- (1) MII interface and PHY communication that conforms to IEEE802.3 specification
- (2) Support 10/100Mbps data transmission rate
- (3) Half-duplex operation
  - Support CSMA/CD protocol
  - Provide back pressure flow control
- (4) Full-duplex operation
  - Support IEEE 802.3x flow control
  - If the flow control input signal disappears, the zero-range pause frame will be automatically transmitted
  - The received pause frame can be forwarded to the user application program
- (5) Insertion of frame data (SFD) in transmit path, and header and frame start data deleted in receive path
- (6) Automatically generate CRC and pad, which can be automatically cleared when receiving frames
- (7) Programmable frame interval

- (8) Programmable frame length; it supports up to 16KB jumbo frame
- (9) Address filter mode
  - Four 48-bit DA address registers; each byte can be masked
  - Three 48-bit SA address registers; each byte can be masked
  - 64-bit Hash filter, applicable to multicast and unicast addresses
  - Can transmit multi-cast address frames
  - Support mixed mode, and can transmit all frames, with network monitoring not filtered
  - A state report will be attached when transmitting incoming data packets
- (10) Independent transmitting, receiving and control interface
- (11) 32-bit data transmitting interface and receiving interface
- (12) Conduct IEEE 802.1Q VLAN variable detection for received frames
- (13) MDIO main interface (optional), used for PHY device configuration and management
- (14) Conduct forced network statistics through RMON/MIB counter
- (15) Detect LAN wake-up frame and AMD Magic Packet™ frame
- (16) Support Ethernet frame timestamp, and each frame gives 64-bit timestamp
- (17) 2KB transmit FIFO of programmable threshold function and 2KB receive FIFO of configurable threshold function
- (18) During multi-frame storage of the receive FIFO, the receiving state vector is inserted into the receive FIFO after EOF transmission, so that the receiving state of these frames will not be stored by the receive FIFO
- (19) In storage and forwarding mode, all error frames will be filtered in receiving process and not be forwarded to the application program
- (20) Generate pulses for lost or damaged frames in the receive FIFO to support data statistics
- (21) Select to forward good frames of small size
- (22) In enhanced receiving, IPv4 header checksum and TCP, UDP or ICMP checksum encapsulated in IPv4 or IPv6 data packets can be checked
- (23) The checksum unloads the received IPv4 and TCP data packets encapsulated by Ethernet frames
- (24) Storage and forwarding mechanism transmitted to MAC

- (25) The pause frame control or back pressure signal to be transmitted to the MAC core is automatically generated according to the receive FIFO filling level
- (26) Handle automatic retransmission of conflict frames during transmission
- (27) Discard frames under excessive collision, delay collision, excessive delay and underflow conditions
- (28) Control and refresh Tx FIFO through software
- (29) Calculate IPv4 header checksum and TCP, UDP or ICMP checksum and insert the frames transmitted in storage and forwarding mode
- (30) Internal loopback through MII during debugging

### **27.2.2 Main characteristics of PTP**

- (1) Timestamp of transmitting and receiving frames
- (2) Coarse calibration and precision calibration
- (3) An interrupt will be triggered when the system time is greater than the target time
- (4) Output second pulse

### **27.2.3 Main characteristics of DMA**

- (1) AHB burst type can be selected at the AHB main interface
- (2) Select address alignment burst from AHB master port
- (3) AHB slave interface supports all AHB burst types
- (4) Double-buffer (buffering ring) or linked list (chain) descriptor link
- (5) Byte aligned addressing supported by data buffer
- (6) Optimize packet-oriented DMA transmission
- (7) Descriptor architecture, which allows transmission of large data blocks with minimal CPU intervention (each descriptor can transmit up to 8KB data)
- (8) Comprehensive state when reporting normal operation and transmission errors
- (9) Size of single programmable burst for transmitting and receiving DMA engine, for optimal host bus
- (10) Programmable interrupt option
- (11) Control transmitting/receiving completion interrupt

- (12) Loop scheduling arbitration or fixed priority arbitration is adopted between the transmitting engine and the receiving engine
- (13) The current Tx/RX descriptor pointer and buffer pointer are used as state registers

## 27.3 Functional description

### 27.3.1 Multiplexing function mapping

The following table displays MAC signal and corresponding MII/RMII signal mapping.

Table 131 Multiplexing Function Mapping

| Port     | AF11                            |
|----------|---------------------------------|
|          | ETH                             |
| PA0-WKUP | ETH_MII_CRS                     |
| PA1      | ETH_MII_RX_CLK/ETH_RMII_REF_CLK |
| PA2      | ETH_MDIO                        |
| PA3      | ETH_MII_COL                     |
| PA7      | ETH_MII_RX_DV/ETH_RMII_CRS_DV   |
| PB0      | ETH_MII_RXD2                    |
| PB1      | ETH_MII_RXD3                    |
| PB5      | ETH_PPS_OUT                     |
| PB8      | ETH_MII_TXD3                    |
| PB10     | ETH_MII_RX_ER                   |
| PB11     | ETH_MII_TX_EN/ETH_RMII_TX_EN    |
| PB12     | ETH_MII_TXD0/ETH_RMII_TXD0      |
| PB13     | ETH_MII_TXD1/ETH_RMII_TXD1      |
| PC1      | ETH_MDC                         |
| PC2      | ETH_MII_TXD2                    |
| PC3      | ETH_MII_TX_CLK                  |
| PC4      | ETH_MII_RXD0/ETH_RMII_RXD0      |
| PC5      | ETH_MII_RXD1/ETH_RMII_RXD1      |

| Port | AF11                         |
|------|------------------------------|
|      | ETH                          |
| PE2  | ETH_MII_TXD3                 |
| PG8  | ETH_PPS_OUT                  |
| PG11 | ETH_MII_TX_EN/ETH_RMII_TX_EN |
| PG13 | ETH_MII_TXD0/ETH_RMII_TXD0   |
| PG14 | ETH_MII_TXD1/ETH_RMII_TXD1   |

### 27.3.2 SMI, MII and RMII

Ethernet peripherals include MAC 802.3 with dedicated DMA controller. It supports MII and RMII used by default and switches them through select bit. It also includes SMI for communicating with external PHY. The mode and function of MAC controller and DMA controller can be selected through a configuration register.

When transmitting data, first transmit the data from the system memory to the TX FIFO buffer through DMA, and then transmit it through the MAC core. The Ethernet frame received through the line is stored by RX FIFO before it is transmitted to the system memory through DMA.

Note: When using Ethernet, the clock frequency of AHB shall be at least 25MHz.

#### 27.3.2.1 Station management interface (SMI)

SMI supports accessing 32 PHY. The application program selects one PHY among the 32 PHY through the 2-wire clock and data line, and then accesses any PHY register. Only one register in one PHY can be addressed at any given time.

Both MDC clock line and MDIO data line are used as multiplexing function I/O in the microcontroller:

- MDC: Periodic clock, which provides reference timing when transmitting data at 2.5MHz. The minimum high/low-level time of MDC is 160ns. The minimum cycle of MDC is 400ns. In idle state, the SMI management interface drives the MDC clock signal to low level.
- MDIO: Data input/output bit stream, which is used to synchronize the transmission state with PHY device through MDC clock signal.

#### SMI frame format



Table 132 Frame Format

| Management frame format |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Header                  | Each operation can be started through the header field, and the header field is used to establish synchronization with the PHY device and corresponds to 32 consecutive logical "1" bits on the MDIO line and 32 cycles on the MDC.                                                                                                                                                                                                                                            |
| Start                   | It is defined by the <01> mode, and used to verify transition of the state of the line from the default logic "1" - logic "0" - logic "1".                                                                                                                                                                                                                                                                                                                                     |
| Operation               | Define the type of ongoing operation.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| PADDR                   | The PHY address has 5 bits, allowing 32 unique PHY addresses. The MSB bit of the address is the first to transmit and receive.                                                                                                                                                                                                                                                                                                                                                 |
| RADDR                   | The register address has 5 bits, and 32 different registers can be addressed in the selected PHY device. The MSB bit of the address is the first to transmit and receive.                                                                                                                                                                                                                                                                                                      |
| TA                      | A 2-bit mode is defined between RADDR and DATA to avoid competition during read operation. When performing read operation, the MAC controller drives two bits of the TA to the high-impedance state on MDIO line. PHY device will drive the first bit of TA to high-impedance state and the second bit to "0".<br>When write operation is performed, the MAC controller will drive the <10> mode for the TA. The PHY device drives two bits of TA to the high-impedance state. |
| Data                    | The data field is 16 bits. Bit 15 of the MAC_DATA register is the first bit.                                                                                                                                                                                                                                                                                                                                                                                                   |
| Idle                    | MDIO line is driven to the high-impedance state. The three-state driver is disabled, and the pull-up resistance of PHY keeps the line in the logic "1" state.                                                                                                                                                                                                                                                                                                                  |

### SMI clock selection

Mac starts management read/write operation. SMI clock is a frequency division clock with AHB clock as clock source. The frequency division factor depends on the clock range set in MAC\_ADDR register.

Table 133 Clock Range

| CR bit      | HCLK clock | MDC clock     |
|-------------|------------|---------------|
| 000         | 60-100MHz  | AHB clock/42  |
| 001         | 100-150MHz | AHB clock/62  |
| 010         | 20-35MHz   | AHB clock/16  |
| 011         | 35-60MHz   | AHB clock/26  |
| 100         | 150-180MHz | AHB clock/102 |
| 101、110、111 | Reserved   | -             |

### SMI write operation

When MB bit and MW bit of MAC\_ADDR are set to 1 by application program, SMI will trigger write operation of PHY register by transmitting PHY address, and register address in PHY, and writing data. When performing write operation, the application program cannot modify MAC\_ADDR and MAC\_DATA registers. After write operation is completed, SMI will reset MB bit.

## SMI read operation

When MB bit of MAC\_ADDR is set and MW bit is cleared to zero, SMI will trigger read operation of PHY register by transmitting PHY address, and register address in PHY. When performing read operation, the application program cannot modify MAC\_ADDR and MAC\_DATA registers. After read operation is completed, SMI will reset MB bit, and update the read data from PHY to MAC\_DATA register.

### 27.3.2.2 Media independent interface (MII)

MII defines the interconnection between MAC sublayer and PHY at data transmission rate of 10 Mbit/s and 100 Mbit/s.

The signals are as follows:

- (1) MII\_TX\_EN: Transmit enable signal; MAC is currently transmitting half byte for MII
- (2) MII\_RX\_DV: Data receiving effective signal; PHY is currently receiving recovered and decoded half byte of MII
- (3) MII\_TXD [3:0]: Data transmitting signal
- (4) MII\_RXD [3:0]: Data receiving signal
- (5) MII\_RX\_ER: Receiving error signal
- (6) MII\_TX\_CLK: Continuous clock signal, providing reference timing for TX data transmission
- (7) MII\_RX\_CLK: Continuous clock signal, providing reference timing for RX data transmission
- (8) MII\_CRD: Carrier sense signal
- (9) MII\_COL: Conflict detection signal

Table 134 TX Interface Signal Encoding

| MII_TX_EN | MII_TXD [3:0] | Description              |
|-----------|---------------|--------------------------|
| 0         | 0000-1111     | Normal frame internal    |
| 1         | 0000-1111     | Normal data transmission |

Table 135 RX Interface Signal Encoding

| MII_RX_DV | MII_RX_ER | MII_RXD [3:0] | Description             |
|-----------|-----------|---------------|-------------------------|
| 0         | 0         | 0000-1111     | Normal frame internal   |
| 0         | 1         | 0000          | Normal frame internal   |
| 0         | 1         | 0001-1101     | Reserved                |
| 0         | 1         | 1110          | Error carrier detection |

| MII_RX_DV | MII_RX_ER | MII_RXD [3:0] | Description           |
|-----------|-----------|---------------|-----------------------|
| 0         | 1         | 1111          | Reserved              |
| 1         | 0         | 0000-1111     | Normal data receiving |
| 1         | 1         | 0000-1111     | Data receiving error  |

### MII clock source

TX\_CLK and RX\_CLK clock signal can take effect only when 25MHz clock is provided to external PHY, and this signal can be output through MCO pin. The required frequency can be obtained on MCO pin through 25 MHz external quartz crystal only when PLL frequency doubling is configured.

### 27.3.2.3 Reduced media independent interface (RMII)

RMII reduces the number of pins of MCU of Ethernet peripherals and external PHY at 10/100Mbit/s. According to IEEE 802.3u standard, MII has 16 data and control signal pins. RMII reduces the number of pins to 7.

RMII is instantiated between MAC and PHY. It is conducive to converting MII of MAC to RMII. RMII has the following characteristics:

- (1) Separate 2-bit wide transmitting and receiving data path
- (2) 10-Mbit/s and 100-Mbit/s running speed
- (3) The reference clock is 50MHz
- (4) Provide the same reference clock to MAC and external Ethernet PHY from the outside

### RMII clock source

Use external 50MHz clock or embedded PLL to generate 50MHz-frequency signal to drive PHY.

### 27.3.2.4 MII/RMII selection

When the Ethernet controller is not in reset mode or the clock is enabled, the application program needs to set MII/RMII mode.

### 27.3.3 Media access control (MAC 802.3)

The access method of IEEE 802.3 international standard applicable to LAN is CSMA/CD. The Ethernet peripheral consists of one MAC 802.3 controller with MII and a dedicated DMA controller.

- (1) The following system uses LAN CSMA/CD sublayer
  - Support half-duplex and full-duplex
  - The conflict detection access method is applicable only to half-duplex

- The data rate of baseband system and broadband system is 10Mbit/s and 100Mbit/s
  - Support MAC to control frame sublayer
- (2) Functions of MAC sublayer
- Data encapsulation
    - Framing
    - Addressing
    - Error detection
  - Media access management
    - Media distribution
    - Contention resolution
- (3) Working mode of MAC sublayer
- Half-duplex: Contention for physical media with CSMA/CD algorithm
  - Full duplex: When the physical media supports synchronous transmission and receiving, and two full-duplex stations are connected to the LAN, data can be transmitted and received at the same time without solving the contention problem.

#### 27.3.3.1 MAC 802.3 frame format

IEEE 802.3-2002 standard specifies MAC uses MAC sublayer and optional MAC control sublayer (10/100 Mbit/s).

- (1) Two frame formats are specified for data communication system using CSMA/CD MAC
- Basic MAC frame format
  - Tagged MAC frame format
- (2) Frame structure of field
- Header: 7 bytes, used for synchronization
  - Start frame delimiter: 1 byte, indicating the start of the frame
  - Destination address and source address: MAC address field (6 bytes), indicating the address of destination station and source station
- (3) Address assignment is based on the following types
- Single address: The physical address related to THE special station in the network.
  - Group address: A multi-destination address related to one or more stations in a given network. There are two kinds of multicast addresses, that is, multicast group address and broadcast address.
  - QTag prefix: A 4-byte field inserted in the source address and MAC client length/type field. This field is an extension of the basic frame (untagged) to obtain the tagged MAC frame. There is no untagged MAC frame.

- Data and PAD: n bytes; the data are completely transparent, which means that any number of bytes may appear in data field. If PAD exists, its size is decided by the data size.
- MAC client length/type: 2 bytes, which have different meanings.
- Frame inspection sequence: 4 bytes including CRC value. CRC calculation is based on the following fields: source address, destination address, QTag prefix, length/type, LLC data and PAD.

#### 27.3.3.2 MAC frame transmission

All operations when DMA controls transmission. DMA pushes the data read from system memory into FIFO. Then the frame will pop up and be transmitted to MAC core. When frame transmission is over, the transmission state will be obtained from MAC core and sent back to DMA. The FIFO fill level is indicated to the DMA to initiate data acquisition in the required system memory burst by using the AHB interface. The data from AHB main interface will be pushed to FIFO. The depth of transmit FIFO is 2KB.

#### Transmit protocol

MAC controls transmission of Ethernet frame. The following functions are implemented to meet IEEE 802.3/802.3z specification:

- Generate header and SFD
- Generate transmitted frame state
- Generate blocking signals in half-duplex mode
- Control the flow (back pressure) in half-duplex mode
- Control Jabber timeout
- Including timestamp snapshot logic that conforms to IEEE 1588

#### Transmit CRC: Automatic generation of CRC and pad

In order to meet the minimum data field requirements of IEEE 802.3, when the number of bytes received from the application program is less than 60, zero will be attached to the transmitted frame to make the data length become 46 bytes. MAC can set not adding filling value. Calculate the CRC of the FCS field and attach it to the data being transmitted. If MAC is set to not attach the CRC value to the end of the Ethernet frame, the CRC will not be transmitted. However, when MAC is set to attach filling to the frame less than 60 bytes, CRC will be attached to the end of the filling frame.

#### Transmit data packets

Transmission of data packets contains transmission of single data packet and multiple data packets, and their operation mode is different.

#### Transmit scheduler

MAC is responsible for scheduling the frame transmission on MII. The interval between two transmitted frames can be maintained, and the truncated binary exponential rollback algorithm can be observed in half-duplex mode. MAC enables transmission after meeting IFG counter and rollback delay conditions.

### **Transmit flow control**

In full-duplex mode, when MAC\_FCTRL[TXFCTRLLEN]=1, MAC will generate pause frame and transmit it when needed. The pause frame and CRC are transmitted together. Generation of the pause frame can be enabled in two ways. When the application program sets FCTRLB bit to 1 or the receive FIFO is full, the pause frame will be transmitted.

### **Transmit FIFO refresh**

FTXF bit of ETH\_DMAOPMOD register controls to clear the transmit FIFO. Even if Tx FIFO is transmitting the frame to MAC core, Tx FIFO and the corresponding pointer will be immediately cleared to the initial state, as a result, an underrun event will be generated to MAC transmitter, and the frame transmission will be terminated. The state of the frame will mark both the underrun event and the frame emptying event.

### **Transmit status word**

After the Ethernet frame is transmitted to the MAC core and the core completes the transmission of the frame, the transmission state will be provided to the application program.

### **Transmit checksum offload**

The communication protocol uses the checksum field, which helps understanding the integrity of data transmitted through the network. Because encapsulating TCP and UDP on IP datagrams is the most wide application of the Ethernet, the Ethernet controller has the function of transmitting checksum offload, and this function supports checksum calculation and insertion in the transmitting path, and error detection in the receiving path.

### **Retransmitting during conflict**

In half-duplex mode, when transmitting frames to MAC, collision event may occur on the MAC line interface. The MAC may even indicate retrying before finishing receiving the frame. Then the frame will be retransmitted and pop up from the FIFO again.

### **MII/RMII**

Each half byte from MII is transmitted on RMII, double bits are transmitted at

one time, and the transmitting order is from low to high.

### 27.3.3.3 MAC frame receiving

The MAC pushes the received frame into the Rx FIFO. Once the state of this FIFO exceeds the configured receiving threshold, it will be indicated to DMA so that DMA can initiate preconfigured burst transmission to AHB interface.

#### Receive protocol

When a frame is received, the header and SFD of the frame will be removed. When SFD is detected, MAC will transmit Ethernet frame data to RX FIFO, which starts from the first byte after SFD. After the IEEE 1588 timestamp function is enabled, once an SFD is detected on the MII, a snapshot of the system time will be obtained. This timestamp will be transmitted to the application program, unless the MAC filters and discards the frame.

#### Receive multiple frames

Since the state is available immediately after receiving the data, the frames can be stored as long as the FIFO is not full.

#### Receive CRC: Automatic CRC and pad removal

The MAC will check the CRC error in the received frame and calculate the 32-bit CRC in it. No matter whether the pad/CRC is automatically removed, the Mac will receive the whole frame to calculate the CRC check of the received frame.

#### Received frame controller

When MAC\_FRAF[RXA]=0, MAC will perform frame filtering according to the destination address and source address. If filtering fails, the frame will be discarded and not be transmitted to the application program. When the filtering parameters change dynamically, the filtering fails, the remaining frames will be discarded and the receive status word will be updated immediately. In Ethernet power-down mode, all received frames will be discarded and not be forwarded to the application program.

#### Receive checksum offload

The IPC bit in the MAC\_CFG register controls the receive checksum offload. This function is to detect and process IPv4 and IPv6 frames in received Ethernet frame to ensure data integrity. The MAC identifies IPv4 or IPv6 frames by checking the type field of the received Ethernet frame. This identification method is also applicable to frames with VLAN tag.

#### Receive flow control

MAC\_FCTRL[RXFCTRLLEN] controls the detection function of pause frame. When this bit is set, the MAC will detect the receiving pause frame and the frame transmission will pause. The specific time is determined by the delay set in the received pause frame. After the flow control is enabled, start to monitor whether the destination address of the received frame matches the multicast address of the control frame. If they match, the MAC will determine whether to transmit the received control frame to the application program according to the MAC\_FRAFPCTRLF bit.

## Error processing

Table 136 Error Handling Situation

| Occurrence                                                                                                           | Processing results                                                                                                                                                                                                                                  |
|----------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rx FIFO has been full before EOF data is received from MAC.                                                          | Discard the entire frame, and the overrun counter in the ETH_DMAMFABOCNT register increases.                                                                                                                                                        |
| Use FERRF and FUF bits in the ETH_DMAOPMOD register to enable the corresponding functions.                           | Rx FIFO can filter error frames and too small frames.                                                                                                                                                                                               |
| Configure the receive FIFO to work in storage and forwarding mode.                                                   | Filter and discard all error frames.                                                                                                                                                                                                                |
| In pass-through mode, if the SOF of the frame is read from Rx FIFO, the state and length of the frame are available. | The whole error frame can be discarded. DMA can empty the error frame being read from FIFO. Then stop the data transmission to DMA, read from the inside and discard the remaining frames. If available, transmission of next frame can be started. |

## Receive status word

At the end of Ethernet frame receiving, MAC will output the receiving state to DMA. The detailed description of receiving state is the same as RXDES0[31:0].

## Frame length interface

The data transmission and receiving between the application and the MAC are conducted in the form of transmitting a complete frame. The application layer needs to know the length of the frame received from the inbound port in order to transmit the frame to the outbound port. The MAC core provides the length of each received frame at the end of receiving of each frame.

## MII/RMII receive bit sequence

Each half byte is transmitted from the two bits received on RMII to MII, and the transmitting order is from low to high.

### 27.3.3.4 MAC interrupt

Various events can generate an interrupt to the MAC core, and the MAC\_ISTS



register describes various event interrupts. Setting the corresponding mask bit in the interrupt mask register can prevent event interrupts from being generated. The interrupt can be cleared by reading the corresponding state register and other registers.

### 27.3.3.5 MAC filtering

#### Address filtering

Check the destination address and source address of all received frames and report the corresponding address filtering state. The address check depends on the setting of the frame filter register. The filtered frames can be identified: multicast frames or broadcast frames. Address filtering uses the MAC address of the station and the multi-broadcast list for address check.

#### Unicast destination address filtering

MAC supports 4 MAC addresses for unicast perfect filtering. If `MAC_FRAF[HUC]=0`, MAC will compare whether all 48 bits of the received unicast address match the set MAC address.

#### Multicast destination address filtering

The PM of `MAC_FRAF` register controls whether to set the MAC to pass all multicast frames. When the PM bit is reset, the HMC bit of the `MAC_FRAF` register controls the multicast address filtering.

#### Hash or perfect address filtering

When setting HPF bit, HUC bit and HMC bit of `MAC_FRAF` register, DA filter is configured to allow frames to pass when its DA matches hash filter or perfect filter. This configuration is applicable to unicast and multicast frames. If the HPF bit is reset, there is only one filtering method.

#### Broadcast address filtering

In the default mode, the MAC does not filter broadcast frames. However, if `MAC_FRAF[DISBF]=1`, all broadcast frames will be discarded.

#### Unicast source address filtering

The MAC performs perfect filtering according to the source address of the received frame. By default, the MAC compares the SA field with the value in the SA register. When Bit 30 in the corresponding register is set, the MAC address register will be configured to contain SA for comparison. If `MAC_FRAF[SAFEN]=0`, the result of SA filtering will be presented in the status bit of the received status word. Otherwise, the MAC will discard the frames that do not pass SA filtering.

## Reverse filtering

In the final output, the DAIF and SAIF bits of MAC\_FRAF control the filtering of destination address and source address respectively. The DAIF bit is applicable to unicast and multicast DA frames. When this bit is set, the result of unicast/multicast destination address filtering will be reversed. When the SAIF bit is set, the result of unicast SA filtering will be reversed.

Table 137 Destination Address Filtering

| Frame type | PR | HUC | HMC | DAIF | PM | DISBF | HPF | DA filtering operation                                                                            |
|------------|----|-----|-----|------|----|-------|-----|---------------------------------------------------------------------------------------------------|
| Broadcast  | 1  | X   | X   | X    | X  | X     | X   | Pass                                                                                              |
|            | 0  | X   | X   | X    | X  | 0     | X   | Pass                                                                                              |
|            | 0  | X   | X   | X    | X  | 1     | X   | Fail                                                                                              |
| Unicast    | 1  | X   | X   | X    | X  | X     | X   | All frames pass                                                                                   |
|            | 0  | 0   | X   | 0    | X  | X     | X   | Pass when perfect/group filter matches                                                            |
|            | 0  | 0   | X   | 1    | X  | X     | X   | Fail when perfect/group filter matches                                                            |
|            | 0  | 1   | X   | 0    | X  | X     | 0   | Pass when hash filter matches                                                                     |
|            | 0  | 1   | X   | 1    | X  | X     | 0   | Fail when hash filter matches                                                                     |
|            | 0  | 1   | X   | 0    | X  | X     | 1   | Pass when hash or perfect/group filter matches                                                    |
|            | 0  | 1   | X   | 1    | X  | X     | 1   | Fail when hash or perfect/group filter matches                                                    |
| Multicast  | 1  | X   | X   | X    | X  | X     | X   | All frames pass                                                                                   |
|            | X  | X   | X   | X    | 1  | X     | X   | All frames pass                                                                                   |
|            | 0  | X   | 0   | 0    | 0  | X     | X   | If PCTRLF=0x, pass when perfect/group filter matches, and discard the pause control frame         |
|            | 0  | X   | 1   | 0    | 0  | X     | 0   | If PCTRLF=0x, pass when hash filter matches, and discard the pause control frame                  |
|            | 0  | X   | 1   | 0    | 0  | X     | 1   | If PCTRLF=0x, pass when hash or perfect/group filter matches, and discard the pause control frame |
|            | 0  | X   | 0   | 1    | 0  | X     | X   | If PCTRLF=0x, fail when perfect/group filter matches, and discard the pause control frame         |
|            | 0  | X   | 1   | 1    | 0  | X     | 0   | If PCTRLF=0x, fail when hash filter matches, and discard the pause control frame                  |

| Frame type | PR | HUC | HMC | DAIF | PM | DISBF | HPF | DA filtering operation                                                                            |
|------------|----|-----|-----|------|----|-------|-----|---------------------------------------------------------------------------------------------------|
|            | 0  | X   | 1   | 1    | 0  | X     | 1   | If PCTRLF=0x, fail when hash or perfect/group filter matches, and discard the pause control frame |

Table 138 Source Address Filtering

| Frame type | PR | SAIF | SAFEN | SA filtering operation                                                               |
|------------|----|------|-------|--------------------------------------------------------------------------------------|
| Unicast    | 1  | X    | X     | All frames pass                                                                      |
|            | 0  | 0    | 0     | Pass when perfect/group filter matches, but the pause control frame is not discarded |
|            | 0  | 1    | 0     | Fail when perfect/group filter matches, but the frame is not discarded               |
|            | 0  | 0    | 1     | Pass when perfect/group filter matches, and discard the failed frames                |
|            | 0  | 1    | 1     | Fail when perfect/group filter matches, but the failed frames are not discarded      |

### 27.3.3.6 MAC loopback mode

MAC can loop back the received frames. This function is controlled by LBM bit of MAC\_CFG register, and it is disabled by default.

### 27.3.3.7 MAC management counter (MMC)

MMC has a control register, two interrupt state registers, and two mask interrupt registers to collect information about received frames and transmitted frames. These registers are accessible from the application program.

Receive the MMC counter and update the frames that have passed address filtering. The discarded frame will not be updated unless the discarded frame is a short frame less than 6 bytes.

#### Good frame

- (1) If there are no following errors during transmission, the transmitted frame is a “good frame”:
  - Frame underrun
  - No carrier/lost carrier
  - Jabber timeout
  - Delay conflict
  - Excessive delay
  - Excessive conflict
- (2) If there are no following errors during receiving, the received frame is a “good frame”:
  - Short frame

- CRC error
  - MII\_RXER input error
  - Alignment error (for 10/100Mb/s only)
  - Length error (for non-type frames only)
  - Out of range (for non-type frames only, exceeding the maximum size)
- (3) The frame type determines the maximum frame size as follows:
- Maximum size of untagged frame=1518
  - Maximum size of VLAN frame=1522

### 27.3.3.8 Power management (PMT)

PMT supports receiving network remote wake-up frame and magic data packet frame. Interrupts can be generated for wake-up frames and magic data packet frames received by MAC. PMT module can be enabled by WKUPFEN bit and MPEN bit of MAC\_PMTCTRLSTS register. When the power-down mode is enabled in the PMT, the MAC will discard all received frames and will not forward them to the application. The power-down mode will exit only when the remote wake-up frame or magic data packet frame is received and the corresponding detection is enabled.

#### Detect remote wake-up frame

When MAC is in sleep mode and MAC\_PMTCTRLSTS[WKUPFEN]=1 is enabled, the MAC can resume normal work after receiving the remote wake-up frame.

#### Detect magic data packet

AMD company's technology can be used to power on the devices which are in sleep mode on the network. MAC receives a specific information packet called magic data packet, and its address is the node on the network. Only the magic data packets that are transmitted to the device or multicast address are checked to determine whether they meet the wake-up requirements.

#### System precautions during power-down

When the EINT 19 interrupt line is enabled, the Ethernet PMT module can detect frames when the system is in stop mode. The MAC receiver state machine shall remain enabled in power-down mode.

### 27.3.3.9 Precision time protocol (IEEE 1588PTP)

The IEEE 1588 standard defines a protocol. It is suitable for systems that communicate through LAN supporting multicast message transmission and synchronous heterogeneous systems, including clocks with different fixing accuracy, resolution and stability. It supports precision clock synchronization in measurement and control systems which are handles by technologies such as

network communication, LAN computing and distributed objects. It supports system-level synchronization accuracy within the subsecond range, and requires minimal network and local clock computing resources. This protocol, called precision time protocol, is transmitted through UDP/IP. The system or network is divided into master node and slave node, which are used to allocate timing/clock information. The protocol synchronizes the slave node to the master node by exchanging PTP messages.

### **Use PTP to transmit frames**

The timestamp is captured when the SFD of the frame is output on the MII. Each transmitted frame may be tagged to indicate whether there is need to capture the timestamp of this frame. PTP frames can be identified without processing the transmitted frame. Transmit the control bit control frame in the descriptor. The captured timestamp is returned to the application in a manner of providing the frame state. The timestamp will be transmitted back to the corresponding transmit descriptor along with the transmission state of the frame, so that the timestamp can be connected with the specific PTP frame. The 64-bit timestamp information is written back to the TXDES2 and TXDES3 fields, wherein TXDES2 maintains the 32 least significant bits of the timestamp.

### **Use PTP to receive frames**

When the IEEE 1588 timestamp function is enabled, the timestamps of all frames received on the MII will be captured by the Ethernet MAC. The MAC provides the timestamp when the frame receiving is completed. The captured timestamp is returned to the application in a manner of providing the frame state. The timestamp will be transmitted back to the corresponding receive descriptor along with the receiving state of the frame. The 64-bit timestamp information is written back to the RXDES2 and RXDES3 fields, wherein RXDES2 maintains the 32 least significant bits of the timestamp.

### **Reference timing source**

To take a time snapshot, the core needs a 64-bit reference time. PTP reference clock input is used to generate reference time and capture timestamp internally. The frequency of the generated reference clock cannot be less than the resolution of the timestamp counter. The synchronization precision target between the master node and each slave node is about 100ns.

### **Calibration method**

Synchronizing or updating the system time in a process is the coarse calibration method, and synchronizing or updating the system time in order to reduce the system time jitter is the precision calibration method.

## System time calibration method

The 64-bit PTP time is refreshed by the PTP input reference clock HCLK. In order to obtain the timestamp of the Ethernet frame transmitted or received on the MII, this time is used as the clock source. The system time timer can be initialized or calibrated in coarse calibration or precision calibration method.

## System time initialization

The timestamp function is controlled by TSEN bit of PTP\_TSCTRL register. After setting, the timestamp can be enabled only by initializing the timestamp counter.

## PTP trigger connected internally to TMR2

In order to avoid the uncertainty of command execution time caused by use of interrupt when the system time is greater than the target time, the PTP trigger output signal internally connected to TMR2 input trigger can be set to high level when the system time is greater than the target time.

## PTP pulse per second output signal

PTP pulse is used to check the synchronization of all nodes in the network. Two clocks can be provided with pulses per second (PPS) output signals to test the difference between the local slave clock and the master reference clock. The pulse width of PPS output is 125ms.

### 27.3.4 DMA controller

DMA is used for packet data transmission. The controller can be set to generate CPU interrupt under normal/error conditions such as completion of transmitting frames and receiving frames. DMA has separate transmitter and receiver and corresponding control and state registers. The transmitter transmits the data in the system memory to Tx FIFO, and the receiver transmits the data received by Rx FIFO to the system memory. DMA descriptor can transmit data from the source address to the destination address with minimal CPU intervention. The communication mode between DMA and CPU falls into the following two data structures:

- Control and state register
- Descriptor list and data buffer

#### 27.3.4.1 Host bus burst access

DMA attempts fixed-length burst transmission on the AHB main interface. The maximum length of the burst depends on the PBL bit of DMABMOD register. The receive and transmit descriptors access the 16 bytes to be read with the maximum possible burst size.

#### 27.3.4.2 Host data buffer alignment

The transmit and receive data buffers do not limit the start address alignment. In our system, the start address of the buffer can be aligned with any of the four bytes. DMA always starts transmission when the address is aligned with the bus width, and uses unnecessary byte channels to transmit empty data at the beginning or end of Ethernet frame transmission.

#### 27.3.4.3 Calculate buffer size

DMA only updates the status of transmit and receive descriptors, not the size. The size needs to be calculated by the driver. Transmit DMA will transmit the correct number of bytes to the MAC core.

#### 27.3.4.4 DMA arbiter

The arbiter in DMA arbitrates between the transmitting channel and the receiving channel accessing the AHB main interface respectively. Circular scheduling and fixed priority arbitration can be used.

#### 27.3.4.5 Error response to DMA

If the slave gives an error response to the data transmission initiated by the DMA channel, the corresponding DMA will stop all operations and update the FBERRFLG bit and ERRB bit in ETH\_DMASTS register.

#### 27.3.4.6 Tx DMA

Tx DMA contains two modes: default mode and OSF mode.

#### Process transmitted frames

The expected data buffer of transmit DMA contains a complete Ethernet frame, excluding header, pad and FCS. The DA, SA, and type/length fields contain valid data. When the transmit descriptor indicates that the MAC core disables the insertion of CRC or pad, the buffer must have a complete Ethernet frame containing CRC bytes. The frame is bounded by the first descriptor and the last descriptor, which can be a data link or across multiple buffers.

#### Pause transmission polling

When DMA detects all descriptors and the TXBU bit of ETH\_DMASTS register is set, the transmission polling will be suspended. Or when a transmission error caused by underrun is detected, the frame transmission will be aborted. The corresponding transmit descriptor 0 bit will be set to 1. If the second condition occurs, AINTS bit and TXUNF bit of ETH\_DMASTS register will be set, and if the information is written to the transmission descriptor 0, the transmission polling will also be suspended.

### 27.3.4.7 Functional description of general transmit descriptor

The general transmit descriptor structure consists of four 32-bit words. If the timestamp is activated or IPv4 checksum offload is activated, the enhanced descriptor must be used.

#### Transmit descriptor word 0 (TXDES0)

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                          |
|-------|-------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | DEF   | R/W | Deferred<br>When this bit is set, it indicates that the MAC is delayed before transmission due to the existence of carrier. This bit is valid only in half-duplex mode.<br>0: No delay<br>1: Delay                                                                                                   |
| 1     | UFERR | R/W | Underflow Error<br>When this bit is set, it indicates the MAC terminates the frame because the data arrives late from the host memory. The underflow error indicates that the DMA encountered an empty transmit buffer while transmitting frames. The transmitting process enters the pending state. |
| 2     | EDEF  | R/W | Excessive Deferral<br>If MAC_CFG[4] is set to 1, this bit indicates that transmission has been over.                                                                                                                                                                                                 |
| 6:3   | CCNT  | R/W | Collision Count<br>The value of this bit field indicates the number of collisions that occurs before frame transmission. Invalid when TXDES0[8] is set to 1.                                                                                                                                         |
| 7     | VLANF | R/W | VLAN Frame<br>When this bit is set, it indicates that the transmitted frame is a frame of VLAN type.                                                                                                                                                                                                 |
| 8     | EC    | R/W | Excessive Collision<br>When this bit is set, it indicates that the transmission is terminated after 16 consecutive collisions when trying to transmit the current frame. If MAC_CFG[9] is set, this bit will be set after the first collision, and the transmission of the frame will be terminated. |
| 9     | LC    | R/W | Late Collision<br>When this bit is set, it indicates that the frame transmission is terminated due to a collision after the collision window. This bit is invalid if underflow error is set.                                                                                                         |
| 10    | NC    | R/W | No Carrier<br>When this bit is set, it indicates that the carrier detection signal of PHY is continuously formed during transmission.                                                                                                                                                                |
| 11    | LSC   | R/W | Loss of Carrier<br>When this bit is set, it indicates that the carrier is lost during frame transmission. Only when the MAC works in half-duplex mode, it is valid for frames transmitted without conflict.                                                                                          |



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12    | IPERR    | R/W | <p>IP Payload Error</p> <p>When this bit is set to 1, it indicates that the MAC transmitter detects an error in the TCP, UDP, or ICMP IP packet payload. The transmitter will check the payload length received in the IPv4 or IPv6 header according to the actual number of bytes of TCP, UDP or ICMP IP packets received from the application program. If there is mismatch, the error status will be displayed.</p>                                                                                                                                                                                                                                                                           |
| 13    | FF       | R/W | <p>Frame Flushed</p> <p>When this bit is set, it indicates that DMA or MTL refreshes the frame due to the software refresh command given by the CPU.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14    | JTO      | R/W | <p>Jabber Timeout</p> <p>When this bit is set, it indicates that the MAC transmitter has experienced a jabber timeout. This bit can be set only when JDIS bit of MAC_CFG register is not set.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15    | ERRS     | R/W | <p>Error Summary</p> <p>The value is OR operation result of the following bits:</p> <p>TXDES0[1]: UFERR<br/> TXDES0[2]: EDEF<br/> TXDES0[8]: EC<br/> TXDES0[9]: LC<br/> TXDES0[10]: NC<br/> TXDES0[11]: LSC<br/> TXDES0[12]: IPERR<br/> TXDES0[13]: FF<br/> TXDES0[14]: JTO<br/> TXDES0[16]: IHERR</p>                                                                                                                                                                                                                                                                                                                                                                                           |
| 16    | IHERR    | R/W | <p>IP Header Error</p> <p>When this bit is set to 1, it indicates that the MAC transmitter has detected an error in the IP data header. The transmitter will check the header length of IPv4 packets according to the number of header bytes received from the application program. If there is a mismatch, it indicates the error status. If the main header length of IPv6 frame is not 40 bytes, a header error will be reported. If the value of the header length field of IPv4 frame is less than 0x5, a header error will also be reported. Besides, the Ethernet length/type field value of IPv4 or IPv6 frame must match the IP header version received along with the data packet.</p> |
| 17    | TXSS     | R/W | <p>TX Timestamp Status</p> <p>This status bit indicates that the timestamp of the corresponding transmitted frame has been captured. When this bit is set, TXDES2 and TXDES3 have the timestamp values captured for the transmitted frames. This bit field is valid only when the last control bit (TXDES0[29]) in the descriptor is set.</p> <p>When the enhanced descriptor is enabled, TXSS=1 indicates that there is timestamp value in TXDES6 and TXDES7.</p>                                                                                                                                                                                                                               |
| 19:18 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20    | TXCH     | R/W | Second Address Chained<br>When this bit is set to 1, the second address in the descriptor is the address of the next descriptor, not the address of the second buffer, and TXDES1[28:16] is "irrelevant" value. The priority of TXDES0[21] is higher than TXDES0[20].                                                                                                                                                                                                                                                                      |
| 21    | TXENDR   | R/W | Transmit End of Ring<br>When this bit is set to 1, the descriptor list has reached the last descriptor. DMA will return the base address of the descriptor list and form a descriptor ring.                                                                                                                                                                                                                                                                                                                                                |
| 23:22 | CHINS    | R/W | Checksum Insertion Control<br>These bits control the calculation and insertion of checksum. The bit codes are as follows:<br>00: Disable checksum insertion<br>01: Enable calculation and insertion of IP header checksum<br>10: Enable the calculation and insertion of payload checksum and IP header checksum, but the pseudo header checksum will not be calculated in hardware<br>11: Enable the calculation and insertion of payload checksum and IP header checksum, and the pseudo header checksum will be calculated in hardware. |
| 24    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 25    | TXTSSEN  | R/W | Transmit Timestamp Enable<br>When this bit is set to 1 and TSEN is set to 1, the IEEE1588 hardware timestamp function will be activated for the transmitted frame described in the descriptor. This bit is valid only when TXDES0[28]=1.                                                                                                                                                                                                                                                                                                   |
| 26    | DISP     | R/W | Disable Pad<br>0: DMA will automatically add complementary bit item and CRC for frames less than 64 bytes. Whether to add CRC field has nothing to do with TXDES0[27]<br>1: MAC will not automatically add complementary bit item for frames less than 64 bytes<br>This bit is valid only when TXDES0[28]=1.                                                                                                                                                                                                                               |
| 27    | DISC     | R/W | Disable CRC<br>When this bit is set to 1, MAC will not attach the CRC to the end of the transmitted frame. This bit is valid only when TXDES0[28]=1.                                                                                                                                                                                                                                                                                                                                                                                       |
| 28    | FS       | R/W | First Segment<br>When this bit is set to 1, it indicates that the buffer includes the first segment of the frame.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 29    | LS       | R/W | Last Segment<br>When this bit is set to 1, it indicates that the buffer includes the last segment of the frame.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 30    | INTC     | R/W | Interrupt on Completion<br>When this bit is set to 1, after transmission of current frame is completed, an interrupt will be transmitted.                                                                                                                                                                                                                                                                                                                                                                                                  |

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                 |
|-------|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | OWN  | R/W | <p>Own</p> <p>0: This descriptor belongs to CPU</p> <p>1: This descriptor belongs to DMA</p> <p>DMA will clear this bit when the frame transmission is completed or the buffer allocated in the descriptor is empty. All bits of the first descriptor of this frame should be set after all subsequent descriptors belonging to the same frame are set.</p> |

#### Transmit descriptor word 1 (TXDES1)

| Field | Name     | R/W | Description                                                                                                                                                                                                                 |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12:0  | TXBS1    | R/W | <p>Transmit Buffer 1 Size</p> <p>These bits indicate the size of the first data buffer. If the bit is 0, DMA will ignore this buffer and use the buffer 2 or the next descriptor, depending on the value of TXDES0[20].</p> |
| 15:13 | Reserved |     |                                                                                                                                                                                                                             |
| 28:16 | TXBS2    | R/W | <p>Transmit Buffer 2 Size</p> <p>These bits indicate the size of the second data buffer in bytes. If TXDES0[20]=1, this field will be invalid.</p>                                                                          |
| 31:29 | Reserved |     |                                                                                                                                                                                                                             |

#### Transmit descriptor word 2 (TXDES2)

| Field | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TXADDR1_TXFTSL | R/W | <p>Transmit Buffer 1 Address Pointer / Transmit frame timestamp low</p> <p>It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data.</p> <p>TXADDR1: When TXDES0[31]=1, these bits indicate the physical address of buffer 1. There are no restrictions on buffer address alignment.</p> <p>TXFTSL: Before TXDES0[31] is cleared to zero, the DMA will update this field with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.</p> |

#### Transmit descriptor word 3 (TXDES3)

| Field | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TXADDR2_TXFTSH | R/W | <p>Transmit Buffer 2 Address Pointer (Next descriptor address) / Transmit frame timestamp high</p> <p>It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data.</p> <p>TXADDR2: When TXDES0[31]=1 and the descriptor ring structure is used, these bits indicate the physical address of buffer 2. If TXDES1[24]=1, this address contains the pointer of the physical register where the next descriptor is located. The buffer address pointer matches the bus width only when TXDES1[24]=1.</p> <p>TXFTSH: Before TXDES0[31] is cleared to zero, the DMA will update this field with the 32 most significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.</p> |

#### 27.3.4.8 Functional description of enhanced transmit descriptor

If the timestamp or IPv4 checksum offload is activated, the enhanced descriptor must be used. The enhanced descriptor consists of eight 32-bit words, which is twice the normal size of the descriptor. Definitions of TXDES0, TXDES1, TXDES2 and TXDES3 are the same as those of general transmit descriptor. TXDES6 and TXDES7 contain the timestamp.

When selecting the enhanced descriptor mode, 32-byte memory need to be allocated for each descriptor. If the timestamp or IPv4 checksum offload is not used, the enhanced descriptor format can be disabled, and the software can use a general descriptor with a default size of 16 bytes.

##### Transmit descriptor word 4 (TXDES4)

| Field | Name | R/W | Description |
|-------|------|-----|-------------|
| 31:0  |      |     | Reserved    |

##### Transmit descriptor word 5 (TXDES5)

| Field | Name | R/W | Description |
|-------|------|-----|-------------|
| 31:0  |      |     | Reserved    |

##### Transmit descriptor word 6 (TXDES6)

| Field | Name   | R/W | Description                                                                                                                                                                                                                                   |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TXFTSL | R/W | <p>Transmit Frame Timestamp Low</p> <p>This bit field will be updated by the DMA with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when LS=1.</p> |

##### Transmit descriptor word 7 (TXDES7)

| Field | Name   | R/W | Description                                                                                                                                                                                                                        |
|-------|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TXFTSH | R/W | Transmit Frame Timestamp High<br>This bit field will be updated by the DMA with the 32 most significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when LS=1. |

#### 27.3.4.9 Rx DMA

##### Obtain receiving descriptor

The receiver always tries to get an additional descriptor to add to the frame to be received. It will attempt to obtain the descriptor when any of the following operations occurs:

- (1) The command of receiving polling requirements has been issued
- (2) After DMA runs, the STRX bit of ETH\_DMAOPMOD register is immediately set
- (3) The descriptor data buffer is full before the end of the currently transmitted frame
- (4) The receiving process is suspended because RDES0[OWN]=0, and a new frame is received
- (5) The receive data frame is completed, but the receive descriptor is not disabled

##### Process received frames

The MAC will transmit the received frames to the memory only when the frame whose size is not less than the threshold number of bytes set for the receive FIFO passes the address filtering, or when the whole frame is written to the FIFO in the storage and forwarding mode.

##### Stop when receiving

If a new received frame is detected when the receiving process is suspended, the DMA will obtain the current descriptor in memory again. If the descriptor is owned by DMA, the frame will be received again. If it is owned by the host, by default, the DMA will discard the current frame at the top of Rx FIFO and the lost frame counter will increase. If multiple frames are stored in Rx FIFO, the above process will be repeated. After DISFRXF bit of ETH\_DMAOPMOD register is set, it can avoid discarding or refreshing the frame at the top of the Rx FIFO. At this time, RXBU bit is set to 1 and the receiving process returns to the suspended state.

### 27.3.4.10 Functional description of general receive descriptor

The general receive descriptor structure consists of four 32-bit words. If the timestamp function or IPv4 checksum offload is activated, the enhanced descriptor must be used.

#### Receive descriptor word 0 (RXDES0)

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PERR_ESA   | R/W | <p>Payload Checksum Error / extended status available</p> <p>When this bit is set, the TCP, UDP or ICMP checksum calculated by the core does not match the checksum field of the received encapsulated TCP, UDP or ICMP segment. This bit will also be set when the number of payload bytes received does not match the value of the length field of the IPv4 or IPv6 datagram encapsulated in the received Ethernet frame.</p> <p>After the enhanced descriptor format is enabled, this bit has ESA functions. When ESA is set to 1, it indicates that there is an extended state in RXDES4. ESA is valid only when RXDES0[8]=1.</p> |
| 1     | CERR       | R/W | <p>CRC Error</p> <p>When this bit is set, a CRC error will occur on the received frame. This bit is valid only when RXDES0[8]=1</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2     | DERR       | R/W | <p>Dribble Error</p> <p>When this bit is set, the received frame has a multiple of non-integer bytes. This bit is valid only in MII mode.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3     | RERR       | R/W | <p>Receive Error</p> <p>When this bit is set and RX_DV signal is transmitted during frame receiving, RX_ERR signal will be generated.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 4     | RXWDTTO    | R/W | <p>Receive Watchdog Timeout</p> <p>When this bit is set, the receive watchdog timer has timed out when receiving the current frame, and the current frame will be truncated when the watchdog times out.</p>                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | FT         | R/W | <p>Frame Type</p> <p>0: The received frame is an Ethernet type frame<br/>1: The received frame is an IEEE802.3 frame</p> <p>When this bit is set or reset, it indicates that this bit is invalid for short frames less than 14 bytes.</p>                                                                                                                                                                                                                                                                                                                                                                                             |
| 6     | LC         | R/W | <p>Late Collision</p> <p>When this bit is set, a delay collision occurs when a frame is received in half-duplex mode.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 7     | IPCERR_TSV | R/W | <p>IPv header Checksum Error / Time Stamp Valid</p> <p>When this bit is set, there is an error in the IPv4 or IPv6 header. The reasons may be: the Ethernet type field is inconsistent with the IP header version field, and does not match the checksum of the header in IPv4, or the Ethernet frame lacks the required number of IP header bytes.</p> <p>After the enhanced descriptor format is enabled, this bit has TSV functions. When TSV=1, it indicates that the timestamp snapshot will be written in RXDES6 and RXDES7. TSV is valid only when RXDES0[8]=1.</p>                                                            |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                           |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8     | LDES   | R/W | Last Descriptor<br>When this bit is set, the buffer pointed to by the descriptor is the last buffer of the frame.                                                                                                                                                                                     |
| 9     | FDES   | R/W | First Descriptor<br>When this bit is set, the descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next descriptor contains the beginning of the frame.    |
| 10    | VLANF  | R/W | VLAN Frame<br>When this bit is set, the frame referred to by this descriptor is a VLAN frame with MAC tag.                                                                                                                                                                                            |
| 11    | OFERR  | R/W | Overflow Error<br>When this bit is set, the received frame is damaged due to buffer overflow in Rx FIFO.                                                                                                                                                                                              |
| 12    | LERR   | R/W | Length Error<br>When this bit is set, the actual length of the received frame does not match the length/type field. This bit is valid only when RXDES0[5]=0.                                                                                                                                          |
| 13    | SADDRF | R/W | Source Address Filter Fail<br>When this bit is set, the SA field of the frame does not pass the SA filter in the MAC.                                                                                                                                                                                 |
| 14    | DESERR | R/W | Descriptor Error<br>When this bit is set, it indicates that the frame is truncated because the frame is not suitable for the current descriptor buffer, and DMA has no next descriptor. The frame is truncated.<br>Note: This field is valid only when the last descriptor (RXDES0[8]) is set.        |
| 15    | ERRS   | R/W | Error Summary<br>The value is OR operation result of the following bits:<br>RXDES0[0]: PERR_ESA<br>RXDES0[1]: CERR<br>RXDES0[3]: RERR<br>RXDES0[4]: RXWDTTO<br>RXDES0[6]: LC<br>RXDES0[7]: IPCERR_TSV<br>RXDES0[11]: OFERR<br>RXDES0[14]: DESERR                                                      |
| 29:16 | FL     | R/W | Frame Length<br>This bit field indicates the byte length of the received frame transmitted to the host memory. This bit is valid only when RXDES0[8]=1 and RXDES0[14]=0.<br>When RXDES0[8]=0 and ERRS=0, it indicates the cumulative number of bytes that have been transmitted to the current frame. |
| 30    | ADDRF  | R/W | Destination Address Filter Fail<br>When this bit is set, it indicates the frame that fails DA filtering in MAC.                                                                                                                                                                                       |

| Field | Name | R/W | Description                                                                                                                                                                                   |
|-------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | OWN  | R/W | Own<br>0: This describer belongs to CPU<br>1: This describer belongs to DMA<br>This bit will be cleared when DMA completes frame receiving or the allocated buffer in the descriptor is full. |

Table 139 Configuration in Normal Descriptor Format

| Bit 0<br>(PERRC_ESA) | Bit 5<br>(FT) | Bit 7<br>(IPCERR_TSV) | Frame state                                                                                                                     |
|----------------------|---------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------|
| 0                    | 0             | 0                     | IEEE 802.3 type frame                                                                                                           |
| 1                    | 0             | 1                     | Type frame which is neither IPv4 nor IPv6                                                                                       |
| 0                    | 1             | 0                     | IPv4/IPv6 type frame; checksum error is not detected                                                                            |
| 1                    | 1             | 0                     | IPv4/IPv6 type frame; payload checksum error is detected                                                                        |
| 0                    | 1             | 1                     | IPv4/IPv6 type frame; IP header checksum error is detected                                                                      |
| 1                    | 1             | 1                     | IPv4/IPv6 type frame; IP header and payload checksum error are detected                                                         |
| 1                    | 0             | 0                     | IPv4/IPv6 type frame; there is no IP header checksum error, and the payload check bypasses because the payload is not supported |
| 0                    | 0             | 1                     | Reserved                                                                                                                        |

#### Receive descriptor word 1 (RXDES1)

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12:0  | RXBS1    | R/W | Receive Buffer 1 Size<br>0: DMA will ignore this buffer and use the buffer 2 or the next descriptor according to the value of RXCH bit.<br>Other: It indicates the size of the first data buffer. The buffer size must be a multiple of 4, 8, or 16, depending on the bus width, even if the value of the buffer 2 address pointer is not aligned. When the buffer size is not a multiple of 4, 8, or 16, the generated behavior is undefined. |
| 13    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 14    | RXCH     | R/W | Second Address Chained<br>When this bit is set, the second address in the descriptor is the address of the next descriptor, not the address of the second buffer. Ignore the value of RXBS2. RXER has priority over RXCH.                                                                                                                                                                                                                      |
| 15    | RXER     | R/W | Receive End of Ring<br>When this bit is set, it indicates that the descriptor list has reached the final descriptor. DMA will return the base address of the descriptor list and create a descriptor ring.                                                                                                                                                                                                                                     |



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28:16 | RXBS2    | R/W | <p>Receive Buffer 2 Size</p> <p>It indicates the size of the second data buffer. The buffer size must be a multiple of 4, 8, or 16, depending on the bus width, even if the value of the buffer 1 address pointer is not aligned. When the buffer size is not a multiple of 4, 8, or 16, the generated behavior is undefined.</p> <p>This bit field will be invalid if RXCH bit is set.</p> |
| 30:29 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                             |
| 31    | DINTC    | R/W | <p>Interrupt on Completion Disable</p> <p>When this bit is set, it will prevent the setting of RXFLG bit and make the received frame end in the buffer indicated by the descriptor, so as to disable causing the host interrupt.</p>                                                                                                                                                        |

### Receive descriptor word 2 (RXDES2)

| Field | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | RXADDR1_RXFTSL | R/W | <p>Receive Buffer 1 Address Pointer / Receive Frame Timestamp Low</p> <p>It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data.</p> <p>RXADDR1: When RXDES0[OWN]=1, these bits indicate physical address of the buffer 1. Except when the starting point of the frame is stored by using the value of RXDES2, the address is generated by DMA by using the configured value. During the start of transmitted frame, the DMA will perform write operation when RXDES2[3:0]=0, but the frame data will be shifted according to the actual buffer address pointer. When the address pointer points to the buffer where the middle or last part of the frame is stored, the DMA will ignore RXDES2[3:0]. There are no restrictions on buffer address alignment.</p> <p>RXFTSL: Before RXDES0[OWN] is cleared to zero, the DMA will update this field with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.</p> |

### Receive descriptor word 3 (RXDES3)

| Field | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | RXADDR2_RXFTSH | R/W | <p>Receive Buffer 2 Address Pointer (Next Descriptor Address) / Receive Frame Timestamp High</p> <p>It indicates the location of the data in the memory to the DMA. When all data have been transmitted, the DMA can use these bits to return the timestamp data.</p> <p>RXADDR1: When RXDES0[OWN]=1 and the descriptor ring structure is used, these bits indicate the physical address of buffer 2. If RXDES[24]=1, this address contains the pointer of the physical register where the next descriptor is located. The buffer address pointer matches the bus width only when RXDES1[24]=1. When RXDES[24]=0, except when the starting point of the frame is stored by using the value of RXDES2, the address is generated by DMA by using the configured value. When the address pointer points to the buffer where the middle or last part of the frame is stored, the DMA will ignore RXDES2[3:0], and there are no restrictions on buffer address alignment.</p> <p>RXFTSH: Before RXDES0[OWN] is cleared to zero, the DMA will update this field with the 32 least significant bits of the timestamp captured for the corresponding transmitted frame. The bit field contains a timestamp only when the timestamp function of this frame is activated and LS=1.</p> |

#### 27.3.4.11 Functional description of enhanced receive descriptor

If the timestamp or IPv4 checksum offload is activated, the enhanced descriptor must be used. The enhanced descriptor consists of eight 32-bit words, which is twice the normal size of the descriptor. Definitions of RXDES0, RXDES1, RXDES2 and RXDES3 are the same as those of general receive descriptor. RXDES4 includes extended state, and RXDES6 and RXDES7 include timestamp.

When selecting the enhanced descriptor mode, 32-byte memory need to be allocated for each descriptor. If the timestamp or IPv4 checksum offload is not used, the enhanced descriptor format can be disabled, and the software can use a general descriptor with a default size of 16 bytes.

#### Receive descriptor word 4 (RXDES4)

It is valid only when there is a state related to IPv4 checksum or timestamp.

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                             |
|-------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | IPPT | R/W | <p>IP Payload Type</p> <p>If IPv4 checksum offload is activated, it indicates the payload type encapsulated in IP datagram. These bits are "00" when there is an IP header error or there is a segmented IP.</p> <p>000: Unknown, or IP payload not processed</p> <p>001: UDP</p> <p>010: TCP</p> <p>011: ICMP</p> <p>1xx: Reserved</p> |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3     | IPHERR   | R/W | IP Header Error<br>When this bit is set, the 16-bit IPv4 header checksum calculated by the core does not match the received checksum, or the IP datagram version does not match the Ethernet type value.                                                                                                                                                                                                                                                                                                                                                               |
| 4     | IPPERR   | R/W | IP Payload Error<br>When this bit is set, the 16-bit IP payload checksum calculated by the core does not match the received checksum. When the TCP, UDP or ICMP segment length does not match the payload length value in the IP header field, it will also be set to 1.                                                                                                                                                                                                                                                                                               |
| 5     | PCBP     | R/W | IP Checksum Bypassed<br>When this bit is set, the checksum offload engine will be bypassed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6     | IPV4P    | R/W | Receive IPv4 Packet<br>When this bit is set, an IPv4 packet is received.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 7     | IPV6P    | R/W | receive IPv6 packet<br>When this bit is set, an IPv6 packet is received.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 11:8  | PTPMT    | R/W | PTP Message Type<br>0000: No PTP message received<br>0001: SYNC (all clock types)<br>0010: Follow_Up (all clock types)<br>0011: Delay_Req (all clock types)<br>0100: Delay_Resp (all clock types)<br>0101: Pdelay_Req (in point-to-point transparent clock) or Announce (in ordinary clock or boundary clock)<br>0110: Pdelay_Resp (in point-to-point transparent clock) or Management (in ordinary clock or boundary clock)<br>0111: Pdelay_Resp_Follow_Up (in point-to-point transparent clock) or Signaling (in ordinary clock or boundary clock)<br>1xxx: Reserved |
| 12    | PTPFT    | R/W | PTP Frame Type<br>0: Transmit through UDP-IPv4 or UDP-IPv6<br>1: Transmit through Ethernet<br>Valid only when the message type is non-zero. The type of packet received can be identified by bit 6 or bit 7.                                                                                                                                                                                                                                                                                                                                                           |
| 13    | PTPV     | R/W | PTP Version<br>Version format used by the received PTP message.<br>0: Version 1<br>1: Version 2<br>Valid only when the message type is non-zero.                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 31:14 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

#### Receive descriptor word 5 (RXDES5)

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 31:0  | Reserved |     |             |

#### Receive descriptor word 6 (RXDES6)

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | RXFTSL | R/W | Receive Frame Timestamp Low<br>This bit field will be updated by the DMA with the 32 least significant bits of the timestamp captured for the corresponding received frame. DMA updates the bit field only for the last descriptor of the received frame. When this bit field and RXFTSH are set at the same time, it is regarded that the timestamp has been damaged. |

#### Receive descriptor word 7 (RXDES7)

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | RXFTSH | R/W | Receive Frame Timestamp High<br>This bit field will be updated by the DMA with the 32 most significant bits of the timestamp captured for the corresponding received frame. DMA updates the bit field only for the last descriptor of the received frame. When this bit field and RXFTSL are set at the same time, it is regarded that the timestamp has been damaged. |

#### 27.3.4.12 DMA interrupt

There are two groups of interrupts: normal interrupt and abnormal interrupt. The interrupt can be cleared by writing to the corresponding bit of ETH\_DMASTS register. When all enabled interrupts in the group are cleared, the summary bit will also be cleared to zero. If the interrupt is caused by the MAC core, the PMTFLG or TSTFLG bits in the ETH\_DMASTS register will be set to high level.

#### 27.3.5 Ethernet interrupt

The Ethernet controller has two interrupt vectors: one for normal Ethernet operation and one for Ethernet wake-up events only when mapped to EINT 19. The first Ethernet vector is reserved for interrupts generated by MAC and DMA. The second is reserved for interrupts generated by PMT when a wake-up event occurs. The mapping of the wake-up event to EINT 19 makes the core exit the low-power mode and generate an interrupt.

When the Ethernet wake-up event mapped to EINT 19 occurs and both MAC PMT interrupt and EINT 19 interrupt with rising edge detection are enabled, two interrupts will be generated.

### 27.4 MAC register address mapping

Table 140 Register Address Mapping

| Register name | Description                  | Offset address |
|---------------|------------------------------|----------------|
| MAC_CFG       | Configuration register       | 0x00           |
| MAC_FRAF      | Frame filter register        | 0x04           |
| MAC_HTH       | Hash table high-bit register | 0x08           |

| Register name  | Description                          | Offset address |
|----------------|--------------------------------------|----------------|
| MAC_HTL        | Hash table low-bit register          | 0x0C           |
| MAC_ADDR       | MII address register                 | 0x10           |
| MAC_DATA       | MII data register                    | 0x14           |
| MAC_FCTRL      | Receive flow control register        | 0x18           |
| MAC_VLANT      | VLAN tag register                    | 0x1C           |
| MAC_REMVKUPFFL | Remote wake-up frame filter register | 0x28           |
| MAC_PMTCTRLSTS | PMT control and state register       | 0x2C           |
| MAC_DBG        | Debug register                       | 0x34           |
| MAC_ISTS       | Interrupt state register             | 0x38           |
| MAC_IMASK      | Interrupt mask register              | 0x3C           |
| MAC_ADDR0H     | MAC address 0 high register          | 0x40           |
| MAC_ADDR0L     | MAC address 0 low register           | 0x44           |
| MAC_ADDR1H     | MAC address 1 high register          | 0x48           |
| MAC_ADDR1L     | MAC address 1 low register           | 0x4C           |
| MAC_ADDR2H     | MAC address 2 high register          | 0x50           |
| MAC_ADDR2L     | MAC address 2 low register           | 0x54           |
| MAC_ADDR3H     | MAC address 3 high register          | 0x58           |
| MAC_ADDR3L     | MAC address 3 low register           | 0x5C           |

## 27.5 MAC register functional description

### 27.5.1 Configuration register (MAC\_CFG)

Offset address: 0x00

Reset value: 0x0000 8000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                             |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0   | Reserved |     |                                                                                                                                                                                                                                                         |
| 2     | RXEN     | R/W | <p>Receiver Enable</p> <p>The receiving state machine of MAC can receive frames from MII. After this bit is set, the receiving state machine of MAC will be turned off after the current frame is received, and will receive no frame from the MII.</p> |
| 3     | TXEN     | R/W | <p>Transmitter Enable</p> <p>The transmitting state machine of MAC can transmit on MII. After this bit is set, the transmitting state machine of MAC will be turned off after the current frame is transmitted, and will transmit no frame.</p>         |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4     | DC       | R/W | <p><b>Deferral Check</b></p> <p>The deferral check function enables MAC. When the delay of the transmitting state machine exceeds the mode of 24288 bits multiplied by 10 or 100 Mbps, the MAC will identify the frame aborted state, and set the excessive delay error in the transmitted frame state.</p> <p>When the bit is reset, the bit will disable the deferral check function until the CRS signal becomes an invalid signal, and the MAC will be delayed. This bit is applicable only in half-duplex mode.</p>                                                                                    |
| 6:5   | BL       | R/W | <p><b>Back off Limit</b></p> <p>This bit determines the random integer of the time delay (4096-bit time for 1000Mbps and 512-bit time for 10/100Mbps) that the MAC waits before retransmission attempt when retrying after collision. This bit is applicable only in half-duplex mode.</p> <p>00: <math>k = \min(n, 10)</math><br/> 01: <math>k = \min(n, 8)</math><br/> 10: <math>k = \min(n, 4)</math><br/> 11: <math>k = \min(n, 1)</math></p> <p>Wherein, <math>n</math> = the number of retransmission attempts. The value range of random integer <math>r</math> is <math>0 \leq r &lt; 2k</math></p> |
| 7     | ACS      | R/W | <p><b>Automatic Pad or CRC Stripping</b></p> <p>Only when the bit length of MAC is less than 1536 bytes, will Pad or FCS be removed when the frame comes in. All received frames with bit length greater than or equal to 1536 bytes are passed to the application program without removing Pad or FCS. When this bit is reset, the MAC will transmit all incoming frames to the host without modification.</p>                                                                                                                                                                                             |
| 8     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 9     | DISR     | R/W | <p><b>Disable Retry</b></p> <p>MAC will try to transmit once only. When a collision occurs to the MII interface, the MAC will ignore transmission of the current frame and report the abortion of a frame with a large collision error in the transmitted frame state. When this bit is reset, retry the MAC according to the setting of BL bit. This bit is applicable only in half-duplex mode.</p>                                                                                                                                                                                                       |
| 10    | IPC      | R/W | <p><b>IPv4 Checksum Offload</b></p> <p>The MAC calculates all 16-bit 1 complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 header checksum of the received Ethernet frame is correct, and gives the state in the receiving state word. This function is disabled when this bit is reset.</p>                                                                                                                                                                                                                                                                            |
| 11    | DM       | R/W | <p><b>Duplex Mode</b></p> <p>MAC works in full-duplex mode and can transmit and receive at the same time.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 12    | LBM      | R/W | <p><b>Loopback Mode</b></p> <p>When this bit is set, the MAC will run in loopback mode on the MII. The MII receive clock input (RX_CLK) needs to work in loopback mode normally, because there is no loopback in the transmit clock.</p>                                                                                                                                                                                                                                                                                                                                                                    |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13    | DISRXO   | R/W | Disable Receive Own<br>When it is confirmed that phy_txen_o is in half-duplex mode, MAC will disable receiving frames. When this bit is reset, MAC will receive all packets transmitted by PHY. This bit is not applicable if the MAC is working in full-duplex mode.                                                                                                                       |
| 14    | SSEL     | R/W | Speed Select<br>0: 10Mbps<br>1: 100Mbps                                                                                                                                                                                                                                                                                                                                                     |
| 15    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                             |
| 16    | DISCRS   | R/W | Disable Carrier Sense During Transmission<br>When it is set to high, the MAC transmitter will ignore the MII CRS signal during frame transmission in half-duplex mode. This request results in no error due to carrier loss or no carrier in such transmission process. When it is set to low, the MAC transmitter will generate a carrier sense error and can even abort the transmission. |
| 19:17 | IFG      | R/W | Inter-Frame Gap<br>These bits are used to control the minimum gap between frames during transmission.<br>000: 96-bit time<br>001: 88-bit time<br>010: 80-bit time<br>...<br>111: 40-bit time<br>In half-duplex mode, the minimum IFG can only be configured as 64 bits (IFG=100), and lower value will not be considered.                                                                   |
| 21:20 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                             |
| 22    | JDIS     | R/W | Jabber Disable<br>The MAC disables the Jabber timer on transmitting end. MAC can transmit up to 16384 bytes frames. When this bit is reset, if the application program transmits more than 2048 bytes of data during transmission, the MAC will cut off the transmitter.                                                                                                                    |
| 23    | WDTDIS   | R/W | Watchdog Disable<br>The MAC disables the watchdog timer on the receiving end. The MAC can receive up to 16384 bytes of frames. When this bit is reset, the MAC does not allow the received frame to exceed 2048 bytes or the watchdog timeout register. After the watchdog limits the number of bytes, the MAC will disable receiving any bytes.                                            |
| 24    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                             |
| 25    | CST      | R/W | CRC Stripping for Type Frames<br>The last 4 bytes of all Ethernet type frames are removed and deleted before they are forwarded to the application program.                                                                                                                                                                                                                                 |
| 31:26 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                             |

## 27.5.2 Frame filter register (MAC\_FRAF)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PR     | R/W | Promiscuous Mode<br>The address filtering module will pass all incoming frames, regardless of destination address or source address. The SA or DA state bits of the receiving state word are always cleared.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1     | HUC    | R/W | Hash Unicast<br>The MAC filters the destination address of unicast frames according to the hash table. After reset, the MAC performs perfect destination address filtering on unicast frames, which compares the DA field with the value programmed in the DA register.                                                                                                                                                                                                                                                                                                                                                                             |
| 2     | HMC    | R/W | Hash Multicast<br>The MAC filters the destination address of received multicast frames according to the hash table. After reset, the MAC performs perfect destination address filtering on multicast frames, which compares the DA field with the value programmed in the DA register.                                                                                                                                                                                                                                                                                                                                                              |
| 3     | DAIF   | R/W | DA Inverse Filtering<br>The address check block compares the DA addresses of unicast and multicast frames in inverse filtering method. After reset, normal frame filtering will be performed.                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 4     | PM     | R/W | Pass All Multicast<br>All received frames whose destination address is multicast address (the first field of the destination address fields is 1) will be delivered. The filtering of multicast frames after reset depends on HMC bit.                                                                                                                                                                                                                                                                                                                                                                                                              |
| 5     | DISBF  | R/W | Disable Broadcast Frames<br>The address filter will filter all incoming broadcast frames. After reset, the address filter will transmit all received broadcast frames.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:6   | PCTRLF | R/W | Pass Control Frames<br>These bits control the forwarding of all control frames (including unicast and multicast pause frames).<br>00: MAC filters all control frames arriving at the application program.<br>01: Even if all control frames except pause frame do not pass the address filter, the MAC will also forward them to the application program.<br>10: Even if the control frames do not pass the address filter, the MAC will also forward them to the application program.<br>11: MAC forwards the control frames that pass the address filtering.<br>Note: MAC is enabled to full-duplex mode when RXFCTRLLEN bit of MAC_FCTRL is set. |
| 8     | SAIF   | R/W | SA Inverse Filtering<br>The address check block compares the addresses of SA in inverse filtering method. SA frames that match the SA register will be marked as SA address filter failure. After reset, the SA frames that do not match the SA register will be marked as SA address filter failure.                                                                                                                                                                                                                                                                                                                                               |
| 9     | SAFEN  | R/W | Source Address Filter Enable<br>The MAC compares the SA field of the received frame with the value programmed in the enabled SA register. If the comparison fails, the MAC will discard the frame. After reset, the MAC will forward the received frames to the application program of receiving state for updating SAFEN bit.                                                                                                                                                                                                                                                                                                                      |
| 10    | HPF    | R/W | Hash or Perfect Filter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |



| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | If it matches the perfect filter or Hash filter set for the HMC or HUC bit, it will configure the address filter to pass the frame. When this bit is low and the HUC or HMC bit is set, the frame will be passed only when the Hash filter matches.                                                                                                                           |
| 30:11 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                               |
| 31    | RXA      | R/W | Receive All<br>The MAC receiving module will transmit all received frames, regardless of whether they pass the address filter. The result of SA or Da filtering is updated in the corresponding bit of the receiving state word. When this bit is reset, the receiving module will only pass these frames to the application program that passes the SA or DA address filter. |

### 27.5.3 Hash table high-bit register (MAC\_HTH)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                    |
|-------|------|-----|------------------------------------------------|
| 31:0  | HTH  | R/W | Hash Table High<br>High 32 bits of Hash table. |

### 27.5.4 Hash table low-bit register (MAC\_HTL)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                  |
|-------|------|-----|----------------------------------------------|
| 31:0  | HTL  | R/W | Hash Table Low<br>Low 32 bits of Hash table. |

### 27.5.5 MII address register (MAC\_ADDR)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | MB   | R/W | MII Busy<br>Write to MAC_HT register and this bit will be valid. During PHY register access period, the software sets this bit to 1, indicating that read or write access is in progress. Therefore, MII data should remain valid in a PHY write operation until the MAC clears this bit. For read operation, MAC_HT is valid after this bit is cleared. Subsequent read and write operation can be performed only after the previous operation is completed. |
| 1     | MW   | R/W | MII Write<br>For PHY, this bit indicates that this is a write operation using the MII data register. If this bit is not set, it indicates that this is a read operation and the data will be put in the MII data register.                                                                                                                                                                                                                                    |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:2   | CR       | R/W | <p>Clock Range</p> <p>The selection of CR clock range determines the frequency of HCLK and is used to determine the frequency of MDC clock:</p> <p>Select HCLK MDC clock</p> <p>000: 60-100 MHz-HCLK/42</p> <p>001: 100-150 MHz-HCLK / 62</p> <p>010: 20-35 MHz-HCLK/16</p> <p>011: 35-60 MHz-HCLK/26</p> <p>100: 150-168 MHz-HCLK/102</p> <p>101, 110, 111: Reserved</p> |
| 5     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                           |
| 10:6  | MR       | R/W | <p>MII Register</p> <p>These bits select the required register in the selected PHY devices.</p>                                                                                                                                                                                                                                                                           |
| 15:11 | PA       | R/W | <p>Physical Layer Address</p> <p>It indicates which of the 32 possible PHY devices are being accessed.</p>                                                                                                                                                                                                                                                                |
| 31:16 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                           |

### 27.5.6 MII data register (MAC\_DATA)

Offset address: 0x14

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | MD       | R/W | <p>MII Data</p> <p>The 16-bit data value read from PHY after performing the management of read operation, or the 16-bit data value written to PHY before performing the management of write operation.</p> |
| 31:16 | Reserved |     |                                                                                                                                                                                                            |

### 27.5.7 Receive flow control register (MAC\_FCTRL)

Offset address: 0x18

Reset value: 0x0000 0000

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | FCTRLB/BPA | R/W | <p>Flow Control Busy/Back Pressure Activate</p> <p>When a pause control frame is initiated in full-duplex mode, this bit should be read as 0 before it is written to the flow control register. Only when the application program sets this bit to 1, can a pause control frame be initialized. During the transmission of the control frame, this bit continues to be set to indicate that the frame transmission is in progress. After the transmission of the pause control frame is completed, the MAC will reset this bit to 0. It cannot be written to the flow control register before this bit is cleared.</p> <p>In half-duplex mode, if the TXFCTRLLEN bit is set, the back pressure function will be activated. When this bit is set (and TXFCTRLLEN is set), the back pressure will be declared by the MAC core. During back pressure period, when the MAC receives a new frame, the transmitter starts to transmit JAM mode, which causes collision. When MAC is configured as full-duplex mode, BPA will be automatically disabled.</p> |

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | TXFCTRLLEN | R/W | <p>Transmit Flow Control Enable</p> <p>In full-duplex mode, when this bit is set, MAC will enable the flow control operation to transmit the pause frame. When this bit is reset, the flow control operation of MAC will be disabled, and MAC will not transmit any pause frame.</p> <p>In half-duplex mode, when this bit is set, the MAC will enable back pressure operation.</p> <p>When this bit is reset, the back pressure characteristic will be disabled.</p>                                                                                                                                                                                                                                                              |
| 2     | RXFCTRLLEN | R/W | <p>Receive Flow Control Enable</p> <p>When this bit is set, the MAC will decode the received pause frame and disable its transmitter within the specified pause time.</p> <p>When this bit is reset, the decoding function of the pause frame will be disabled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 3     | UNPFDETE   | R/W | <p>Unicast Pause Frame Detect</p> <p>When this bit is set, the MAC uses the unique multicast address to detect the pause frames, and also uses the specified unicast address in the MAC_ADDR0H and MAC_ADDR0L registers to detect the pause frame.</p> <p>When this bit is reset, the MAC only detects the pause frame of the unique multicast address specified in the 802.3x standard.</p>                                                                                                                                                                                                                                                                                                                                       |
| 5:4   | PTSEL      | R/W | <p>Pause Threshold Select</p> <p>Set the threshold of Pause timer for automatic retransmission of pause frames. The threshold should always be less than the pause time configured by bit [31:16]. For example, if PT = 100H (256 slot time) and PTSEL = 01, and the second PAUSE frame is initiated at 228 (256-28) slot time after the first PAUSE frame is transmitted, the second Pause frame will be automatically transmitted.</p> <p>Select the threshold</p> <p>00: Pause time - 4-slot time</p> <p>01: Pause time - 28-slot time</p> <p>10: Pause time - 144-slot time</p> <p>11: Pause time - 256-slot time</p> <p>The slot time is defined as the time that the MII interface takes to transmit 512 bits (64 bytes)</p> |
| 6     | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 7     | ZQPDIS     | R/W | <p>Zero-quanta Pause Disable</p> <p>When this bit is set, it is disabled to automatically generate zero-range pause control frame when the flow control signal of FIFO layer fails.</p> <p>When this bit is reset, normal operation of automatic zero-range pause control frame generation is enabled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:8  | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 31:16 | PT         | R/W | <p>Pause Time</p> <p>This bit saves the value used in the transmission of control frame. If this bit is configured to be double synchronized to the MII clock domain, continuous write operations should be performed on the register only after at least 4 clock cycles in the target clock domain.</p>                                                                                                                                                                                                                                                                                                                                                                                                                           |

### 27.5.8 VLAN tag register (MAC\_VLANT)

Offset address: 0x1C

Reset value: 0x0000 0000

This register contains the IEEE 802.1Q VLAN tag, used to identify the VLAN frame. The MAC compares No. 13 and No. 14 bytes of the received frame (length/type) with 0x8100, and compares the next 2 bytes with VLAN tag; if the match is successful, set the receive VLAN bit of the received frame state. The legal length of the frame increases from 1518 bytes to 1522 bytes.

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | VLANTID   | R/W | VLAN Tag Identifier<br>It contains 802.1Q VLAN tag, which is used to identify VLAN frames and compare them with No. 15 byte and No. 16 byte of the received frame. Bit [15:13] is the user priority, bit [12] is the canonical format indicator, and bit [11:0] is the VLAN identifier of the VLAN tag. When the VLANTCOMP bit is set, only bit [11:0] is used for comparison. If VLANTID is all 0, the MAC does not check the VLAN tag comparison of No. 15 byte and No. 16 byte, and declares all frames with Type value of 0x8100 as VLAN frames. |
| 16    | VLANTCOMP | R/W | 12-bit VLAN Tag Comparison<br>When this bit is set, the VLAN identifier of bit 12 instead of the complete 16-bit VLAN tag will be used for comparison and filtering. The VLAN tag bit [11:0] is compared with the corresponding bit in the received VLAN tag frame.<br>When this bit is reset, all 16 bits of No. 15 and No. 16 bytes of the received VLAN frame will be used for comparison.                                                                                                                                                        |
| 31:17 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

### 27.5.9 Remote wake-up frame filter register (MAC\_REMWKUPFFL)

Offset address: 0x28

Reset value: 0x0000 0000

The application program will write/read the remote wake-up frame filter register through this address. In fact, the wake-up frame filter register is eight (opaque) wake-up frame filter registers. Eight continuous write operations to this address of the offset (0x0028) will write/read all wake-up frame filter registers. This register contains the high 16 bits of the seventh MAC address.

#### Wake-up frame filter register x (MAC\_WKUPFFLx) (x=0-3)

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | FLXBMASK | R/W | Filter x Byte Mask<br>This register defines which bytes of the frame are detected by the filter x to determine whether the frame is a wake-up frame.<br>MSB[31] must be zero. Bit y[30:0] is byte mask. If the bit y (the number of bytes) of byte mask is set to 1, the filter x offset + y of the incoming frame will be processed by the CRC module; otherwise, the filter x offset + y will be ignored. |

#### Wake-up frame filter register 4 (MAC\_WKUPFFL4)

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | FL0COM   | R/W | <p>Filter 0 Command</p> <p>This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.</p> |
| 7:4   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8  | FL1COM   | R/W | <p>Filter 1 Command</p> <p>This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.</p> |
| 15:12 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 19:16 | FL2COM   | R/W | <p>Filter 2 Command</p> <p>This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.</p> |
| 23:20 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 27:24 | FL3COM   | R/W | <p>Filter 3 Command</p> <p>This 4-bit command controls filter x operation. Bit 3 specifies the address type and defines the destination address type of the mode. When this bit is set to 1, the mode is applicable only to multicast frames. When this bit is reset, the mode is applicable only to unicast frames. Bit 2 and Bit 1 are reserved bits. Bit 0 is the enable bit of filter X; if bit 0 is set to 1, filter x will be enabled.</p> |
| 31:28 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

#### Wake-up frame filter register 5 (MAC\_WKUPFFL5)

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | FL0OFF | R/W | <p>Filter 0 Offset</p> <p>This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame).</p> |
| 15:8  | FL1OFF | R/W | <p>Filter 1 Offset</p> <p>This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame).</p> |

| Field | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                       |
|-------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:16 | FL2OFF | R/W | <b>Filter 2 Offset</b><br>This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame). |
| 31:24 | FL3OFF | R/W | <b>Filter 3 Offset</b><br>This register defines the offset (within the frame range) of the frame to be detected by the filter x. This 8-bit mode offset is the offset of the first byte of the filter x to be detected. The minimum allowable value is 12, which indicates the 13th byte of the frame (the offset value 0 indicates the first byte of the frame). |

#### Wake-up frame filter register 6 (MAC\_WKUPFFL6)

| Field | Name     | R/W | Description                                                                                                                                                          |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | FL0CRC16 | R/W | <b>Filter 0 CRC-16</b><br>This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module. |
| 31:16 | FL1CRC16 | R/W | <b>Filter 1 CRC-16</b><br>This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module. |

#### Wake-up frame filter register 7 (MAC\_WKUPFFL7)

| Field | Name     | R/W | Description                                                                                                                                                          |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | FL2CRC16 | R/W | <b>Filter 2 CRC-16</b><br>This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module. |
| 31:16 | FL3CRC16 | R/W | <b>Filter 3 CRC-16</b><br>This register contains the CRC_16 value calculated according to the mode, and the byte mask programmed for wake-up filter register module. |

### 27.5.10 PMT control and state register (MAC\_PMTCTRLSTS)

Offset address: 0x2C

Reset value: 0x0000 0000

This register will configure the wake-up time request and monitor the wake-up event.

| Field | Name     | R/W  | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | PD       | R/S  | Power Down<br>When this bit is set to 1, all received frames will be discarded. When receiving the magic packet or wake-up frame, this bit will be automatically cleared to zero and the power-down mode will be disabled. After this bit is cleared to zero, the received frame will be forwarded to the application program. This bit can be set to 1 only when the magic packet is enabled or the wake-up frame bit is set to 1. |
| 1     | MPEN     | R/W  | Magic Packet Enable<br>When this bit is set to 1, this bit will enable the power management event generated due to receiving of a magic packet.                                                                                                                                                                                                                                                                                     |
| 2     | WKUPFEN  | R/W  | Wakeup Frame Enable<br>When this bit is set to 1, this bit will enable the power management event generated due to receiving of a wake-up frame.                                                                                                                                                                                                                                                                                    |
| 4:3   | Reserved |      |                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 5     | MPRX     | RC_R | Magic Packet Received<br>When this bit is set to 1, it indicates that the power management event is generated due to receiving of a magic packet. This bit can be cleared to zero by reading the register.                                                                                                                                                                                                                          |
| 6     | WKUPFRX  | RC_R | Wakeup Frame Received<br>When this bit is set to 1, it indicates that the power management event is generated due to receiving of a wake-up frame. This bit can be cleared to zero by reading the register.                                                                                                                                                                                                                         |
| 8:7   | Reserved |      |                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9     | GUN      | R/W  | Global Unicast<br>When this bit is set to 1, it will enable any filtered unicast packet confirmed by MAC address to a wake-up frame.                                                                                                                                                                                                                                                                                                |
| 30:10 | Reserved |      |                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 31    | WKUPFRST | R/S  | Wakeup Frame Filter Register Pointer Reset<br>When this bit is set to 1, it will reset the remote wake-up frame filter register pointer to 000b. It will be automatically cleared to zero after 1 clock cycle.                                                                                                                                                                                                                      |

### 27.5.11 Debug register (MAC\_DBG)

Offset address: 0x34

Reset value: 0x0000 0000

This register gives the status of all main modules of transmitting and receiving data path and FIFO. When it is set to all zero, it indicates that the MAC core is idle (FIFO is empty) and there is no activity in the data path.

| Field | Name   | R/W | Description                                                                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | RPESTS | R   | MAC MII Receive Protocol Engine Status<br>When set to high, it indicates that the MAC MII receiving protocol engine is actively receiving data instead of in IDLE state. |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                     |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:1   | RFCFCSTS | R   | MAC Receive Frame FIFO Controller Status<br>When set to high, it indicates that the FIFO read/write controller of the MAC receive frame FIFO controller is active.<br>0: Write controller status<br>1: Read controller status                   |
| 3     | Reserved |     |                                                                                                                                                                                                                                                 |
| 4     | RWCSTS   | R   | RX FIFO Write Controller Active Status<br>When set to high, it indicates that the RX FIFO write controller is valid and transmitting the received frame to FIFO.                                                                                |
| 6:5   | RRCSTS   | R   | RX FIFO Read Controller State<br>00: IDLE state<br>01: Read frame data<br>10: Read frame status (or timestamp)<br>11: Refresh frame data and status                                                                                             |
| 7     | Reserved |     |                                                                                                                                                                                                                                                 |
| 9:8   | RXFSTS   | R   | RX FIFO full - level Status<br>00: RX FIFO is empty<br>01: RX FIFO fill level is below the flow control failure threshold<br>10: RX FIFO fill level is above the flow control activation threshold<br>11: RX FIFO is full                       |
| 15:10 | Reserved |     |                                                                                                                                                                                                                                                 |
| 16    | TPESTS   | R   | MAC MII Transmit Protocol Engine Status<br>When set to high, it indicates that the MAC MII transmitting protocol engine is actively transmitting data instead of in idle state.                                                                 |
| 18:17 | TFCSTS   | R   | MAC Transmit Frame Controller Status<br>00: IDLE state<br>01: Wait for the previous frame or IFG or return to the state of end of rollback cycle<br>10: Generate and transmit the pause frame (in full-duplex mode)<br>11: Transmit input frame |
| 19    | TXPAUSED | R   | MAC Transmitter in Pause<br>When set to high, it indicates that the MAC transmitter is in a pause state (in full-duplex mode), so no frames will be transmitted.                                                                                |
| 21:20 | TRCSTS   | R   | TX FIFO Read Controller Status<br>00: IDLE state<br>01: Read status (transmit data to MAC transmitter)<br>10: Wait for TX status from MAC transmitter<br>11: Write the received TX status or refresh TX FIFO                                    |
| 22    | TWCSTS   | R   | TX FIFO Write Controller Status<br>When set to high, it indicates that TX FIFO write controller is active and transmitting data to TX FIFO.                                                                                                     |
| 23    | Reserved |     |                                                                                                                                                                                                                                                 |
| 24    | TXFSTS   | R   | TX FIFO Not Empty Status<br>When set to high, it indicates that TX FIFO is not empty and there are still some data waiting to be transmitted.                                                                                                   |



| Field | Name      | R/W | Description                                                                                                                                    |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------|
| 25    | TXSTSFSTS | R   | TX Status FIFO Full Status<br>When set to high, it indicates that TX FIFO is full. Therefore, no more frames can be received for transmission. |
| 31:26 | Reserved  |     |                                                                                                                                                |

### 27.5.12 Interrupt state register (MAC\_ISTS)

Offset address: 0x38

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                     |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | Reserved |     |                                                                                                                                                                                                                                 |
| 3     | PMTIS    | R   | PMT Interrupt Status<br>This bit is set when a magic packet or remote wake-up frame is received in power-off mode. When bit [6:5] is cleared due to read operation of PMT control and state register, this bit will be cleared. |
| 4     | MMCIS    | R   | MMC Interrupt Status<br>When any bit [6:5] is set to high, this bit will be set to high and it can be cleared only when all these bits are low.                                                                                 |
| 5     | MMCRXIS  | R   | MMC Receive Interrupt Status<br>When an interrupt is generated in the MMC receive interrupt register, this bit will be set to high. When all bits in the interrupt register are cleared, this bit will also be cleared.         |
| 6     | MMCTXIS  | R   | MMC Transmit Interrupt Status<br>When an interrupt is generated in the MMC transmit interrupt register, this bit will be set to high. When all bits in the interrupt register are cleared, this bit will also be cleared.       |
| 8:7   | Reserved |     |                                                                                                                                                                                                                                 |
| 9     | TSIS     | R   | Timestamp Interrupt Status<br>When the system time value is equal to or exceeds the value specified in the target time register, this bit will be set to 1. It will be cleared to zero when reading this register.              |
| 15:10 | Reserved |     |                                                                                                                                                                                                                                 |

### 27.5.13 Interrupt mask register (MAC\_IMASK)

Offset address: 0x3C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                      |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0   | Reserved |     |                                                                                                                                                                                  |
| 3     | PMTIM    | R/W | PMT Interrupt Mask<br>When this bit is set, the PMT interrupt status bit is set in the register "interrupt state register", so this bit disables generation of interrupt signal. |
| 8:4   | Reserved |     |                                                                                                                                                                                  |

| Field | Name     | R/W | Description                                                                                                        |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------|
| 9     | TSTIM    | R/W | Time Stamp Trigger Interrupt Mask<br>If this bit is set to 1, generation of timestamp interrupts will be disabled. |
| 15:10 | Reserved |     |                                                                                                                    |

#### 27.5.14 MAC address 0 high register (MAC\_ADDR0H)

Offset address: 0x40

Reset value: 0x8000 FFFF

| Field | Name     | R/W | Description                                                                                                                                                                                                                                      |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | ADDR0H   | R/W | MAC Address 0 High Bit [47:32]<br>It contains the first 16 bits (47:32) of the first 6 bytes of MAC address 0. The MAC uses this field to filter the received frames and inserts the MAC address in the transmission flow control (pause) frame. |
| 30:16 | Reserved |     |                                                                                                                                                                                                                                                  |
| 31    | AL1      | R   | Always 1                                                                                                                                                                                                                                         |

#### 27.5.15 MAC address 0 low register (MAC\_ADDR0L)

Offset address: 0x44

Reset value: 0xFFFF FFFF

| Field | Name   | R/W | Description                                                                                                                                                                                                                                       |
|-------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | ADDR0L | R/W | MAC Address 0 Low Bit [31:0]<br>This bit field contains the low 32 bits of the first 6-byte MAC address 0. This is the frame used by MAC to filter the received frames and insert the MAC address in the transmission flow control (pause) frame. |

#### 27.5.16 MAC address 1 high register (MAC\_ADDR1H)

Offset address: 0x48

Reset value: 0x0000 FFFF

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | ADDR1H    | R/W | MAC Address 1 High Bit [47:32]<br>It contains the first 16 bits (47:32) of the first 6-byte MAC address 1. The MAC uses this field to filter the received frames and inserts the MAC address in the transmission flow control (pause) frame.                                                                                                                                                                        |
| 23:16 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 29:24 | MASKBCTRL | R/W | Mask Byte Control<br>These bits are used to compare the mask control bits of 1 byte of each MAC address. When they are set to high level, the MAC core will not compare the corresponding bytes of the received DA/SA with the contents of the MAC address 1 register. Each bit is used to control the mask of bytes, as follows:<br>Bit 29: ADDR1H [15:8]<br>Bit 28: ADDR1H [7:0]<br>Bit 27: ADDR1L [31:24]<br>... |

| Field | Name    | R/W | Description                                                                                                                                                                  |
|-------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |         |     | Bit 24: ADDR1L [7:0]                                                                                                                                                         |
| 30    | ADDRSEL | R/W | Address Select<br>0: Compare the MAC address 1 [47:0] with the DA field of the received frame<br>1: Compare the MAC address 1 [47:0] with the SA field of the received frame |
| 31    | ADDREN  | R/W | Address Enable<br>0: The address filter will ignore the address used for filtering<br>1: The address filter uses the MAC address 1 for filtering                             |

### 27.5.17 MAC address 1 low register (MAC\_ADDR1L)

Offset address: 0x4C

Reset value: 0xFFFF FFFF

| Field | Name   | R/W | Description                                                                                                                                                                                                                      |
|-------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | ADDR1L | R/W | MAC Address 1 Low Bit [31:0]<br>This bit field contains the low 32 bits of the first 6-byte MAC address 1. If the application does not load the content of this bit field after initialization, the content will not be defined. |

### 27.5.18 MAC address 2 high register (MAC\_ADDR2H)

Offset address: 0x50

Reset value: 0x0000 FFFF

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | ADDR2H    | R/W | MAC address 2 high bit [47:32] (MAC Address 2)<br>It contains the first 16 bits (47:32) of the first 6 bytes of MAC address 2.                                                                                                                                                                                                                                                                                                               |
| 23:16 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 29:24 | MASKBCTRL | R/W | Mask Byte Control<br>These bits are used to compare the mask control bits of 2 bytes of each MAC address. When they are set to high level, the MAC core will not compare the corresponding bytes of the received DA/SA with the contents of the MAC address 2 register. Each bit is used to control the mask of bytes, as follows:<br>Bit 29: ADDR2H [15:8]<br>Bit 28: ADDR2H [7:0]<br>Bit 27: ADDR2L [31:24]<br>...<br>Bit 24: ADDR2L [7:0] |
| 30    | ADDRSEL   | R/W | Address Select<br>0: Compare the MAC address 2 [47:0] with the DA field of the received frame<br>1: Compare the MAC address 2 [47:0] with the SA field of the received frame                                                                                                                                                                                                                                                                 |
| 31    | ADDREN    | R/W | Address Enable<br>0: The address filter will ignore the address used for filtering<br>1: The address filter uses the MAC address 2 for filtering                                                                                                                                                                                                                                                                                             |

### 27.5.19 MAC address 2 low register (MAC\_ADDR2L)

Offset address: 0x54

Reset value: 0xFFFF FFFF

| Field | Name   | R/W | Description                                                                                                                                                                                                                                      |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | ADDR2L | R/W | MAC Address 2 low bit [31:0] (MAC Address 2)<br>This bit field contains the low 32 bits of the first 6-byte MAC address 2. If the application does not load the content of this bit field after initialization, the content will not be defined. |

### 27.5.20 MAC address 3 high register (MAC\_ADDR3H)

Offset address: 0x58

Reset value: 0x0000 FFFF

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | ADDR3H    | R/W | MAC address 3 high bit [47:32] (MAC Address 3)<br>It contains the first 16 bits (47:32) of the first 6-byte MAC address 3.                                                                                                                                                                                                                                                                                                                   |
| 23:16 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 29:24 | MASKBCTRL | R/W | Mask Byte Control<br>These bits are used to compare the mask control bits of 3 bytes of each MAC address. When they are set to high level, the MAC core will not compare the corresponding bytes of the received DA/SA with the contents of the MAC address 3 register. Each bit is used to control the mask of bytes, as follows:<br>Bit 29: ADDR3H [15:8]<br>Bit 28: ADDR3H [7:0]<br>Bit 27: ADDR3L [31:24]<br>...<br>Bit 24: ADDR3L [7:0] |
| 30    | ADDRSEL   | R/W | Address Select<br>0: Compare the MAC address 3 [47:0] with the DA field of the received frame<br>1: Compare the MAC address 3 [47:0] with the SA field of the received frame                                                                                                                                                                                                                                                                 |
| 31    | ADDREN    | R/W | Address Enable<br>0: The address filter will ignore the address used for filtering<br>1: The address filter uses the MAC address 3 for filtering                                                                                                                                                                                                                                                                                             |

### 27.5.21 MAC address 3 low register (MAC\_ADDR3L)

Offset address: 0x5C

Reset value: 0xFFFF FFFF

| Field | Name   | R/W | Description                                                                                                                                                                                                                                      |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | ADDR3L | R/W | MAC Address 3 low bit [31:0] (MAC Address 3)<br>This bit field contains the low 32 bits of the first 6-byte MAC address 3. If the application does not load the content of this bit field after initialization, the content will not be defined. |

## 27.6 MMC register address mapping

Table 141 MMC Register Address Mapping

| Register name | Description                                               | Offset address |
|---------------|-----------------------------------------------------------|----------------|
| MMC_CTRL      | Control register                                          | 0x100          |
| MMC_RXINT     | Receive interrupt register                                | 0x104          |
| MMC_TXINT     | Transmit interrupt register                               | 0x108          |
| MMC_RXINTMASK | Mask receive interrupt register                           | 0x10C          |
| MMC_TXINTMASK | Mask transmit interrupt register                          | 0x110          |
| MMC_TXGFSCCNT | Transmitted good frames single collision counter register | 0x14C          |
| MMC_TXGFMCCNT | Transmitted good frames more collision counter register   | 0x150          |
| MMC_TXGFCNT   | Transmitted good frames counter register                  | 0x168          |
| MMC_RXFCECNT  | Received Frames CRC Error Counter register                | 0x194          |
| MMC_RXFAECNT  | Received frame alignment error counter register           | 0x198          |
| MMC_RXGUNCNT  | Received good unicast frame counter register              | 0x1C4          |

## 27.7 MMC register functional description

### 27.7.1 Control register (MMC\_CTRL)

Offset address: 0x100

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                                                            |
|-------|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CNTRST    | R/W | Counter Reset<br>When this bit is set, all counters will be reset. This bit will be automatically cleared to zero after 1 clock cycle                                                                                                                  |
| 1     | CNTSTOPRO | R/W | Counter Stop Rollover<br>When this bit is set, the counter will not return to zero when it reaches its maximum value.                                                                                                                                  |
| 2     | RSTOR     | R/W | Reset on Read<br>When this bit is set, after reading the MMC counter, this counter will be reset. The counter will be cleared to zero after reading the least significant byte channel.                                                                |
| 3     | MCNTF     | R/W | MMC Counter Freeze<br>When this bit is set, all MMC counters will be frozen so that they remain at the current value. (Only after this bit is cleared to zero, will the MMC counter be updated due to the existence of transmitted or received frames) |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4     | MCNTP    | R/W | MMC Counter Preset<br>When this bit is set to 1, all counters will be preset to either almost the maximum value or almost half the value based on the value of the MCNTVALP bit. This bit will be automatically cleared to zero after 1 clock cycle. This bit, together with the MCNTVALP bit, is used to debug and test the interrupts caused by the MMC counter reaching half, full, or maximum values. |
| 5     | MCNTVALP | R/W | MMC Counter Value Preset<br>When MCNTP bit is set to 1:<br>When MCNTVALP is low, all MMC counters will be preset to almost half the value. All frame counters are preset to 0x7FFF_FFF0 (half value -16).<br>When MCNTVALP is high, all MMC counters will be preset to almost full value. All frame counters are preset to 0xFFFF_FFF0 (full value -16).                                                  |
| 31:6  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                           |

### 27.7.2 Receive interrupt register (MMC\_RXINT)

Offset address: 0x104

Reset value: 0x0000 0000

| Field | Name     | R/W  | Description                                                                                                                                            |
|-------|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | Reserved |      |                                                                                                                                                        |
| 5     | RXFCE    | RC_R | Received Frames CRC Errors<br>This bit will be set when the received frame counter has a CRC error and reaches half of its maximum value.              |
| 6     | RXFAE    | RC_R | Received Frames Alignment Errors<br>This bit will be set when the received frame counter has an alignment error and reaches half of its maximum value. |
| 16:7  | Reserved |      |                                                                                                                                                        |
| 17    | RXGUNF   | RC_R | Received Good Unicast Frames<br>This bit will be set when the received good unicast frame counter reaches half of its maximum value.                   |
| 31:18 | Reserved |      |                                                                                                                                                        |

### 27.7.3 Transmit interrupt register (MMC\_TXINT)

Offset address: 0x108

Reset value: 0x0000 0000

| Field | Name     | R/W  | Description                                                                                                                                                              |
|-------|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13:0  | Reserved |      |                                                                                                                                                                          |
| 14    | TXGFSCOL | RC_R | Transmitted Good Frames Single Collision<br>This bit will be set when the good frame counter transmitted after a single collision reaches half of its maximum value.     |
| 15    | TXGFMCOL | RC_R | Transmitted Good Frames More Single Collision<br>This bit will be set when the good frame counter transmitted after multiple collisions reach half of its maximum value. |

| Field | Name     | R/W  | Description                                                                                                                |
|-------|----------|------|----------------------------------------------------------------------------------------------------------------------------|
| 20:16 | Reserved |      |                                                                                                                            |
| 21    | TXGF     | RC_R | Transmitted Good Frames<br>This bit will be set when the transmitted good frame counter reaches half of its maximum value. |
| 31:22 | Reserved |      |                                                                                                                            |

#### 27.7.4 Mask receive interrupt register (MMC\_RXINTMASK)

Offset address: 0x10C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                              |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | Reserved |     |                                                                                                                                                                                          |
| 5     | RXFCEM   | R/W | Received Frames CRC Error Mask<br>When this bit is set, the interrupt will be masked when the received frame counter has a CRC error and reaches half of its maximum value.              |
| 6     | RXFAEM   | R/W | Received Frames Alignment Error Mask<br>When this bit is set, the interrupt will be masked when the received frame counter has an alignment error and reaches half of its maximum value. |
| 16:7  | Reserved |     |                                                                                                                                                                                          |
| 17    | RXGUNFM  | R/W | Received Good Unicast Frames Mask<br>When this bit is set, the interrupt will be masked when the received good unicast frame counter reaches half of its maximum value.                  |
| 31:18 | Reserved |     |                                                                                                                                                                                          |

#### 27.7.5 Mask transmit interrupt register (MMC\_TXINTMASK)

Offset address: 0x110

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                   |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13:0  | Reserved  |     |                                                                                                                                                                                                               |
| 14    | TXGFSCOLM | R/W | Transmitted Good Frames Single Collision Mask<br>When this bit is set, the interrupt will be masked when the good frame counter transmitted after single collision reaches half of its maximum value.         |
| 15    | TXGFMCOLM | R/W | Transmitted Good Frames More Single Collision Mask<br>When this bit is set, the interrupt will be masked when the good frame counter transmitted after multiple collisions reaches half of its maximum value. |
| 20:16 | Reserved  |     |                                                                                                                                                                                                               |
| 21    | TXGFM     | R/W | Transmitted Good Frames Mask<br>When this bit is set, the interrupt will be masked when the transmitted good frame counter reaches half of its maximum value.                                                 |
| 31:22 | Reserved  |     |                                                                                                                                                                                                               |

### 27.7.6 Transmitted good frames single collision counter register (MMC\_TXGFSCCNT)

Offset address: 0x14C

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                      |
|-------|-----------|-----|--------------------------------------------------|
| 31:0  | TXGFSCCNT | R   | Transmitted Good Frames Single Collision Counter |

### 27.7.7 Transmitted good frames more collision counter register (MMC\_TXGFMCCNT)

Offset address: 0x150

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                    |
|-------|-----------|-----|------------------------------------------------|
| 31:0  | TXGFMCCNT | R   | Transmitted Good Frames More Collision Counter |

### 27.7.8 Transmitted good frames counter register (MMC\_TXGFCNT)

Offset address: 0x168

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                     |
|-------|---------|-----|---------------------------------|
| 31:0  | TXGFCNT | R   | Transmitted Good Frames Counter |

### 27.7.9 Received Frames CRC Error Counter register (MMC\_RXFCECNT)

Offset address: 0x194

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                       |
|-------|----------|-----|-----------------------------------|
| 31:0  | RXFCECNT | R   | Received Frames CRC Error Counter |

### 27.7.10 Received frame alignment error counter register (MMC\_RXFAECNT)

Offset address: 0x198

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                             |
|-------|----------|-----|-----------------------------------------|
| 31:0  | RXFAECNT | R   | Received Frames Alignment Error Counter |

### 27.7.11 Received good unicast frame counter register (MMC\_RXGUNCNT)

Offset address: 0x1C4

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                          |
|-------|----------|-----|--------------------------------------|
| 31:0  | RXGUNCNT | R   | Received Good Unicast Frames Counter |

## 27.8 PTP register address mapping

Used to support the register of precision network clock synchronization which is



in accordance with IEEE 1588 standard.

Table 142 PTP Register Address Mapping

| Register name | Description                        | Offset address |
|---------------|------------------------------------|----------------|
| PTP_TSCTRL    | Timestamp control register         | 0x700          |
| PTP_SUBSECI   | Subsecond increment register       | 0x704          |
| PTP_TSH       | Timestamp high bit register        | 0x708          |
| PTP_TSL       | Timestamp low bit register         | 0x70C          |
| PTP_TSHUD     | Timestamp high bit update register | 0x710          |
| PTP_TSLUD     | Timestamp low bit update register  | 0x714          |
| PTP_TSA       | Timestamp addend register          | 0x718          |
| PTP_TTSH      | Target timestamp high bit register | 0x71C          |
| PTP_TTSL      | Target timestamp low bit register  | 0x720          |
| PTP_TSSTS     | Timestamp state register           | 0x728          |
| PTP_PPSCTRL   | PPS control register               | 0x72C          |

## 27.9 PTP register functional description

### 27.9.1 Timestamp control register (PTP\_TSCTRL)

Offset address: 0x700

Reset value: 0x0000 2000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                       |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TSEN     | R/W | Time Stamp Enable<br>0: Disable<br>1: Enable<br>Since the maintained system time is suspended, after this bit is set to high level, it will be always necessary to initialize the timestamp function (system time).                                                                                               |
| 1     | TSUDSEL  | R/W | Time Stamp Update Mode Select<br>Select the method of updating the system timestamp<br>0: Rough update<br>1: Precision update                                                                                                                                                                                     |
| 2     | TSSTINIT | R/W | Time Stamp System Time Initialize<br>When this bit is set, the system time will be initialized with the value specified in the timestamp high-bit update register and timestamp low-bit update register. Before this bit is set, it must be read as zero. After initialization, this bit will be cleared to zero. |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3     | TSSTUD   | R/W | Time Stamp System Time Update<br>When this bit is set, the system time will be updated with the value specified in the timestamp high-bit update register and timestamp low-bit update register. TSSTINIT and TSSTUD must be read as zero before this bit is set. After the update is completed, this bit will be cleared to zero.                                                                       |
| 4     | TSTRGIEN | R/W | Time Stamp Trigger Interrupt Enable<br>When this bit is set, if the value written in the target time register is less than the system time, a timestamp interrupt will be generated. This bit will be cleared to zero when a timestamp interrupt is triggered.                                                                                                                                           |
| 5     | TSADDUD  | R/W | Time Stamp Addend Register Update<br>When this bit is set, the contents of the timestamp addend register will be updated to PTP for precision calibration. After the update is completed, this bit will be cleared to zero. Before this bit is set, it must be read as zero.                                                                                                                             |
| 7:6   | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| 8     | TSSNEN   | R/W | Time Stamp Snapshot for Received Frames Enable<br>When this bit is set, all frames received by the core will enable timestamp snapshot.                                                                                                                                                                                                                                                                  |
| 9     | TSSUBRO  | R/W | Time Stamp Subsecond Rollover<br>0: The rollover value of the subsecond register reaches 0x7FFF FFFF. The subsecond increment is programmed according to the PTP reference clock frequency and the value of this bit.<br>1: If the subsecond counter value reaches 0x3B9A C9FF (decimal 999 999 999) and the number of timestamp (high-bit) seconds increases, the timestamp low-bit register will flip. |
| 10    | LISTVSEL | R/W | Listening Version Select<br>Select the version format of listening PTP packet<br>0: Version 1<br>1: Version 2                                                                                                                                                                                                                                                                                            |
| 11    | TSSPTPEN | R/W | Time Stamp Snapshot for PTP Ethernet Frames Enable<br>When this bit is set, the timestamp snapshot of the frame containing PTP message in the Ethernet frame will be taken. By default, take the snapshot of UDP IP Ethernet PTP packets.                                                                                                                                                                |
| 12    | TSS6EN   | R/W | Time stamp snapshot for IPv6 frames Enable<br>When this bit is set, the timestamp snapshot of IPv6 frames will be taken.                                                                                                                                                                                                                                                                                 |
| 13    | TSS4EN   | R/W | Time Stamp Snapshot for IPv4 Frames Enable<br>When this bit is set, the timestamp snapshot of IP4 frames will be taken.                                                                                                                                                                                                                                                                                  |
| 14    | TSSMESEL | R/W | Time Stamp Snapshot for Message Select<br>0: Take snapshots of all messages except Announce, Management and Signaling<br>1: Take a timestamp snapshot of the event message (SYNC、Delay_Re, Pdelay_Req or Pdelay_Resp)                                                                                                                                                                                    |

| Field | Name         | R/W | Description                                                                                                                                                                       |
|-------|--------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | TSSMNSEL     | R/W | Time Stamp Snapshot for Master Node Select<br>0: Slave node<br>1: Master node                                                                                                     |
| 17:16 | TSCLKNSEL    | R/W | Time stamp Clock Node Select<br>00: Ordinary clock<br>01: Boundary clock<br>10: End-to-end transparent clock<br>11: Point-to-point transparent clock                              |
| 18    | TSSPTPFMACEN | R/W | Time Stamp PTP Frame Filtering MAC Address Enable<br>When this bit is set and PTP is transmitted directly through Ethernet, this bit will filter PTP frames by using MAC address. |
| 31:19 | Reserved     |     |                                                                                                                                                                                   |

Table 143 Timestamp Snapshot Message

| TSCLKNSEL | TSSMNSEL   | TSSMESEL | Snapshot message                                                |
|-----------|------------|----------|-----------------------------------------------------------------|
| 0X        | Irrelevant | 0        | SYNC, Follow_Up, Delay_Req, Delay_Resp                          |
|           | 1          | 1        | Delay_Req                                                       |
|           | 0          | 1        | SYNC                                                            |
| 10        | x          | 0        | SYNC, Follow_Up, Delay_Req, Delay_Resp                          |
|           |            | 1        | SYNC, Follow_Up                                                 |
| 11        |            | 0        | SYNC, Follow_Up, Delay_Req, Delay_Resp, Pdelay_Req, Pdelay_Resp |
|           |            | 1        | SYNC, Pdelay_Req, Pdelay_Resp                                   |

Note: x=not applicable

### 27.9.2 Subsecond increment register (PTP\_SUBSECI)

Offset address: 0x704

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                         |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------|
| 7:0   | STSUBSECI | R/W | System Time Subseconds Increment<br>It will be added to the system time subsecond value at the time of each update. |
| 31:8  | Reserved  |     |                                                                                                                     |

### 27.9.3 Timestamp high bit register (PTP\_TSH)

Offset address: 0x708

Reset value: 0x0000 0000

| Field | Name  | R/W | Description                                     |
|-------|-------|-----|-------------------------------------------------|
| 31:0  | STSEC | R   | System Time Second Value<br>System second time. |

### 27.9.4 Timestamp low bit register (PTP\_TSL)

Offset address: 0x70C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                             |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30:0  | STSUBSEC | R   | System Time Subseconds Value<br>System subsecond time, with precision of 0.46ns.                                                                                                                        |
| 31    | STSEL    | R   | System Time Select<br>This bit indicates positive and negative values of the system time.<br>0: Positive<br>1: Negative<br>Since the system time should always be positive, this bit is generally zero. |

### 27.9.5 Timestamp high bit update register (PTP\_TSHUD)

Offset address: 0x710

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                      |
|-------|---------|-----|--------------------------------------------------------------------------------------------------|
| 31:0  | TSUDSEC | R/W | Time Stamp Update Second Value<br>The second time to be initialized or added to the system time. |

### 27.9.6 Timestamp low bit update register (PTP\_TSLUD)

Offset address: 0x714

Reset value: 0x0000 0000

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30:0  | TSUDSUBSEC | R/W | Time Stamp Update Subseconds Value<br>The subsecond time to be initialized or added to the system time.<br>The precision is 0.46ns.                                                                                                                                                                                                                                        |
| 31    | TSUDSEL    | R/W | Time Stamp Update Select<br>This bit indicates positive and negative values of the system time.<br>0: Positive<br>1: Negative<br>When TSSTINIT bit is set, this bit is 0. When TSSTUD bit and this bit are set to 1 at the same time, the value of the timestamp update register shall be subtracted from the system time. Otherwise, it will be added to the system time. |

### 27.9.7 Timestamp addend register (PTP\_TSA)

Offset address: 0x718

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                              |
|-------|------|-----|--------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TSA  | R/W | Time Stamp Addend Value<br>The 32-bit time value to be added to the accumulator register, used for time synchronization. |

### 27.9.8 Target timestamp high bit register (PTP\_TTSH)

Offset address: 0x71C

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                  |
|-------|------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TTSH | R/W | Target Time Stamp High Value<br>Storage second time. When the value of the timestamp matches or exceeds two target timestamp registers at the same time, the MAC will generate an interrupt. |

### 27.9.9 Target timestamp low bit register (PTP\_TTSL)

Offset address: 0x720

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                     |
|-------|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TTSL | R/W | Target Time Stamp Low Value<br>Storage nanosecond time. When the value of the timestamp matches or exceeds two target timestamp registers at the same time, the MAC will generate an interrupt. |

### 27.9.10 Timestamp state register (PTP\_TSSTS)

Offset address: 0x728

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                               |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TSSECOVR | R   | Time Stamp Second Value Overflow<br>When this bit is set, the second value of the timestamp has overflowed, exceeding 0xFFFF FFFF.        |
| 1     | TTSRD    | R   | Target Time Stamp Value Reached<br>When this bit is set, the system time value is greater than or equal to the value of PTP_TTS register. |
| 31:2  | Reserved |     |                                                                                                                                           |

### 27.9.11 PPS control register (PTP\_PPSCTRL)

Offset address: 0x72C

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|---------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0   | PPSFSEL | R   | PPS Frequency Selection<br>PPS output frequency is set to $2^{\text{PPSFSEL}}$ Hz<br>0000: 1Hz; the binary flip pulse width is 125ms, and the digital flip pulse width is 100ms<br>0001: 2Hz, binary flip; the duty cycle is 50% (digital flip is not recommended)<br>0010: 4Hz, binary flip; the duty cycle is 50% (digital flip is not recommended)<br>0011: 8Hz, binary flip; the duty cycle is 50% (digital flip is not recommended)<br>0100: 16Hz, binary flip; the duty cycle is 50% (digital flip is not recommended)<br>...<br>1111: 32768Hz, binary flip; the duty cycle is 50% (digital flip is not recommended) |

| Field | Name     | R/W | Description                                                                                                                                                          |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | Note: As PPS output has irregular waveform at higher frequency, do not use the PPS output with frequency other than 1Hz as much as possible when using digital flip. |
| 31:4  | Reserved |     |                                                                                                                                                                      |

## 27.10 DMA register address mapping

Table 144 DMA Register Address Mapping

| Register name   | Description                                       | Offset address |
|-----------------|---------------------------------------------------|----------------|
| ETH_DMABMOD     | DMA mode register                                 | 0x1000         |
| ETH_DMATXPD     | Transmit poll demand register                     | 0x1004         |
| ETH_DMARXPD     | Receive poll demand register                      | 0x1008         |
| ETH_DMARXDLADDR | Receive descriptor list address register          | 0x100C         |
| ETH_DMATXDLADDR | Transmit descriptor list address register         | 0x1010         |
| ETH_DMASTS      | State register                                    | 0x1014         |
| ETH_DMAOPMOD    | Operation mode register                           | 0x1018         |
| ETH_DMAINTEN    | Interrupt enable register                         | 0x101C         |
| ETH_DMAMFABOcnt | Missed frame and buffer overflow counter register | 0x1020         |
| ETH_DMARXFLGWDt | Receive interrupt watchdog timer register         | 0x1024         |
| ETH_DMAHTXD     | Current host transmit descriptor register         | 0x1048         |
| ETH_DMAHRXD     | Current host receive descriptor register          | 0x104C         |
| ETH_DMAHTXBADDR | Current host transmit buffer address register     | 0x1050         |
| ETH_DMAHRXBADDR | Current host receive buffer address register      | 0x1054         |

## 27.11 DMA register functional description

### 27.11.1 DMA bus mode register (ETH\_DMABMOD)

Offset address: 0x1000

Reset value: 0x0002 0101

| Field | Name | R/W | Description                                                                                                                                                                                                                                                       |
|-------|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | SWR  | R/W | Software Reset<br>When this bit is set, the MAC DMA controller will reset the MAC logic and all internal registers. It will be cleared automatically after all clock domains are reset. You should read a 0 value in this bit before reprogramming any registers. |
| 1     | DAS  | R/W | DMA Arbitration Scheme<br>It specifies the arbitration scheme between the transmitting and receiving paths of channel 0.<br>0: Weighted round robin scheduling of Rx:Tx is used, given in [15:14]                                                                 |

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |       |     | 1: The priority of Rx is higher than that of Tx                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 6:2   | DSL   | R/W | <p>Descriptor Skip Length</p> <p>This bit specifies the number of Word, Dword, or Lword skipped between two unlinked descriptors Address skip starts from the end of the current descriptor to the beginning of the next descriptor. When the DSL value is equal to 0, DMA will regard the descriptor table as continuous in ring mode.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 7     | EDFEN | R/W | <p>Enhanced Descriptor Format Enable</p> <p>When this bit is set, enable the enhanced descriptor format and increase the descriptor size to 32 bytes. If the timestamp function or IPv4 checksum offload has been activated, this bit must be set to 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 13:8  | PBL   | R/W | <p>Programmable Burst Length</p> <p>These bits indicate the maximum number of beats to be transmitted in a DMA transaction. This is the maximum value used in a single block read and write. Each time the burst transmission is started on the host bus, DMA will always attempt to follow the burst specified in PBL. PBL can be programmed with allowable value 1, 2, 4, 8, 16 and 32. Any other value may result in undefined behaviors. When USP is set to high level, the PBL value is only applicable to Tx DMA transactions.</p> <p>The PBL value has the following limitations: the maximum number of possible beats is limited by the size of Tx FIFO and Rx FIFO of MTL layer and the width of data bus on DMA. FIFO has a limitation, namely, the maximum beat supported is half the FIFO depth unless specified.</p> |
| 15:14 | PR    | R/W | <p>Priority Ratio</p> <p>These bits control the priority ratio of weighted round robin arbitration between Rx direct memory access and Tx direct memory access. These bits are valid only when bit [1] is reset.</p> <p>00: Priority ratio is 1:1<br/> 01: Priority ratio is 2:1<br/> 10: Priority ratio is 3:1<br/> 11: Priority ratio is 4:1</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 16    | FB    | R/W | <p>Fixed Burst</p> <p>This bit controls whether the AHB main interface performs fixed burst transmission. After it is set, at the beginning of normal burst transmission, the AHB interface only uses SINGLE, INCR4, INCR8 or INCR16. When it is reset, the AHB interface uses single and INCR burst transmission operations.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 22:17 | RPBL  | R/W | <p>Receive DMA programmable burst length (Rx DMA PBL)</p> <p>This bit field indicates the maximum number of beats to transmitted in a Rx DMA transaction. This is the maximum value used in a single block read and write.</p> <p>Each time the burst transmission is started on the host bus, Rx DMA will always attempt to follow the burst specified in RPBL. RPBL can be programmed with allowable value 1, 2, 4, 8, 16 and 32. Any other value may result in undefined behaviors.</p> <p>This field is valid only when USP is set to high level.</p>                                                                                                                                                                                                                                                                         |
| 23    | USP   | R/W | <p>Use Separate PBL</p> <p>When set to high level, this bit configures Rx DMA using the value configured in bit [22:17] as PBL. The PBL value in bit [13:8] is applicable only to Tx DMA operations.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | When reset to low level, the PBL value in bit [13:8] is applicable to two kinds of DMA engines.                                                                                                                                                                                                                                                            |
| 24    | PBLx4    | R/W | <b>PBLx4 Mode</b><br>When set to high level, this bit will multiply the programmed PBL value by four times. Therefore, the DMA will transmit data at a maximum beam number of 4, 8, 16, 32, 64 and 128 according to the PBL value.                                                                                                                         |
| 25    | AAL      | R/W | <b>Address-Aligned Beats</b><br>When this bit is set to high level and the FB bit is equal to 1, the AHB interface will generate all bursts aligned with the LS bit of the start address. If the FB bit is equal to 0, the first burst (the start address of the access data buffer) is misaligned, but the subsequent bursts are aligned to this address. |
| 26    | MB       | R/W | <b>Mixed Burst</b><br>When this bit is set to high level and the FB bit is set to low level, the AHB main interface will start all burst INCR with a length of more than 16, and it will recover to a fixed burst with a burst length of 16 or less.                                                                                                       |
| 31:27 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                            |

### 27.11.2 Transmit poll demand register (ETH\_DMATXPD)

Offset address: 0x1004

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                  |
|-------|------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TXPD | R/W | <b>Transmit Poll Demand</b><br>When these bits are written with any value, DMA will read the current descriptor pointed to by the ETH_DMAHTXD register. If the descriptor is not available, the pending state will be transmitted and returned and the bit [2] of the ETH_DMASTS register will be set. If the descriptor is available, continue to transmit. |

### 27.11.3 Receive poll demand register (ETH\_DMARXPD)

Offset address: 0x1008

Reset value: 0x0000 0000

| Field | Name | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | RXPD | R/W | <b>Receive Poll Demand</b><br>When these bits are written with any value, DMA will read the current descriptor pointed to by the ETH_DMAHRXD register. If the descriptor is not available (owned by the host), the pending state will be transmitted and returned and the bit [7] of the ETH_DMASTS register will be set. If the descriptor is available, Rx DMA will return to active state. |

### 27.11.4 Receive descriptor list address register (ETH\_DMARXDLADDR)

Offset address: 0x100C

Reset value: 0x0000 0000



| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                  |
|-------|-------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | RXSTA | R/W | <p>Start of Receive List</p> <p>This field contains the base address of the first descriptor in the receive descriptor list. LSB bits [1:0, 2:0, or 3:0] of 32-bit, 64-bit, or 128-bit bus width is ignored and is regarded as all zero by DMA. Therefore, these LSB bits are read-only.</p> |

### 27.11.5 Transmit descriptor list address register (ETH\_DMATXDLADDR)

Offset address: 0x1010

Reset value: 0x0000 0000

| Field | Name  | R/W | Description                                                                                                                                                                                                                                                                                   |
|-------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | TXSTA | R/W | <p>Start of Transmit List</p> <p>This field contains the base address of the first descriptor in the receive descriptor list. LSB bits [1:0, 2:0, or 3:0] of 32-bit, 64-bit, or 128-bit bus width is ignored and is regarded as all zero by DMA. Therefore, these LSB bits are read-only.</p> |

### 27.11.6 State register (ETH\_DMASTS)

Offset address: 0x1014

Reset value: 0x0000 0000

| Field | Name   | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TXFLG  | RC_W1 | <p>Transmit Flag</p> <p>Frame transmission has been completed and TXDES1[31] bit in the first descriptor is set to 1.</p>                                                                                                                                                                                                                                                                                                  |
| 1     | TXSFLG | RC_W1 | <p>Transmit Stopped Flag</p> <p>This bit is set when the transmission stops.</p>                                                                                                                                                                                                                                                                                                                                           |
| 2     | TXBU   | RC_W1 | <p>Transmit Buffer Unavailable</p> <p>This bit indicates that the host owns the next descriptor in the transmit list and DMA cannot get it. Transmission pauses. Bit [22:20] explains the state conversion of the transmission process. To resume processing of the transmit descriptor, the host should change the ownership of the descriptor by setting TXDES0 [31], and then issue a transmit poll demand command.</p> |
| 3     | TXJTO  | RC_W1 | <p>Transmit Jabber Timeout</p> <p>This bit indicates that the transmit Jabber timer times out, and the transmission process will be terminated and in the stop state. This will cause Jabber timeout and the TXDES0 [14] flag bit to be set.</p>                                                                                                                                                                           |
| 4     | RXOVF  | RC_W1 | <p>Receive Overflow</p> <p>This bit indicates that the receive buffer overflows during frame receiving. If part of the frame is transmitted to the application program, the overflow state will be set in RXDES0 [11].</p>                                                                                                                                                                                                 |
| 5     | TXUNF  | RC_W1 | <p>Transmit Underflow</p> <p>This bit indicates that the transmit buffer underflows during frame transmission. Transmission is suspended and the underflow error TXDES0 [1] is set.</p>                                                                                                                                                                                                                                    |
| 6     | RXFLG  | RC_W1 | <p>Receive Flag</p> <p>Frame receiving is completed, and the specific frame state information is updated in the descriptor. Receive and keep running.</p>                                                                                                                                                                                                                                                                  |

| Field | Name     | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7     | RXBU     | RC_W1 | <p>Receive Buffer Unavailable</p> <p>This bit indicates that the host owns the next descriptor in the receive list and DMA cannot get it. The receiving process is suspended. To resume processing of the receive descriptor, the host should change the ownership of the descriptor and issue a receive poll demand command. If no receive poll demand is issued, the receiving process will be resumed when the next confirmed incoming frame is received. This bit is set only when the current receive descriptor is owned by DMA.</p>                                                                                                                                                                                                                                                                                                      |
| 8     | RXSFLG   | RC_W1 | <p>Receive Stopped Flag</p> <p>This bit will be set to 1 when the receiving process enters the stop state.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 9     | RXWTOFLG | RC_W1 | <p>Receive Watchdog Timeout Flag</p> <p>This bit is will be set to 1 when the length of the received frame is greater than 2048 bytes.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10    | ETXFLG   | RC_W1 | <p>Early Transmit Flag</p> <p>The frame to be transmitted has been completely transmitted to the transmit FIFO.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 12:11 | Reserved |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13    | FBERRFLG | RC_W1 | <p>Fatal Bus Error Flag</p> <p>This bit indicates that a bus error has occurred, as described in bit [25:23]. When this bit is set, the corresponding DMA engine will disable all its bus access.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 14    | ERXFLG   | RC_W1 | <p>Early Receive Flag</p> <p>This bit indicates that DMA fills the first data buffer of the packet. When the software writes 1 to this bit or bit [6] of this register is set, this bit will be cleared.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15    | AINTS    | RC_W1 | <p>Abnormal Interrupt Summary</p> <p>When the corresponding interrupt bit is enabled in ETH_DMAINTEN register, the value of abnormal interrupt summary bit is the logic or operation result of the following bits:</p> <p>ETH_DMASTS[1]: Stop in transmission proces</p> <p>ETH_DMASTS[3]: Transmit Jabber timeout</p> <p>ETH_DMASTS[4]: Receive overflow</p> <p>ETH_DMASTS[5]: Transmit underflow</p> <p>ETH_DMASTS[7]: Receive buffer is unavailable</p> <p>ETH_DMASTS[8]: Stop in receiving proces</p> <p>ETH_DMASTS[9]: Receive watchdog timeout</p> <p>ETH_DMASTS[10]: Early transmit interrupt</p> <p>ETH_DMASTS[13]: Fatal bus error</p> <p>Only the unmasked bit affects the abnormal interrupt summary bit. This is a sticky bit and it must be cleared each time the corresponding bit that causes this bit to be set is cleared.</p> |
| 16    | NINTS    | RC_W1 | <p>Normal Interrupt Summary</p> <p>When the corresponding interrupt bit is enabled in ETH_DMAINTEN register, the value of normal interrupt summary bit is the logic or operation result of the following bits:</p> <p>ETH_DMASTS[0]: Transmit interrupt</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | ETH_DMASTS[2]: Transmit buffer is unavailable<br>ETH_DMASTS[6]: Receive interrupt<br>ETH_DMASTS[14]: Early receive interrupt<br>Only the unmasked bit affects the normal interrupt summary bit.<br>This is a sticky bit and it must be cleared each time the corresponding bit that causes this bit to be set is cleared.                                                                                                                                                                                                                                                                                      |
| 19:17 | RXSTS    | R   | Receive Process State<br>This field indicates the receive DMA FSM state. This field does not generate any interrupt.<br>000: Stop: Issue the reset or stop receiving command<br>001: Run: get the receive and transmit descriptors<br>010: Reserved<br>011: Run: wait for receiving message<br>100: Pending: the receive descriptor is unavailable<br>101: Run: disable the receive descriptor<br>110: Reserved<br>111: Run: in the progress of transmitting the received packet data from receive buffer to host memory                                                                                       |
| 22:20 | TXSTS    | R   | Transmit Process State<br>This field indicates the transmit DMA FSM state. This field does not generate any interrupt.<br>000: Stop: issue the reset or stop transmission command<br>001: Run: get the transmit descriptor<br>010: Run: waiting state<br>011: Run: read data from host memory buffer and queue the transmit buffer (Tx FIFO)<br>100, 101: Reserved<br>110: Suspended: the transmit descriptor is unavailable or the transmit buffer underflows<br>111: Run: disable the transmit descriptor                                                                                                    |
| 25:23 | ERRB     | R   | Error Bits<br>This field indicates the type of error that causes the bus error, such as the error response of the AHB interface. This field is valid only when the bit [13] is set. This field does not generate any interrupt.<br>000: An error occurs in transmission process of Rx DMA write data<br>011: An error occurs in transmission process of Tx DMA read data<br>100: An error occurs in Rx DMA descriptor write access<br>101: An error occurs in Tx DMA descriptor write access<br>110: An error occurs in Rx DMA descriptor read access<br>111: An error occurs in Tx DMA descriptor read access |
| 26    | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 27    | MMCFLG   | R   | MMC Flag<br>This bit reflects an interrupt event in the MMC module of MAC.<br>The software must read the corresponding register in the MAC to obtain the exact cause of the interrupt, and clear the interrupt                                                                                                                                                                                                                                                                                                                                                                                                 |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | source to clear this bit to 0. When this bit is high, an interrupt will be generated after it is enabled.                                                                                                                                                                                                                                               |
| 28    | PMTFLG   | R   | <p>PMT Flag</p> <p>This bit indicates an interrupt event in the PMT module of MAC. The software must read the PMT control and state register in the MAC to obtain the exact cause of the interrupt and clear its source to clear this bit to 0. When this bit is high, an interrupt will be generated after it is enabled.</p>                          |
| 29    | TSTFLG   | R   | <p>Timestamp Trigger Flag</p> <p>This bit indicates an interrupt event in the timestamp generator block of the MAC. The software must read the corresponding register in the MAC to obtain the exact cause of the interrupt, and clear its source to clear the bit to 0. When this bit is high, an interrupt will be generated after it is enabled.</p> |
| 31:30 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                         |

### 27.11.7 Operation mode register (ETH\_DMAOPMOD)

Offset address: 0x1018

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1     | STRX     | R/W | <p>Start or Stop Receive</p> <p>When this bit is set, the receiving process will be in running state. DMA attempts to obtain the descriptor from the receive list and process the incoming frames. Try to obtain the descriptor from the current location in the list, and this location is the address set by the ETH_DMARXDLADDR register, or the location reserved when stopping before the receiving process. If DMA does not own this descriptor, receive will be suspended and ETH_DMASTS[7] will be set. The "Start receiving" command is valid only after receiving stops. If the command is issued before the ETH_DMARXDLADDR register is set, DMA behavior is unpredictable.</p> <p>When this bit is cleared, Rx DMA operation will stop after transmission of the current frame. The location of next descriptor in the receive list will be saved and become the current location after restarting the receiving process. The stop receiving command is valid only when the receiving process is in "running" or "suspended" state.</p> |
| 2     | OSECF    | R/W | <p>Operate on Second Frame</p> <p>When this bit is set, it indicates that DMA is processing the second frame of transmitted data, even before obtaining the state of the first frame.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 4:3   | RXTHCTRL | R/W | <p>Receive Threshold Control</p> <p>These two bits control the threshold level of the receive FIFO. When transmitting to the DMA starts, the frame size of receive FIFO is greater than the threshold. In addition, the complete frame with the length less than the threshold will be transmitted automatically.</p> <p>When the configured "receive FIFO size" is 128 bytes, 11 will not be used. These bits are valid only when the RXSF bit is 0 and will be ignored when the RXSF bit is 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | 00: 64<br>01: 32<br>10: 96<br>11: 128                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 5     | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 6     | FUF      | R/W | Forward Undersized Good Frames<br>When it is set, Rx FIFO will forward small frames, including padding bytes and CRC. When it is reset, Rx FIFO will discard all frames less than 64 bytes unless a frame has been transmitted because the receiving threshold is low, such as RTC=01.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7     | FERRF    | R/W | Forward Error Frames<br>When this bit is reset, Rx FIFO will discard the frames with error state. However, if the start byte pointer of the frame has been transferred to the read controller end (in threshold mode), the frame will not be discarded.<br><br>If the start byte of the frame is not transmitted (output) on the ARI bus, Rx FIFO will discard the error frame.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 12:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 13    | STTX     | R/W | Start or Stop Transmission Command<br>When this bit is set, the transmission will be put in the running state, and DMA will check the transmit list of the current location to obtain the frame to be transmitted. The descriptor tries to obtain from the current location in the list or from the previous location reserved when the transmission stops. If the DMA does not own the current descriptor, the transmission will enter the suspended state and the ETH_DMASTS[2] will be set. This command will take effect only when the transmission stops. If the command is issued before the ETH_DMATXDLADDR register is set, DMA behavior is unpredictable.<br><br>When this bit is reset, the transmission process will stop after transmission of the current frame is completed. The location of next descriptor in the transmit list will be saved and when transmission is restarted, it will become the current location. The stop transmission command is valid only when transmission of the current frame is completed or the transmission is in the "suspended" state. |
| 16:14 | TXTHCTRL | R/W | Transmit Threshold Control<br>These bits control the threshold level of the transmit FIFO. At the beginning of transmission, the frame size in the transmit FIFO is greater than the threshold. In addition, the complete frame with the length less than the threshold will also be transmitted. These bits are used only when the bit [21] is reset.<br><br>000: 64<br>001: 128<br>010: 192<br>011: 256<br>100: 40<br>101: 32<br>110: 24<br>111: 16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:17 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20    | FTXF     | R/W | <p>Flush Transmit FIFO</p> <p>When this bit is set, the transmit FIFO controller logic will be reset to its default value, so all data in Tx FIFO will be lost or refreshed. This bit will be cleared internally when the refresh operation is completed. Before this bit is cleared, it should not be written into the operation mode register.</p>                                           |
| 21    | TXSF     | R/W | <p>Transmit Store and Forward</p> <p>When this bit is set, transmission will start if there is a complete frame in the transmit FIFO. When this bit is set, the TTC value specified in bit [16:14] will be ignored. This bit can be replaced only when transmission stops.</p>                                                                                                                 |
| 23:22 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                |
| 24    | DISFRXF  | R/W | <p>Disable Flushing of Received Frames</p> <p>When this bit is set, Rx DMA will not refresh any frames because the receive descriptor or buffer is not available as it normally does when this bit is reset.</p>                                                                                                                                                                               |
| 25    | RXSF     | R/W | <p>Receive Store and Forward</p> <p>When this bit is set, the frame can be read after a complete frame is written to Rx FIFO, and the RTC bit will be ignored. When this bit is reset, Rx FIFO will run in pass-through mode, limited by the threshold specified by the RTC bit.</p>                                                                                                           |
| 26    | DISDT    | R/W | <p>Disable Dropping of TCP/IP Checksum Error Frames</p> <p>When this bit is set, the MAC will not discard the error frames detected only by the receive checksum offload engine. Such a frame has no error in the Ethernet frame received by the MAC, and only has errors in the encapsulated load. When this bit is reset, if the FERRF bit is reset, all error frames will be discarded.</p> |
| 31:27 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                |

### 27.11.8 Interrupt enable register (ETH\_DMAINTEN)

Offset address: 0x101C

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                                                                                                                                                                 |
|-------|---------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | TXIEN   | R/W | <p>Transmit Interrupt Enable</p> <p>When this bit is set to 1 through bit [16], the transmit interrupt will be enabled. When this bit is reset, the transmit interrupt will be disabled.</p>                                                |
| 1     | TXSEN   | R/W | <p>Transmit Stopped Enable</p> <p>When this bit is set to 1 through bit [15], the transmit stop interrupt will be enabled. When this bit is reset, the transmit stop interrupt will be disabled</p>                                         |
| 2     | TXBUEN  | R/W | <p>Transmit Buffer Unavailable Enable</p> <p>When this bit is set to 1 through bit [16], the transmit buffer unavailable interrupt will be enabled. When this bit is reset, the transmit buffer unavailable interrupt will be disabled.</p> |
| 3     | TXJTOEN | R/W | <p>Transmit Jabber Timeout Enable</p> <p>When this bit is set to 1 through bit [15], the transmit Jabber timeout interrupt will be enabled. When this bit is reset, the transmit Jabber timeout interrupt will be disabled.</p>             |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4     | RXOVFEN  | R/W | Receive Overflow Interrupt Enable<br>When this bit is set to 1 through bit [15], the receive overflow interrupt will be enabled. When this bit is reset, the overflow interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                                   |
| 5     | TXUNFEN  | R/W | Transmit Underflow Interrupt Enable<br>When this bit is set to 1 through bit [15], the transmit underflow interrupt will be enabled. When this bit is reset, the underflow interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                              |
| 6     | RXIEN    | R/W | Receive Interrupt Enable<br>When this bit is set to 1 through bit [16], the receive interrupt will be enabled. When this bit is reset, the receive interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 7     | RXBUEN   | R/W | Receive Buffer Unavailable Enable<br>When this bit is set to 1 through bit [15], the receive buffer unavailable interrupt will be enabled. When this bit is reset, the receive buffer unavailable interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                       |
| 8     | RXSEN    | R/W | Receive Stopped Enable<br>When this bit is set to 1 through bit [15], the receive stop interrupt will be enabled. When this bit is reset, the receive stop interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                                              |
| 9     | RXWTOEN  | R/W | Receive Watchdog Timeout Enable<br>When this bit is set to 1 through bit [15], the receive watchdog timeout interrupt will be enabled. When this bit is reset, the receive watchdog timeout interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                             |
| 10    | ETXIEN   | R/W | Early Transmit Interrupt Enable<br>When this bit is set to 1 through bit [15], the early transmit interrupt will be enabled. When this bit is reset, the early transmit interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                                 |
| 12:11 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 13    | FBERREN  | R/W | Fatal Bus Error Enable<br>When this bit is set to 1 through bit [15], the fatal bus error interrupt will be enabled. When this bit is reset, the fatal bus error interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                                        |
| 14    | ERXIEN   | R/W | Early Receive Interrupt Enable<br>When this bit is set to 1 through bit [16], the early receive interrupt will be enabled. When this bit is reset, the early receive interrupt will be disabled.                                                                                                                                                                                                                                                                                                                                                                                    |
| 15    | AINTSEN  | R/W | Abnormal Interrupt Summary Enable<br>When this bit is set, the abnormal interrupt summary will be enabled. When this bit is reset, the abnormal interrupt summary will be disabled. This bit can enable the following interrupts:<br>ETH_DMASTS[1]: Stop in transmission proces<br>ETH_DMASTS[3]: Transmit Jabber timeout<br>ETH_DMASTS[4]: Receive overflow<br>ETH_DMASTS[5]: Transmit underflow<br>ETH_DMASTS[7]: Receive buffer is unavailable<br>ETH_DMASTS[8]: Stop in receiving proces<br>ETH_DMASTS[9]: Receive watchdog timeout<br>ETH_DMASTS[10]: Early transmit interrupt |

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |          |     | ETH_DMASTS[13]: Fatal bus error                                                                                                                                                                                                                                                                                                                                                                        |
| 16    | NINTSEN  | R/W | Normal Interrupt Summary Enable<br>When this bit is set, the normal interrupt summary will be enabled.<br>When this bit is reset, the normal interrupt summary will be disabled.<br>This bit can enable the following interrupts:<br>ETH_DMASTS[0]: Transmit interrupt<br>ETH_DMASTS[2]: Transmit buffer is unavailable<br>ETH_DMASTS[6]: Receive interrupt<br>ETH_DMASTS[14]: Early receive interrupt |
| 31:17 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                        |

### 27.11.9 Missed frame and buffer overflow counter register (ETH\_DMAMFABOCNT)

Offset address: 0x1020

Reset value: 0x0000 0000

| Field | Name       | R/W  | Description                                                                                                                                                                                                            |
|-------|------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | MISFCNT    | RC_R | Controller Missed Frame Counter<br>It indicates the number of frames lost by the controller because the host receive buffer is not available. This counter will increase each time the DMA discards an incoming frame. |
| 16    | MISFCNTOVF | RC_R | Overflow Bit for Missed Frame Counter                                                                                                                                                                                  |
| 27:17 | AMISFCNT   | RC_R | Application Missed Frame Counter<br>It indicates the number of frames lost by application program.                                                                                                                     |
| 28    | OVFCNTOVF  | RC_R | Overflow Bit for FIFO Overflow Counter                                                                                                                                                                                 |
| 31:29 | Reserved   |      |                                                                                                                                                                                                                        |

### 27.11.10 Receive flag watchdog timer register (ETH\_DMARXFLGWDT)

Offset address: 0x1024

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | RXWDTCNT | R/W | RXFLG Watchdog Timer Count<br>This bit indicates the number of system clock cycles for setting the watchdog timer is multiplied by 256. The watchdog timer is triggered by the value set by the program after Rx DMA completes the transmission of a frame in which the RXFLG state bit is not set, because of the setting in the corresponding descriptor RXDES1[31]. After the watchdog timer times out, set the RXFLG bit to stop the timer. Because RXFLG automatically sets RXDES1[31] of the received frame, the RXFLG bit is set to high level, and the watchdog timer is reset. |
| 31:8  | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

### 27.11.11 Current host transmit descriptor register (ETH\_DMAHTXD)

Offset address: 0x1048

Reset value: 0x0000 0000



| Field | Name      | R/W | Description                                                                          |
|-------|-----------|-----|--------------------------------------------------------------------------------------|
| 31:0  | HTXDADDRP | R   | Host Transmit Descriptor Address Pointer<br>Pointer updated by DMA during operation. |

#### 27.11.12 Current host receive descriptor register (ETH\_DMAHRXD)

Offset address: 0x104C

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                         |
|-------|-----------|-----|-------------------------------------------------------------------------------------|
| 31:0  | HRXDADDRP | R   | Host Receive Descriptor Address Pointer<br>Pointer updated by DMA during operation. |

#### 27.11.13 Current host transmit buffer address register (ETH\_DMAHTXBADDR)

Offset address: 0x1050

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                      |
|-------|-----------|-----|----------------------------------------------------------------------------------|
| 31:0  | HTXBADDRP | R   | Host Transmit Buffer Address Pointer<br>Pointer updated by DMA during operation. |

#### 27.11.14 Current host receive buffer address register (ETH\_DMAHRXBADDR)

Offset address: 0x1054

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                     |
|-------|-----------|-----|---------------------------------------------------------------------------------|
| 31:0  | HRXBADDRP | R   | Host Receive Buffer Address Pointer<br>Pointer updated by DMA during operation. |

## 28 Analog-to-digital Converter (ADC)

### 28.1 Full name and abbreviation description of terms

Table 145 Full Name and Abbreviation Description of ADC Terms

| Full name in English | English abbreviation |
|----------------------|----------------------|
| Analog watchdog      | AWD                  |
| Conversion           | C                    |
| Injected             | INJ                  |
| Regular              | REG                  |
| Start                | S                    |
| Scan                 | SCAN                 |
| Single               | SINGLE               |
| Automatic            | A                    |
| Group                | G                    |
| Discontinuous        | DISC                 |
| Count                | CNT                  |
| Dual                 | DUAL                 |
| Continuous           | C                    |
| Calibration          | CAL                  |
| Reset                | RST                  |
| Alignment            | ALIGN                |
| External             | EXT                  |
| Event                | E                    |
| Trigger              | TRG                  |
| Temperature          | T                    |
| Sensor               | S                    |
| Time                 | TIM                  |
| Sample               | SMP                  |
| Offset               | OF                   |
| High                 | H                    |
| Low                  | L                    |
| Threshold            | T                    |
| Sequence             | SEQ                  |

| Full name in English  | English abbreviation |
|-----------------------|----------------------|
| Length                | LEN                  |
| Regular Channels      | REG                  |
| Injected Channel      | INJ                  |
| Injected Group        | INJG                 |
| Automatic             | A                    |
| Conversion            | C                    |
| Analog Watchdog       | AWD                  |
| Discontinuous Mode    | DISC                 |
| Scan Mode             | SCAN                 |
| Continuous Conversion | CONTC                |
| Single Conversion     | SINGLEC              |
| External              | EXT                  |
| External Trigger      | EXTTRG               |
| Sample Time           | SMPTIM               |
| Sequence              | SEQ                  |
| Number                | NUM                  |

## 28.2 Introduction

The series product has 3 ADC with 12-bit precision. Each ADC has up to 16 external channels and 3 internal channels, and the A/D conversion modes of each channel include single, continuous, scan or discontinuous. ADC conversion results can be left-aligned or right-aligned and stored in 16-bit data register.

## 28.3 Main characteristics

- (1) ADC power supply requirements: From 2.4V to 3.6V during full-speed operation; 1.8V during low-speed operation.
- (2) ADC input range:  $V_{REF-} \leq V_{IN} \leq V_{REF+}$ .
- (3) 12-bit, 10-bit, 8-bit or 6-bit resolutions are configurable.
- (4) ADC conversion time:
  - Formula:  $T_{CONV} = \text{sampling time} + 12 \text{ cycles}$
  - The sampling time is controlled by  $SMPCYCCFGx[2:0]$ , the minimum sample cycle is 3, and when  $ADCCLK = 30\text{MHz}$ , the sample time is 3 cycles:  $T_{CONV} = 3 \text{ cycles} + 12 \text{ cycles} = 15 \text{ cycles} = 0.5\mu\text{s}$ .

- (5) Mode input channel category:
  - External GPIO input channel
  - One internal temperature sensor ( $V_{SENSE}$ ) input channel
  - One internal reference voltage ( $V_{REFINT}$ ) input channel
  - One internal backup voltage ( $V_{BAT}$ ) input channel
- (6) Channel conversion mode:
  - Single channel conversion mode: single conversion mode, continuous conversion mode
  - Input channel classification: regular channel, injected channel
  - One-group channel conversion mode: scan mode, discontinuous mode and injected channel management
  - ADC mode: Independent ADC mode, and dual/triple ADC mode
- (7) Trigger mode:
  - On-chip timer signal trigger
  - External pin
  - Software trigger
- (8) Data register:
  - Regular data register
  - Injected data register
  - General regular data register
- (9) Interrupt:
  - End of conversion interrupt
  - Analog watchdog interrupt
  - Overflow interrupt
- (10) DMA request supporting regular data conversion
- (11) Data alignment:
  - Configurable data alignment of DALIGNCFG bit of data register  
ADC\_CTRL2 is left or right alignment.

## 28.4 Functional description

### 28.4.1 ADC pins

Table 146 ADC Pins

| Name       | Description                                                                                  | Signal type                                |
|------------|----------------------------------------------------------------------------------------------|--------------------------------------------|
| $V_{REF+}$ | High-end/Positive electrode reference voltage used by ADC, $1.8V \leq V_{REF+} \leq V_{DDA}$ | Input, analog reference positive electrode |

| Name              | Description                                                                                                                                                                                                               | Signal type                                |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|
| V <sub>DDA</sub>  | Equivalent to analog power supply of V <sub>DD</sub> and:<br>2.4V ≤ V <sub>DDA</sub> ≤ V <sub>DD</sub> (3.6V) during full-speed operation,<br>1.8V ≤ V <sub>DDA</sub> ≤ V <sub>DD</sub> (3.6V) during low-speed operation | Input, analog power supply                 |
| V <sub>REF-</sub> | Low-end/Negative reference voltage used by ADC, V <sub>REF-</sub> = V <sub>SSA</sub>                                                                                                                                      | Input, analog reference negative electrode |
| V <sub>SSA</sub>  | Equivalent to analog power supply of V <sub>SS</sub>                                                                                                                                                                      | Input, analog power ground                 |
| ADCx_IN[15:0]     | 16 analog input channels                                                                                                                                                                                                  | Analog input signal                        |

## 28.4.2 ADC conversion mode

The product has multiple built-in ADC and channels (refer to the data manual for the specific number), which can be combined into a variety of conversion modes.

Multiple built-in ADCs, according to the number of ADCs, the conversion mode can be classified into independent ADC mode and dual ADC mode. Multiple built-in channels, which can be classified into two groups, that is, regular channel and injected channel. The internal conversion mode of each group can be divided into scan mode and discontinuous mode. For the internal channels of each group, the conversion mode is divided into single conversion mode and continuous conversion mode.

In the application, according to the actual application requirements, the number of ADC, the number of conversion channels and the conversion mode of each channel, the ADC conversion mode meeting the requirements can be designed.

### 28.4.2.1 Conversion mode of single ADC and single channel

#### Single conversion mode

In this mode, for single channel, only one conversion is performed for this channel. For multiple channels, only one conversion is performed for this group of channels.

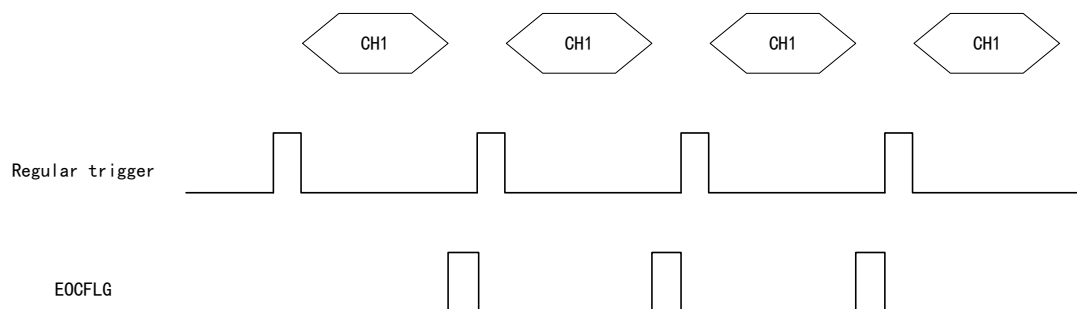
Starting method:

- Set SWSTART to 1 in the ADC\_CTRL2 register (for regular channels only)
- Place JSWSTART at position 1 (for injection channels)
- External trigger (for regular channels or injection channels)

After one conversion of regular channel is over, the converted data will be stored in 16-bit ADC\_REGDATA register, and EOCFLG bit will be set to 1. If configuration EOCIEN bit is set to 1, an interrupt will be generated.

After one conversion of injected channel is over, the converted data will be stored in 16-bit ADC\_INJDATA x (x=1...4) register, and INJEOCFLG bit will be set to 1. If configuration INJEOCIEN bit is set to 1, an interrupt will be generated.

Figure 114 Single Conversion Mode Timing Diagram



### Continuous conversion mode

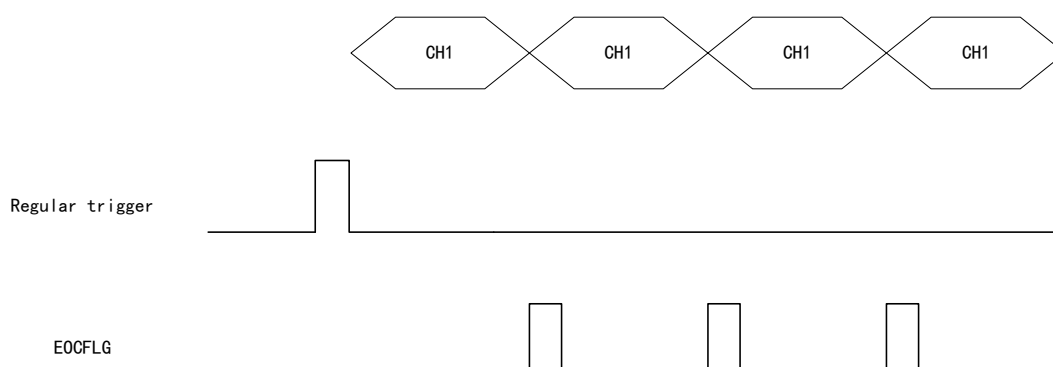
In this mode, for single channel, continuous conversion is conducted for this channel.

This mode is started by the ADCEN bit of configuration register ADC\_CTRL2 or is started by external trigger.

After the conversion of one regular channel is over, the converted data will be stored in 16-bit ADC\_REGDATA register, and EOCFLG bit will be set to 1. If configuration EOCIEN bit is set to 1, an interrupt will be generated.

After the conversion of one injected channel is over, the converted data will be stored in 16-bit ADC\_INJDATA x(x=1...4) register, and INJEOCFLG bit will be set to 1. If configuration INJEOCIEN bit is set to 1, an interrupt will be generated.

Figure 115 Continuous Conversion Mode Timing Diagram



## 28.4.2.2 Conversion mode of single ADC and one group of channels

### Classification of analog input channels

#### Regular channel group

- The regular group consists of 16 channels
- Regular channel conversion sequence is determined by the register ADC\_REGSEQx
- The total number of conversion channels of regular group is determined by REGSEQLEN bit of configuration register ADC\_REGSEQ1

#### Injected channel group

- The injected group consists of 4 channels
- Injected channel conversion sequence is determined by the register ADC\_INJSEQ
- The total number of conversion channels of injected group is determined by INJSEQLEN bit of configuration register ADC\_INJSEQ

#### Internal input channel

Temperature sensor:

- The temperature sensor is used to measure the internal temperature of the chip
- The temperature sensor selects ADC1\_IN16 input channel
- Start through TSVREFEN bit of the configuration register ADC\_CCTRL

Internal reference voltage  $V_{REFINT}$ :

- The internal reference voltage is used to provide a stable voltage output for ADC
- Internal reference voltage  $V_{REFINT}$  is used to select ADC1\_IN17 input channel

Internal backup voltage  $V_{BAT}$ :

- Internal backup voltage  $V_{BAT}$  is used to select ADC1\_IN18 input channel

### Channel conversion sequence

#### Configuration of regular sequence registers:

- Configure REGSEQC1~REGSEQC6 bits of the register ADC\_REGSEQ3 to set No. 1~6 conversion channels
- Configure REGSEQC7~REGSEQC12 bits of the register ADC\_REGSEQ2 to set No. 7~12 conversion channels
- Configure REGSEQC13~REGSEQC16 bits of the register ADC\_REGSEQ1 to set No. 13~16 conversion channels

- Configure REGSEQLEN of the register ADC\_REGSEQ1 to set the number of channels for conversion

#### Configuration of injected sequence register:

- Configure INJSEQC1~INJSEQC4 bit of the register ADC\_INJSEQ to set No. 1~4 conversion channels
- Configure INJSEQLEN of the register ADC\_INJSEQ to set the number of channels for conversion
- If the value of INJSEQLEN is less than 4, the conversion sequence will be different and start from (4-INJSEQLEN).

### Channel conversion mode

#### Scan Mode

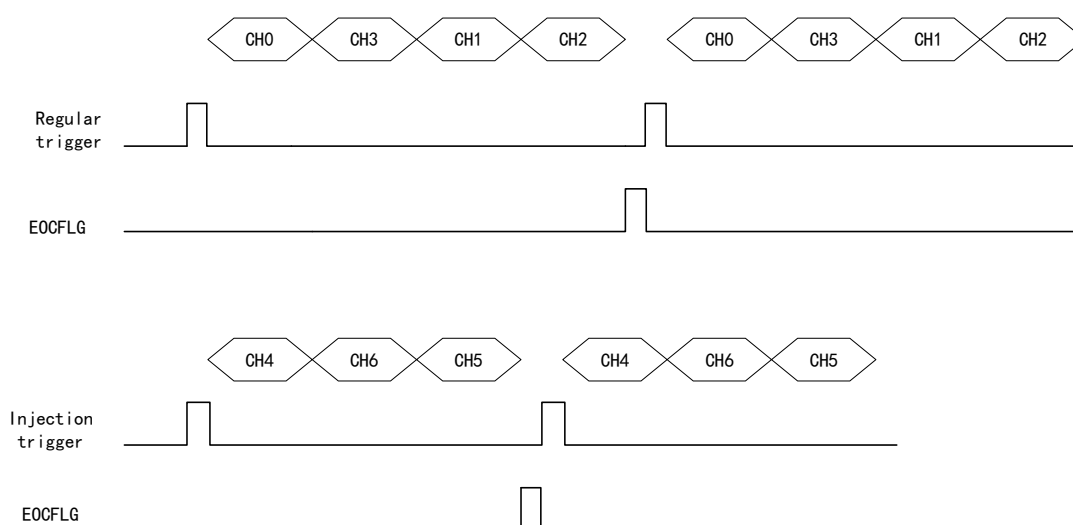
This mode is applicable to one group of channels, which is equivalent to a single conversion on each channel of one group of channels.

This mode is started by SCANEN bit of configuration register ADC\_CTRL1, and after startup, ADC scans all channels which are arranged according to the sequence register ADC\_REGSEQ or the ADC\_INJSEQ, and after each channel conversion is completed, it will be automatically converted to the next channel of the group.

If the configuration CONTCEN bit is set to 1, the conversion will continue from the first channel of the group when the last channel of the group completes conversion.

If the configuration DMAEN bit is set to 1, the DMA controller will transmit the converted data of regular channel to SRAM every time the channel conversion is completed.

Figure 116 Scan Mode Timing Diagram





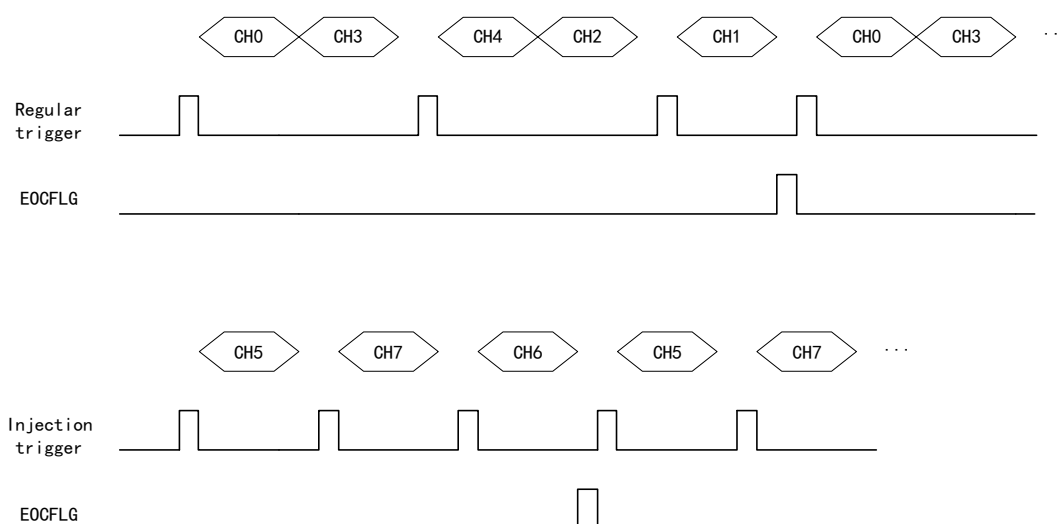
## Discontinuous mode

This mode is suitable for a group of channels, which is equivalent to continuous conversion of multiple channels in a group of channels.

For regular groups, this mode is started by REGDISCEN bit of configuration register ADC\_CTRL1. After startup, conduct short sequence conversion of n channels ( $n \leq 8$ ), and n is determined by DISCNUMCFG[2:0] of configuration register ADC\_CTRL1; next round of conversion of n channels can be started through software control or external trigger source and when the conversion of all channels of this group is completed, EOCFLG bit will be set to 1.

For injected groups, this mode is enabled by INJDISCEN bit of configuration register ADC\_CTRL1; after startup, one channel will be converted according to the configuration sequence of the sequence register; conversion of next channels can be started by software control or external trigger source and when the conversion of all channels of this group is completed, EOCFLG bit and INJEOCFLG bit will be set to 1.

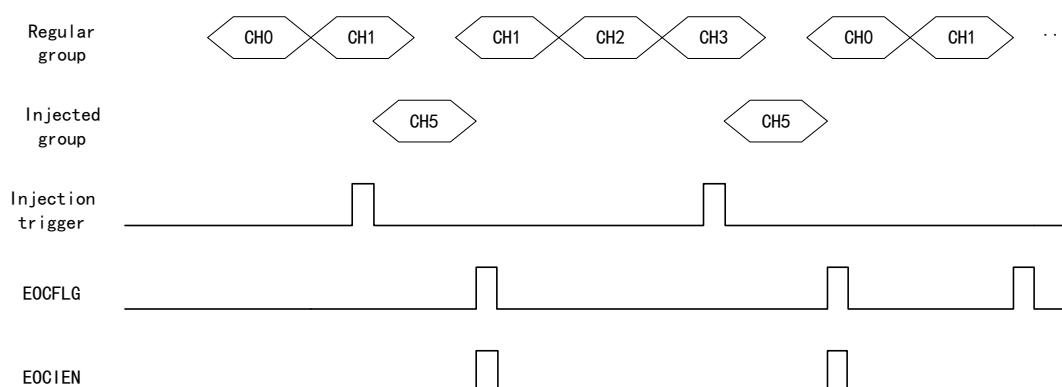
Figure 117 Discontinuous Mode Timing Diagram



## Injected channel management

Trigger injection: By clearing INJGACEN bit of the register ADC\_CTRL1 If a software trigger or external trigger is generated during the conversion of regular group channels, the injected conversion will be triggered. At this time, the regular channel conversion will stop, the injected channel sequence will start conversion, and after the injected group channel conversion is completed, the regular group channel conversion will be recovered.

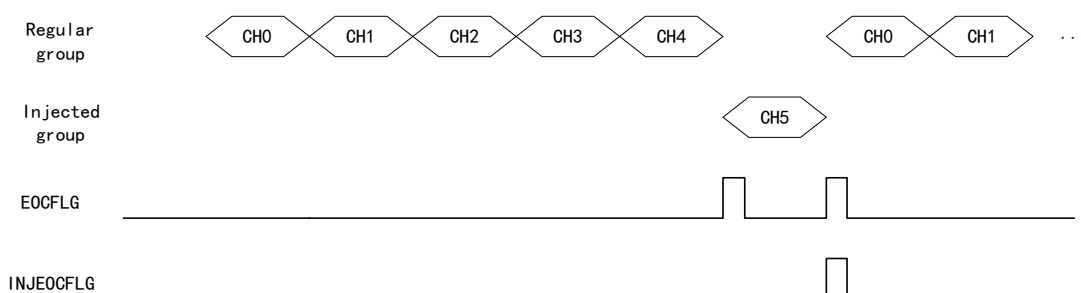
Figure 118 Trigger Injection Timing Diagram



Automatic injection: Start by INJGACEN bit of configuration register ADC\_CTRL1; after conversion of the regular group channels is completed, the injected group channels will start conversion automatically; in the automatic injection mode, external trigger of the injected group channels must be disabled.

If the CONTCEN bit of the register ADC\_CTRL2 is also configured, all channels of regular group and injection group will convert continuously.

Figure 119 Automatic Injection Timing Diagram



### 28.4.2.3 Dual or triple ADC mode and conversion mode of one group of channels

For products with two or more ADC modules, dual or triple ADC mode is used. ADC1 is the master ADC by default, while others are the slave ADC by default, and the ADC mode is set by configuring ADCMSEL bit in ADC1\_CCTRL register.

When the configuration is triggered by external event, it is required to set it to trigger only the master ADC, and then configure the slave ADC to be triggered by software.

**There are six possible dual or triple ADC modes:**

#### (1) Simultaneous regular mode

The simultaneous regular mode means multiple ADC convert a regular channel group at the same time. Two ADC cannot convert one channel at the same time. The external trigger event is determined by REGEXTTRGSEL of the register

ADC1\_CTRL2.

EOCFLG interrupt will be generated after all ADC regular channels are converted. Dual ADC mode: After conversion is over, a DMA transmission request will be generated, and the ADC1 converted data are stored in low 16 bits of the register ADC1\_REGDATA, while the ADC2 converted data are stored in high 16 bits of the register ADC\_REGDATA. Triple ADC mode: After conversion is over, three DMA requests will be generated to transmit ADC1, ADC2 and ADC3 converted data to the memory.

#### (2) **Simultaneous injection mode**

The simultaneous injection mode means multiple ADC convert an injected channel group at the same time. Two ADC cannot convert one channel at the same time. The external trigger event is determined by INJEXTTRGSEL of the register ADC1\_CTRL2.

After ADC conversion is over, the converted data will be stored in the register ADC\_INJDATAx of each ADC interface.

INJEOCFLG interrupt will be generated after all ADC injected channels are converted.

#### (3) **Alternate mode**

The alternate mode means multiple ADC convert a regular channel group alternately. The external trigger event is determined by REGEXTTRGSEL of the register ADC1\_CTRL2.

Dual ADC mode: After triggering, ADC1 starts first, ADC2 starts after delay, and the delay is configured through SMPDEL2 bit of the register ADC\_CCTRL. After the conversion is completed, an EOCFLG interrupt will be generated, and then a DMA request will be generated, and the data will be transmitted in DMA mode 2. Triple ADC mode: After triggering, ADC1 starts first, ADC2 starts after delay, ADC3 starts after delay of ADC2 conversion, and the delay is configured through SMPDEL2 bit of register ADC\_CCTRL. Every two conversions are made, a DMA request will be generated and the data will be transmitted in DMA mode 2.

#### (4) **Alternate trigger mode**

The alternate trigger mode means multiple ADC trigger and convert an injected channel group alternately. The external trigger event is determined by INJEXTTRGSEL of the register ADC1\_CTRL2.

Dual ADC mode: When the first trigger is generated, convert all channels of injection group in ADC1, and when the second trigger is generated, convert all channels of injection group in ADC2, and after each ADC completes conversion, generate an INJEOCFLG interruption. Triple ADC mode: When the first trigger is generated, convert all channels of injection group in ADC1, and when the

second trigger is generated, convert all channels of injection group in ADC2, and when the third trigger is generated, convert all channels of injection group in ADC3, and after each ADC completes conversion, generate an INJEOCFG interrupt.

#### (5) Mixed simultaneous regular/injection mode

The mixed simultaneous regular/injection mode means after the simultaneous regular mode is interrupted, the simultaneous injection mode will be enabled.

In this mode, a sequence of the same length must be converted or a trigger interval time must be set to complete the conversion of a longer sequence.

#### (6) Mixed simultaneous regular + alternate trigger mode

The mixed simultaneous regular + alternate trigger mode means after the simultaneous regular mode is interrupted, the alternate trigger mode will be enabled.

In this mode, a sequence of the same length must be converted or a trigger interval time must be set to complete the conversion of a longer sequence.

### 28.4.3 External trigger

Register configuration of external trigger is as follows:

- The external event trigger of regular group channel is enabled by REGEXTTRGSEL bit of configuration register ADC\_CTRL2
- The external event trigger of injected group channel is started by INJGEXTTRGSEL bit of configuration register ADC\_CTRL2.

Table 147 External Trigger of Regular Channel

| Trigger source | REGEXTTRGSEL[3:0] | Trigger type                       |
|----------------|-------------------|------------------------------------|
| TMR1_CC1       | 0000              | Internal signal from on-chip timer |
| TMR1_CC2       | 0001              |                                    |
| TMR1_CC3       | 0010              |                                    |
| TMR2_CC2       | 0011              |                                    |
| TMR2_CC3       | 0100              |                                    |
| TMR2_CC4       | 0101              |                                    |
| TMR2_TRGO      | 0110              |                                    |
| TMR3_CC1       | 0111              |                                    |
| TMR3_TRGO      | 1000              |                                    |
| TMR4_CC4       | 1001              |                                    |
| TMR5_CC1       | 1010              |                                    |
| TMR5_CC2       | 1011              |                                    |

| Trigger source | REGEXTTRGSEL[3:0] | Trigger type |
|----------------|-------------------|--------------|
| TMR5_CC3       | 1100              |              |
| TMR8_CC1       | 1101              |              |
| TMR8_TRGO      | 1110              |              |
| EINT Line 11   | 1111              | External pin |

Table 148 External Trigger of Injected Channel

| Trigger source | INJGEXTTRGSEL[3:0] | Trigger type                       |
|----------------|--------------------|------------------------------------|
| TMR1_CC4       | 0000               | Internal signal from on-chip timer |
| TMR1_TRGO      | 0001               |                                    |
| TMR2_CC1       | 0010               |                                    |
| TMR2_TRGO      | 0011               |                                    |
| TMR3_CC2       | 0100               |                                    |
| TMR3_CC4       | 0101               |                                    |
| TMR4_CC1       | 0110               |                                    |
| TMR4_CC2       | 0111               |                                    |
| TMR4_CC3       | 1000               |                                    |
| TMR4_TRGO      | 1001               |                                    |
| TMR5_CC4       | 1010               |                                    |
| TMR5_TRGO      | 1011               |                                    |
| TMR8_CC2       | 1100               |                                    |
| TMR8_CC3       | 1101               |                                    |
| TMR8_CC4       | 1110               |                                    |
| EINT Line 15   | 1111               | External pin                       |

## 28.4.4 Data register

### 28.4.4.1 Regular data register

ADC\_REGDATA is a 32-bit ADC regular data register. In single-ADC mode, only the lower 16 bits are used to store the converted data. The data are left aligned or right aligned.

It is determined by DALIGNCFG bit of configuration register ADC\_CTRL2 whether to use DMA transmission. There are at most 16 regular channels, but only one regular data register. Therefore, data coverage will occur in multi-channel conversion, and DMA transmission is needed at this time.

### 28.4.4.2 Injection data memory

ADC\_INJDATA<sub>x</sub> (x=1,2,3,4) is ADC injected data register, and there are four 32-

bit registers, of which the low 16 bits are effective and the high 16 bits are reserved. There are at most four injected channels and four injection data registers, so data coverage will not occur in multi-channel conversion. The data are left aligned or right aligned.

#### 28.4.4.3 General regular data memory

ADC\_CDATA is a general regular data register of ADC, and is only applicable to dual or triple mode. DMA is generally required to cooperate with data transmission in dual or triple mode.

### 28.4.5 Interrupt

#### 28.4.5.1 End of conversion interrupt

##### Interrupt of end of conversion of regular group channels

An interrupt will be generated by the end of conversion of regular channels. Read the value of the regular data register in the interrupt function.

Interrupt is enabled by the EOCIEN bit of the control register ADC\_CTRL1.

The EOCFLG bit of the status register ADC\_CSTS is used to query the event criteria.

##### Interrupt of end of conversion of injected group channels

An interrupt will be generated after the conversion of injected channels is completed. Read the value of the regular data register in the interrupt function.

Interrupt is enabled by the INJEOCIEN bit of the control register ADC\_CTRL1

The INJEOCFLG bit of the status register ADC\_CSTS is used to query the event criteria.

#### 28.4.5.2 Analog watchdog interrupt

If the input analog voltage is not within the threshold range, an analog watchdog interrupt will be generated.

Interrupt is enabled by the AWDIEN bit of the control register ADC\_CTRL1.

The AWDFLG bit of the status register ADC\_CSTS is used to query the event criteria.

#### 28.4.5.3 Overflow interrupt

When the conversion data is lost (overflow), an overflow interrupt will be generated.

Interrupt is enabled by the OVRIEN bit of the control register ADC\_CTRL1.

The OVRFLG bit of the status register ADC\_CSTS is used to query the event

criteria.

#### 28.4.6 DMA

DMA request will be generated after the conversion of regular channels is completed; the converted data result can be transmitted to the memory from the ADC\_REGDATA register.

#### 28.4.7 On-chip Hardware Oversampling

The on-chip hardware oversampling unit performs data preprocessing to alleviate the CPU load. It can handle multiple conversions and average the results of these conversions to produce a 16-bit wide data output. The resulting value is calculated using the following formula, where the values of N and M can be adjusted. The oversampling unit can be enabled by setting the OSEN bit in the ADC\_OSAMPCTRL register, which reduces data output rate in exchange for higher resolution.  $D_{out}(n)$  refers to the nth digital signal output from the ADC:

$$Result = \frac{1}{M} \times \sum_{n=0}^{N-1} (D_{out}(n))$$

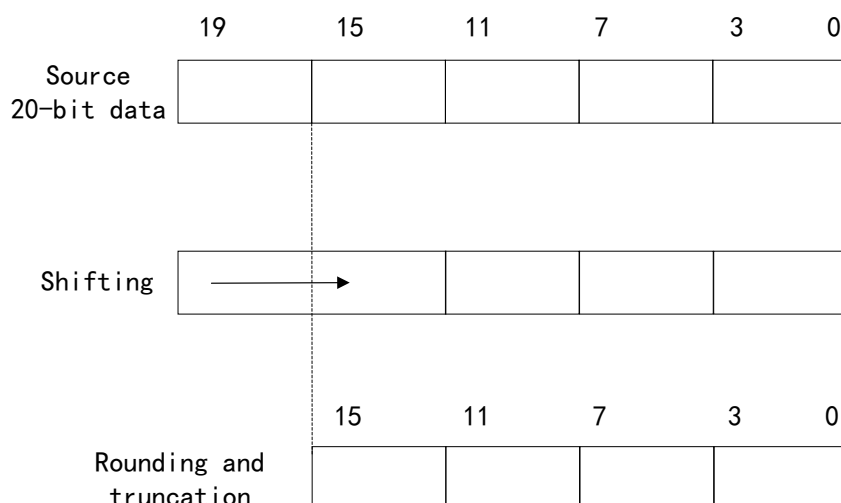
The on-chip hardware oversampling unit performs two functions: sum and the bit right shifting.

The oversampling rate N is defined by the OSR[2:0] bits in the ADC\_OSAMPCTL register, with a range from 2x to 256x. The division coefficient M is defined as a right shift of up to 8 bits, configured through the OSS[3:0] bits in the ADC\_OSAMPCTRL register.

The sum unit can generate a value of up to 20 bits (256 \* 12 bits). First, this value is right-shifted; the remaining part after shifting is rounded to produce an approximate value. Finally, the high bits are truncated, keeping only the lowest 16 bits as the final value, which is then written to the corresponding data register.

#### Result truncation from 20 bits to 16 bits

Figure 120 Result Truncation from 20 bits to 16 bits



Note:

- (1) If the intermediate result after shifting still exceeds 16 bits, the higher bits will be directly truncated.
- (2) The oversampling function is not applicable to ADC injection data mode.

## 28.5 Register address mapping

Table 149 ADC Register Address Mapping

| Register name | Description                                 | Offset address |
|---------------|---------------------------------------------|----------------|
| ADC_STS       | ADC state register                          | 0x00           |
| ADC_CTRL1     | ADC control register 1                      | 0x04           |
| ADC_CTRL2     | ADC control register 2                      | 0x08           |
| ADC_SMPTIM1   | ADC sampling time register 1                | 0x0C           |
| ADC_SMPTIM2   | ADC sampling time register 2                | 0x10           |
| ADC_INJDOFx   | ADC injected channel data offset register x | 0x14-0x20      |
| ADC_AWDHT     | Analog watchdog high-threshold register     | 0x24           |
| ADC_AWDLT     | Analog watchdog low-threshold register      | 0x28           |
| ADC_REGSEQ1   | ADC regular sequence register 1             | 0x2C           |
| ADC_REGSEQ2   | ADC regular sequence register 2             | 0x30           |
| ADC_REGSEQ3   | ADC regular sequence register 3             | 0x34           |
| ADC_INJSEQ    | ADC injected sequence register              | 0x38           |
| ADC_INJDATAx  | ADC injected data register X                | 0x3C-0x48      |
| ADC_REGDATA   | ADC regular data register                   | 0x4C           |



| Register name | Description                                                    | Offset address |
|---------------|----------------------------------------------------------------|----------------|
| ADC_OSAMPCTRL | ADC oversampling control register                              | 0x50           |
| ADC_CSTS      | ADC general-purpose state register                             | 0x00           |
| ADC_CCTRL     | ADC general-purpose control register                           | 0x04           |
| ADC_CDATA     | Applicable to dual and triple mode general rule data registers | 0x08           |

## 28.6 Register functional description

### 28.6.1 ADC state register (ADC\_STS)

Offset address: 0x00

Reset value: 0x0000 0000

| Field | Name      | R/W   | Description                                                                                                                                                                    |
|-------|-----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | AWDFLG    | RC_W0 | Analog Watchdog Occur Flag<br>This bit is set to 1 by hardware and cleared by software, indicating whether an analog watchdog event occurs.<br>0: No occurrence<br>1: Occurred |
| 1     | EOCFLG    | RC_W0 | Regular Channel End of Conversion Flag<br>0: Not completed<br>1: Completed                                                                                                     |
| 2     | INJEOCFLG | RC_W0 | Injected Channel End of Conversion Flag<br>0: Not completed<br>1: Completed                                                                                                    |
| 3     | INJCSFLG  | RC_W0 | Injected Channel Conversion Start Flag<br>0: Not start<br>1: Start                                                                                                             |
| 4     | REGCSFLG  | RC_W0 | Regular Channel Conversion Start Flag<br>0: Not start<br>1: Start                                                                                                              |
| 5     | OVRFLG    | RC_W0 | Overrun Flag<br>0: Not occur<br>1: Occurred                                                                                                                                    |
| 31:6  | Reserved  |       |                                                                                                                                                                                |

### 28.6.2 ADC control register 1 (ADC\_CTRL1)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                        |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | AWDCHSEL  | R/W | Analog Watchdog Channel Select<br>00000: ADC analog input channel 0<br>00001: ADC analog input channel 1<br>.....<br>01111: ADC analog input channel 15<br>10000: ADC analog input channel 16<br>10001: ADC analog input channel 17<br>10010: ADC analog input channel 18<br>Other value: Reserved |
| 5     | EOCIEN    | R/W | EOC Interrupt Enable<br>Used to enable the generation of interrupt after the conversion is completed.<br>0: Disable<br>1: Enable                                                                                                                                                                   |
| 6     | AWDIEN    | R/W | Analog Watchdog Interrupt Enable<br>If the bit is set and in scan mode, when the watchdog detects that the value exceeds the threshold, an interrupt will be generated and the scan will be aborted.<br>0: Disable<br>1: Enable                                                                    |
| 7     | INJEOCIEN | R/W | Interrupt Enable for Injected Channels End Of Conversion Flag<br>0: Disable<br>1: Enable                                                                                                                                                                                                           |
| 8     | SCANEN    | R/W | Scan Mode Enable<br>In the scan mode, convert the channel selected by ADC_REGSEQX or ADC_INJSEQX register.<br>0: Disable<br>1: Enable<br>Note: If EOCIEN or INJEOCIEN bit is set respectively, EOC or INJEOC interrupt will be generated only after the last channel is converted.                 |
| 9     | AWDSGLEN  | R/W | Enable The Watchdog on A Single Channel In Scan Mode<br>This channel is specified by AWDCHSEL[4:0] bit.<br>0: Enable on all channels<br>1: Enable on a single channel;                                                                                                                             |
| 10    | INJGACEN  | R/W | Automatic Injected Group Conversion Enable<br>Used to enable automatic conversion of injected channels after the conversion of regular channel group is completed.<br>0: Disable<br>1: Enable                                                                                                      |
| 11    | REGDISCEN | R/W | Discontinuous Mode on Regular Channels Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                           |
| 12    | INJDISCEN | R/W | Discontinuous Mode on Injected Channels Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                          |

| Field | Name       | R/W | Description                                                                                                          |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------|
| 15:13 | DISCNUMCFG | R/W | Discontinuous Mode Channel Number Configure<br>000: One channel<br>001: Two channels<br>.....<br>111: Eight channels |
| 21:16 | Reserved   |     |                                                                                                                      |
| 22    | INJAWDEN   | R/W | Enable the Analog Watchdog Function on the Injected Channels<br>0: Disable<br>1: Enable                              |
| 23    | REGAWDEN   | R/W | Enable the Analog Watchdog Function on the Regular Channels<br>0: Disable<br>1: Enable                               |
| 25:24 | RESSEL     | R/W | Resolution Selection<br>00: 12 bits<br>01: 10 bits<br>10: 8 bits<br>11: 6 bits                                       |
| 26    | OVRIEN     | R/W | Overrun Interrupt Enable<br>0: Disable<br>1: Enable                                                                  |
| 31:27 | Reserved   |     |                                                                                                                      |

### 28.6.3 ADC control register 2 (ADC\_CTRL2)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                   |
|-------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ADCEN     | R/W | ADC Enable<br>0: Disable ADC conversion and enter the power-down mode<br>1: Enable ADC and start conversion                                                                   |
| 1     | CONTGEN   | R/W | Continuous Conversion Mode Enable<br>0: Single conversion mode<br>1: Continuous conversion mode                                                                               |
| 7:2   | Reserved  |     |                                                                                                                                                                               |
| 8     | DMAEN     | R/W | DMA Mode Enable<br>0: Disable<br>1: Enable                                                                                                                                    |
| 9     | DMADISSEL | R/W | DMA disable selection<br>0: No new DMA request will be issued after the last transmission<br>1: DMA request will be issued whenever data conversion occurs and DMA is enabled |
| 10    | EOCSEL    | R/W | End of conversion selection<br>0: EOCFLG bit will be set to 1 at the end of each regular conversion sequence                                                                  |

| Field | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |              |     | 1: EOCFLG bit will be set to 1 at the end of each regular conversion                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11    | DALIGNCFG    | R/W | Data Alignment Mode Configure<br>0: Right alignment<br>1: Left alignment                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:12 | Reserved     |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 19:16 | INJEXTTRGSEL | R/W | Select the External Trigger Event to Start the Injected Group Conversion<br>0000: CC4 event of timer 1<br>0001: TRGO event of timer 1<br>0010: CC1 event of timer 2<br>0011: TRGO event of timer 2<br>0100: CC2 event of timer 3<br>0101: CC4 event of timer 3<br>0110: CC1 event of timer 4<br>0111: CC2 event of timer 4<br>1000: CC3 event of timer 4<br>1001: TRGO event of timer 4<br>1010: CC4 event of timer 5<br>1011: TRGO event of timer 5<br>1100: CC2 event of timer 8<br>1101: CC3 event of timer 8<br>1110: CC4 event of timer 8<br>1111: EINT Line 15 |
| 21:20 | INJEXTTRGEN  | R/W | Enable the External Trigger for Injected Channels<br>00: Trigger detection is disabled<br>01: Trigger detection on rising edge<br>10: Trigger detection on falling edge<br>11: Trigger detection on rising edge and falling edge                                                                                                                                                                                                                                                                                                                                     |
| 22    | INJSWSC      | R/W | Start Conversion of Injected Channels<br>0: Reset state<br>1: Start conversion of injected channels                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23    | Reserved     |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 27:24 | REGEXTTRGSEL | R/W | Select the External Trigger Event to Start the Regular Group Conversion<br>0000: CC1 event of timer 1<br>0001: CC2 event of timer 1<br>0010: CC3 event of timer 1<br>0011: CC2 event of timer 2<br>0100: CC3 event of timer 2<br>0101: CC4 event of timer 2<br>0110: TRGO event of timer 2<br>0111: CC1 event of timer 3<br>1000: TRGO event of timer 3<br>1001: CC4 event of timer 4<br>1010: CC1 event of timer 5<br>1011: CC2 event of timer 5<br>1100: CC3 event of timer 5<br>1101: CC1 event of timer 8<br>1110: TRGO event of timer 8<br>1111: EINT Line 11   |

| Field | Name       | R/W | Description                                                                                                                                                                                                                     |
|-------|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:28 | REEXTTRGEN | R/W | Enable the External Trigger for Regular Channels<br>00: Trigger detection is disabled<br>01: Trigger detection on rising edge<br>10: Trigger detection on falling edge<br>11: Trigger detection on rising edge and falling edge |
| 30    | REGSWSC    | R/W | Start Conversion of Regular Channels<br>0: Reset state<br>1: Start conversion of regular channels                                                                                                                               |
| 31    | Reserved   |     |                                                                                                                                                                                                                                 |

#### 28.6.4 ADC sampling time register 1 (ADC\_SMPTIM1)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field | Name            | R/W | Description                                                                                                                                                                         |
|-------|-----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:0  | SMPCYCCFGx[2:0] | R/W | Channel x Sample Cycles Configure<br>000: 3 cycles<br>001: 15 cycles<br>010: 28 cycles<br>011: 56 cycles<br>100: 84 cycles<br>101: 112 cycles<br>110: 144 cycles<br>111: 480 cycles |
| 31:27 | Reserved        |     |                                                                                                                                                                                     |

#### 28.6.5 ADC sampling time register 2 (ADC\_SMPTIM2)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name            | R/W | Description                                                                                                                                                                         |
|-------|-----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:0  | SMPCYCCFGx[2:0] | R/W | Channel x Sample Cycles Configure<br>000: 3 cycles<br>001: 15 cycles<br>010: 28 cycles<br>011: 56 cycles<br>100: 84 cycles<br>101: 112 cycles<br>110: 144 cycles<br>111: 480 cycles |
| 31:30 | Reserved        |     |                                                                                                                                                                                     |

#### 28.6.6 ADC injected channel data offset register x (ADC\_INJDOFx) (x=1...4)

Offset address: 0x14-0x20

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                             |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:0  | INJDOFx  | R/W | Data Offset for Injected Channel x<br>When converting the injected channels, these bits define the values to be subtracted from the original converted data, and the result of the conversion can be read in the ADC_INJDATAx register. |
| 31:12 | Reserved |     |                                                                                                                                                                                                                                         |

### 28.6.7 Analog watchdog high-threshold register (ADC\_AWDHT)

Offset address: 0x24

Reset value: 0x0000 0FFF

| Field | Name        | R/W | Description                    |
|-------|-------------|-----|--------------------------------|
| 11:0  | AWDHT[11:0] | R/W | Analog Watchdog High Threshold |
| 31:12 | Reserved    |     |                                |

### 28.6.8 Analog watchdog low-threshold register (ADC\_AWDLT)

Offset address: 0x28

Reset value: 0x0000 0000

| Field | Name        | R/W | Description                   |
|-------|-------------|-----|-------------------------------|
| 11:10 | AWDLT[11:0] | R/W | Analog Watchdog Low Threshold |
| 31:12 | Reserved    |     |                               |

### 28.6.9 ADC regular sequence register 1 (ADC\_REGSEQ1)

Offset address: 0x2C

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                                                                               |
|-------|-----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | REGSEQC13 | R/W | 13 <sup>th</sup> Conversion in Regular Sequence<br>Define the channel number of No. 13 conversion in regular sequence (0~17)                                                                                              |
| 9:5   | REGSEQC14 | R/W | 14 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13.                                                                                                                                 |
| 14:10 | REGSEQC15 | R/W | 15 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13.                                                                                                                                 |
| 19:15 | REGSEQC16 | R/W | 16 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13.                                                                                                                                 |
| 23:20 | REGSEQLEN | R/W | Regular Channel Sequence Length<br>These bits are defined by software as the number of channels in regular channel conversion sequence.<br>0000: One conversion<br>0001: Two conversions<br>.....<br>1111: 16 conversions |
| 31:24 | Reserved  |     |                                                                                                                                                                                                                           |

### 28.6.10 ADC regular sequence register 2 (ADC\_REGSEQ2)

Offset address: 0x30

Reset value: 0x0000 000

| Field | Name      | R/W | Description                                                                               |
|-------|-----------|-----|-------------------------------------------------------------------------------------------|
| 4:0   | REGSEQC7  | R/W | 7 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13.  |
| 9:5   | REGSEQC8  | R/W | 8 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13.  |
| 14:10 | REGSEQC9  | R/W | 9 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13.  |
| 19:15 | REGSEQC10 | R/W | 10 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 24:20 | REGSEQC11 | R/W | 11 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 29:25 | REGSEQC12 | R/W | 12 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 31:30 | Reserved  |     |                                                                                           |

### 28.6.11 ADC regular sequence register 3 (ADC\_REGSEQ3)

Offset address: 0x34

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                              |
|-------|----------|-----|------------------------------------------------------------------------------------------|
| 4:0   | REGSEQC1 | R/W | 1 <sup>st</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 9:5   | REGSEQC2 | R/W | 2 <sup>nd</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 14:10 | REGSEQC3 | R/W | 3 <sup>rd</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 19:15 | REGSEQC4 | R/W | 4 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 24:20 | REGSEQC5 | R/W | 5 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 29:25 | REGSEQC6 | R/W | 6 <sup>th</sup> Conversion in Regular Sequence<br>Refer to the description of REGSEQC13. |
| 31:30 | Reserved |     |                                                                                          |

### 28.6.12 ADC injected sequence register (ADC\_INJSEQ)

Offset address: 0x38

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                  |
|-------|----------|-----|------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | INJSEQC1 | R/W | 1 <sup>st</sup> Conversion in Injected Sequence<br>Define the channel number of No. 1 conversion in injected sequence (0~17) |

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:5   | INJSEQC2  | R/W | 2 <sup>nd</sup> Conversion in Injected Sequence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 14:10 | INJSEQC3  | R/W | 3 <sup>rd</sup> Conversion in Injected Sequence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 19:15 | INJSEQC4  | R/W | 4 <sup>th</sup> Conversion In Injected Sequence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 21:20 | INJSEQLEN | R/W | <p>Injected Channel Sequence Length</p> <p>These bits are defined by software as the number of channels in injected channel conversion sequence, and the conversion sequence is:</p> <p>INJSEQC(4-INJSEQLEN) → INJSEQ (5-INJSEQLEN) → INJSEQC(6-INJSEQLEN)</p> <p>→ INJSEQC(7-INJSEQLEN); the details are as follows:</p> <p>00: One conversion, only converting INJSEQC4</p> <p>01: Two conversions; the conversion sequence is INJSEQC3→INJSEQC4</p> <p>10: Three conversions; the conversion sequence is INJSEQC2→INJSEQC3→INJSEQC4</p> <p>11: Four conversions; the conversion sequence is INJSEQC1→INJSEQC2→INJSEQC3→INJSEQC4</p> |
| 31:22 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 28.6.13 ADC injected data register x (ADC\_INJDATAx) (x= 1...4)

Offset address: 0x3C–0x48

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                              |
|-------|----------|-----|------------------------------------------------------------------------------------------|
| 15:0  | INJDATA  | R   | <p>Injected Conversion Data</p> <p>Conversion result of injected channel, read-only.</p> |
| 31:16 | Reserved |     |                                                                                          |

### 28.6.14 ADC regular data register (ADC\_REGDATA)

Offset address: 0x4C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                            |
|-------|----------|-----|----------------------------------------------------------------------------------------|
| 15:0  | REGDATA  | R   | <p>Regular Conversion Data</p> <p>Conversion result of regular channel, read-only.</p> |
| 31:16 | Reserved |     |                                                                                        |

### 28.6.15 ADC oversampling control register (ADC\_OSAMPCTRL)

Offset address: 0x50

Reset value: 0x0000 0000



| 位/域  | 名称       | R/W | 描述                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | OSEN     | R/W | <p>Oversampling Enable</p> <p>This bit can be set or cleared via software.</p> <p>0: Disabled</p> <p>1: Enabled</p> <p>Note: Writing to this bit via software is only allowed when ADCEN=0 (ensure no conversions are in progress).</p>                                                                                                                                                                                                                                                |
| 3:1  | OSR      | R/W | <p>Oversampling Rate</p> <p>Define the oversampling rate.</p> <p>000: 2x</p> <p>001: 4x</p> <p>010: 8x</p> <p>011: 16x</p> <p>100: 32x</p> <p>101: 64x</p> <p>110: 128x</p> <p>111: 256x</p> <p>Note: Writing to this bit via software is only allowed when ADCEN=0 (ensure no conversions are in progress).</p>                                                                                                                                                                       |
| 7:4  | OSS      | R/W | <p>Oversampling Shift</p> <p>This bit can be set or cleared via software.</p> <p>0000: No shift</p> <p>0001: Shift by 1 bit</p> <p>0010: Shift by 2 bits</p> <p>0011: Shift by 3 bits</p> <p>0100: Shift by 4 bits</p> <p>0101: Shift by 5 bits</p> <p>0110: Shift by 6 bits</p> <p>0111: Shift by 7 bits</p> <p>1000: Shift by 8 bits</p> <p>Others: Reserved</p> <p>Note: Writing to this bit via software is only allowed when ADCEN=0 (ensure no conversions are in progress).</p> |
| 8    | TOS      | R/W | <p>Oversampling Trigger</p> <p>This bit can be set or cleared via software.</p> <p>0: Execute all conversions of the oversampling channel continuously after one trigger</p> <p>1: Requires a trigger for each conversion of the oversampling channel; number of triggers is determined by the oversampling rate (OSR)</p> <p>Note: Writing to this bit via software is only allowed when ADCEN=0 (ensure no conversions are in progress).</p>                                         |
| 31:9 | Reserved |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 28.6.16 ADC general-purpose state register (ADC\_CSTS)

Offset address: 0x00 (this offset address is only related to ADC1 base address+0x300)

Reset value: 0x0000 0000

| Field | Name       | R/W | Description                                     |
|-------|------------|-----|-------------------------------------------------|
| 0     | AWDFLG1    | R   | Analog Watchdog Flag of ADC1                    |
| 1     | EOCFLG1    | R   | End of Conversion Flag of ADC1                  |
| 2     | INJEOCFLG1 | R   | Injected Channel End of Conversion Flag of ADC1 |
| 3     | INJCSFLG1  | R   | Injected Channel Start Flag of ADC1             |
| 4     | REGCSFLG1  | R   | Regular Channel Start Flag of ADC1              |
| 5     | OVRFLG1    | R   | Overrun Flag of ADC1                            |
| 7:6   | Reserved   |     |                                                 |
| 8     | AWDFLG2    | R   | Analog Watchdog Flag of ADC2                    |
| 9     | EOCFLG2    | R   | End of Conversion Flag of ADC2                  |
| 10    | INJEOCFLG2 | R   | Injected Channel End of Conversion Flag of ADC2 |
| 11    | INJCSFLG2  | R   | Injected Channel Start Flag of ADC2             |
| 12    | REGCSFLG2  | R   | Regular Channel Start Flag of ADC2              |
| 13    | OVRFLG2    | R   | Overrun Flag of ADC2                            |
| 15:14 | Reserved   |     |                                                 |
| 16    | AWDFLG3    | R   | Analog Watchdog Flag of ADC3                    |
| 17    | EOCFLG3    | R   | End of Conversion Flag of ADC3                  |
| 18    | INJEOCFLG3 | R   | Injected Channel End of Conversion Flag of ADC3 |
| 19    | INJCSFLG3  | R   | Injected Channel Start Flag of ADC3             |
| 20    | REGCSFLG3  | R   | Regular Channel Start Flag of ADC3              |
| 21    | OVRFLG3    | R   | Overrun Flag of ADC3                            |
| 31:22 | Reserved   |     |                                                 |

### 28.6.17 ADC general-purpose control register (ADC\_CCTRL)

Offset address: 0x04 (this offset address is only related to ADC1 base address+0x300)

Reset value: 0x0000 0000

| Field | Name    | R/W | Description                                                                                                                                                                                                      |
|-------|---------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0   | ADCMSEL | R/W | ADC mode selection<br>All ADC are independent<br>00000: Independent mode<br>Dual mode: ADC1 and ADC2 work together, while ADC3 is independent<br>0001: Regular simultaneous+ injected simultaneous combined mode |

| Field | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |           |     | 00010: Regular simultaneous+ alternate trigger combined mode<br>00011: Reserved<br>00101: Only injected simultaneous mode<br>00110: Only regular simultaneous mode<br>00111: Only alternate mode<br>01001: Only alternate trigger mode<br>Triple mode: ADC1, ADC2 and ADC3 work together<br>10001: Regular simultaneous+ injected simultaneous combined mode<br>10010: Regular simultaneous+ alternate trigger combined mode<br>10011: Reserved<br>10101: Only injected simultaneous mode<br>10110: Only regular simultaneous mode<br>10111: Only alternate mode<br>11001: Only alternate trigger mode |
| 7:5   | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11:8  | SMPDEL2   | R/W | Delay Between 2 Sampling Phases<br>These bits are used in dual or triple alternate mode.<br>0000: $5 \cdot T_{ADCCCLK}$<br>0001: $6 \cdot T_{ADCCCLK}$<br>0010: $7 \cdot T_{ADCCCLK}$<br>...<br>1111: $20 \cdot T_{ADCCCLK}$                                                                                                                                                                                                                                                                                                                                                                           |
| 12    | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13    | DMADISSEL | R/W | DMA Disable Selection<br>0: No new DMA request will be issued after the last transmission<br>1: DMA request will be issued whenever data conversion occurs and DMAMODE=01, 10 or 11                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15:14 | DMAMODE   | R/W | DMA Mode<br>00: DMA mode is disabled<br>01: DMA mode 1 is enabled<br>10: DMA mode 2 is enabled<br>11: DMA mode 3 is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 17:16 | ADCPRE    | R/W | ADC Prescaler<br>00: PCLK2 2 divided frequency<br>01: PCLK2 4 divided frequency<br>10: PCLK2 6 divided frequency<br>11: PCLK2 8 divided frequency                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 21:18 | Reserved  |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 22    | VBATEN    | R/W | V <sub>BAT</sub> Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 23    | TSVREFEN  | R/W | Temperature Sensor and V <sub>REFINT</sub> Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

| Field | Name | R/W | Description |
|-------|------|-----|-------------|
| 31:24 |      |     | Reserved    |

### 28.6.18 Applicable to dual and triple mode general rule data registers (ADC\_CDATA)

Offset address: 0x08 (this offset address is only related to ADC1 base address+0x300)

Reset value: 0x0000 0000

| Field | Name  | R/W | Description                                                                                                                                                                       |
|-------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0  | DATA1 | R   | 1st Data Item of a Pair of Regular Conversions<br>In dual mode, these bits include regular data of ADC1<br>In triple mode, these bits include regular data of ADC1, ADC3 and ADC2 |
| 31:16 | DATA2 | R   | 2nd Data Item of a Pair of Regular Conversions<br>In dual mode, these bits include regular data of ADC2<br>In triple mode, these bits include regular data of ADC1, ADC3 and ADC2 |

## 29 Digital-to-analog Converter (DAC)

### 29.1 Full name and abbreviation description of terms

Table 150 Full Name and Abbreviation Description of DAC Terms

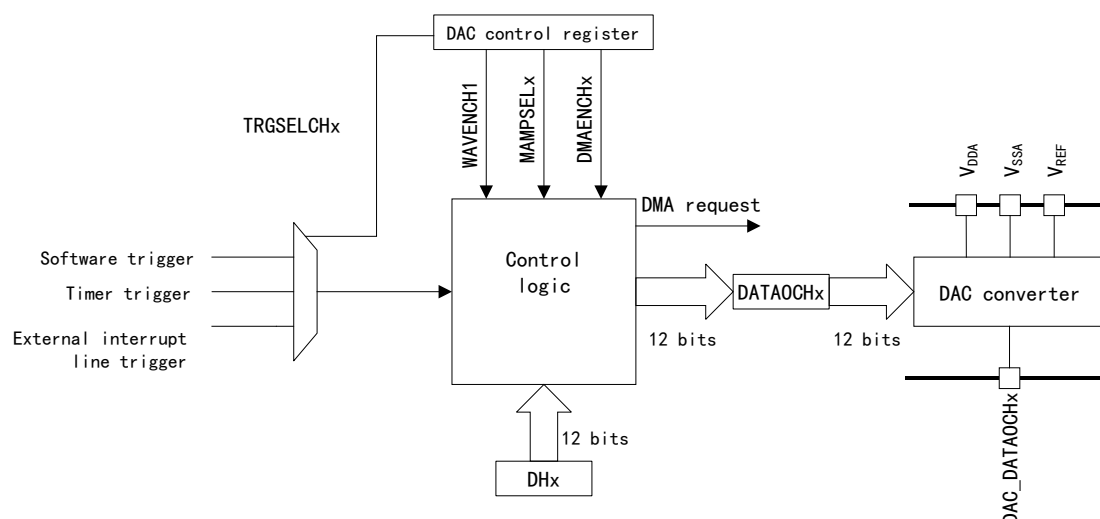
| Full name in English           | English abbreviation |
|--------------------------------|----------------------|
| Linear Feedback Shift Register | LFSR                 |

### 29.2 Introduction

DAC is a digital/analog converter that can be configured to input 8-bit or 12-bit data and output voltage. When 12-bit data is input, the data can be set to be left aligned or right aligned. It has two-way DAC output channels, which do not affect each other; each channel has multiple trigger sources to trigger conversion. A single channel can trigger conversion output, or both channels can trigger conversion output at the same time. Both channels can generate noise waveform and triangle waveform independently.

### 29.3 Structure block diagram

Figure 121 DAC Structure Block Diagram



### 29.4 Functional description

#### 29.4.1 DAC conversion and trigger source

DAC output can obtain corresponding voltage value by calculating the data in DAC\_DATAOCHx register. However, it is impossible to write data directly to DAC\_DATAOCHx register, and it is required to write to DAC\_DHx register and then through corresponding trigger, load the data in DAC\_DHx to

DAC\_DATAOCHx.

When the channel trigger is disabled (TRGENCHx bit in the register DAC\_CTRL is set to 0), write the value in DAC\_DHx register and it will be automatically transferred to DAC\_DATAOCHx after one APB1 clock cycle.

When the channel trigger is enabled (TRGENCHx bit in the register DAC\_CTRL is set to 1), write the value in DAC\_DHx register and it will be transferred to DAC\_DATAOCHx after different clock cycles according to the selected trigger source. Three types of trigger sources can be selected:

- Timer update event
- External interrupt trigger
- Software trigger

When the update event and external interrupt of the timer are selected as the trigger source, the transmission will be completed after three APB clock cycles; when software trigger is selected, the transmission will be completed after one APB1 clock cycle.

When transmitting the data to DAC\_DATAOCHx register, after a period of time, the digital data will be outputted after it is converted linearly into analog voltage. The intermediate conversion time will vary according to the power supply voltage and the analog output load.

#### 29.4.2 DAC reference voltage and output

DAC uses  $V_{REF}$  as reference voltage and by grounding the  $V_{SSA}$ , the output voltage range of DAC can be obtained, namely:  $0-V_{REF}$ .

DAC output calculation formula is:  $DAC\ output = V_{REF} * (DATAOCHx / 4095)$ .

#### 29.4.3 DAC data format

##### Single-channel DAC

The registers that are written in three modes are as follows:

- 8-bit data right aligned: DAC\_DH8Rx[7:0]
- 12-bit data left aligned: DAC\_DH12Lx[15:4]
- 12-bit data right aligned: DAC\_DH12Rx[11:0]

##### Double-channel DAC

The registers that are written in three modes are as follows:

- 8-bit data right aligned: DAC\_DH8RD[15:0]
- 12-bit data left aligned: DAC\_DH12LDUAL[15:4],  
DAC\_DH12LDUAL[31:20]
- 12-bit data right aligned: DAC\_DH12RDUAL[11:0],  
DAC\_DH12RDUAL[27:16]

#### 29.4.4 DAC waveform generation

Each channel of DAC can independently generate noise and triangle wave.

#### 29.4.5 DAC double-channel conversion

When two channels work at the same time, the written data can be written to the common registers: DH8RDUAL, DH12RDUAL and DH12LDUAL, so as to effectively use the bus bandwidth.

Dual-channel conversion can be divided into independent conversion and synchronous conversion. The specific configurations and descriptions are as follows.

##### 29.4.5.1 Independent trigger

###### Waveform generator disabled

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use different trigger sources.

###### Use the same LFSR

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use different trigger sources;
- (3) Enable the noise generation function of two channels, and set the same LFSR mask value.

###### Use different LFSR

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use different trigger sources;
- (3) Enable the noise generation function of two channels, and set different LFSR mask values.

###### Generate the same triangle wave

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use different trigger sources;
- (3) Enable the triangle wave generation function of two channels, and set the same triangular amplitude.

###### Generate different triangle wave

- (1) Enable two-channel trigger mode;

- (2) Configure two channels and use different trigger sources;
- (3) Enable the triangle wave generation function of two channels, and set different triangular amplitudes.

#### 29.4.5.2 Synchronous trigger

##### **Synchronous software startup**

Disable the trigger mode of two channels; after writing data, wait for one APB1 clock cycle and then transfer to DAC\_DATAOCH1 and DAC\_DATAOCH2 registers at the same time.

##### **Waveform generator disabled**

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use the same trigger source.

##### **Use the same LFSR**

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use the same trigger source;
- (3) Enable the noise generation function of two channels, and set the same LFSR mask value.

##### **Use different LFSR**

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use the same trigger source;
- (3) Enable the noise generation function of two channels, and set different LFSR mask values.

##### **Generate the same triangle wave**

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use the same trigger source;
- (3) Enable the triangle wave generation function of two channels, and set the same triangular amplitude.

##### **Use different triangle wave**

- (1) Enable two-channel trigger mode;
- (2) Configure two channels and use the same trigger source;



- (3) Enable the triangle wave generation function of two channels, and set different triangular amplitudes.

## 29.5 Register address mapping

Table 151 DAC Register Address Mapping

| Register name | Description                                              | Offset address |
|---------------|----------------------------------------------------------|----------------|
| DAC_CTRL      | DAC control register                                     | 0x00           |
| DAC_SWTRG     | DAC software Trigger Register                            | 0x04           |
| DAC_DH12R1    | DAC Channel 1 12-bit right-aligned data holding register | 0x08           |
| DAC_DH12L1    | DAC Channel 1 12-bit left-aligned data holding register  | 0x0C           |
| DAC_DH8R1     | DAC Channel 1 8-bit right-aligned data holding register  | 0x10           |
| DAC_DH12R2    | DAC Channel 2 12-bit right-aligned data holding register | 0x14           |
| DAC_DH12L2    | DAC Channel 2 12-bit left-aligned data holding register  | 0x18           |
| DAC_DH8R2     | DAC Channel 2 8-bit right-aligned data holding register  | 0x1C           |
| DAC_DH12RDUAL | Dual-DAC 12-bit right-aligned data holding register      | 0x20           |
| DAC_DH12LDUAL | Dual-DAC 12-bit left-aligned data holding register       | 0x24           |
| DAC_DH8RDUAL  | 8-bit right-aligned data holding register of double DAC  | 0x28           |
| DAC_DATAOCH1  | DAC Channel 1 data output register                       | 0x2C           |
| DAC_DATAOCH2  | DAC Channel 2 data output register                       | 0x30           |
| DAC_STS       | DAC state register                                       | 0x34           |

## 29.6 Register functional description

### 29.6.1 DAC control register (DAC\_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                    |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | ENCH1     | R/W | DAC Channel1 Enable<br>0: Disable<br>1: Enable                                                                                                 |
| 1     | BUFFDCH1  | R/W | DAC Channel1 Output Buffer Disable<br>0: Enable<br>1: Disable                                                                                  |
| 2     | TRGENCH1  | R/W | DAC Channel1 Trigger Enable<br>0: Disable<br>1: Enable                                                                                         |
| 5:3   | TRGSELCH1 | R/W | DAC Channel1 Trigger Source Select<br>The trigger source can be selected through this register when Channel 1 trigger is enabled (TRGENCH1=1). |

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |            |     | 000: TMR6 TRGO event<br>001: TMR8 TRGO event<br>010: TMR7 TRGO event<br>011: TMR5 TRGO event<br>100: TMR2 TRGO event<br>101: TMR4 TRGO event<br>110: External interrupt line 9<br>111: Software trigger                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:6   | WAVENCH1   | R/W | DAC Channel1 Noise/Triangle Wave Generation Enable<br>00: Waveform is not generated<br>01: Noise waveform is generated<br>1x: Triangle waveform is generated                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:8  | MAMPSELCH1 | R/W | Select DAC Channel1 LFSR Bit Mask/Triangle Wave Amplitude Selector<br>In the mode of "generating LFSR noise", select the bit to mask LFSR through this bit;<br>In the mode of "generating triangle wave", select the amplitude of triangle wave through this bit.<br>0000: Unmask LFSR bit 0/triangle wave amplitude is 1<br>0001: Unmask LFSR bit [1:0]/triangle wave amplitude is 3<br>0010: Unmask LFSR bit [2:0]/triangle wave amplitude is 7<br>0011: Unmask LFSR bit [3:0]/triangle wave amplitude is 15<br>0100: Unmask LFSR bit [4:0]/triangle wave amplitude is 31<br>0101: Unmask LFSR bit [5:0]/triangle wave amplitude is 63<br>0110: Unmask LFSR bit [6:0]/triangle wave amplitude is 127<br>0111: Unmask LFSR bit [7:0]/triangle wave amplitude is 255<br>1000: Unmask LFSR bit [8:0]/triangle wave amplitude is 511<br>1001: Unmask LFSR bit [9:0]/triangle wave amplitude is 1023<br>1010: Unmask LFSR bit [10:0]/triangle wave amplitude is 2047<br>≥1011: Unmask LFSR bit [11:0] / triangle wave amplitude is 4095 |
| 12    | DMAENCH1   | R/W | DAC Channel1 DMA Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 13    | DMAUDIEN1  | R/W | DAC Channel1 DMA Underrun Interrupt Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:14 | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 16    | ENCH2      | R/W | DAC Channel2 Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 17    | BUFFDCH2   | R/W | DAC Channel2 Output Buffer Disable<br>0: Enable<br>1: Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 18    | TRGENCH2   | R/W | DAC Channel2 Trigger Enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

| Field | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21:19 | TRGSELCH2  | R/W | <p>DAC Channel2 Trigger Source Select</p> <p>The trigger source can be selected through this register when Channel 2 trigger is enabled (TRGENCH2=1)</p> <p>000: TMR6 TRGO event<br/> 001: TMR8 TRGO event<br/> 010: TMR7 TRGO event<br/> 011: TMR5 TRGO event<br/> 100: TMR2 TRGO event<br/> 101: TMR4 TRGO event<br/> 110: External interrupt line 9<br/> 111: Software trigger</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 23:22 | WAVENCH2   | R/W | <p>DAC Channel2 Noise/Triangle Wave Generation Enable</p> <p>00: Waveform is not generated<br/> 01: Noise waveform is generated<br/> 1x: Triangle waveform is generated</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 27:24 | MAMPSELCH2 | R/W | <p>Select DAC Channel2 LFSR Bit Mask/Triangle Wave Amplitude Selector</p> <p>In the mode of "generating LFSR noise", select the bit to mask LFSR through this bit;<br/> In the mode of "generating triangle wave", select the amplitude of triangle wave through this bit.</p> <p>0000: Unmask LFSR bit 0/triangle wave amplitude is 1<br/> 0001: Unmask LFSR bit [1:0]/triangle wave amplitude is 3<br/> 0010: Unmask LFSR bit [2:0]/triangle wave amplitude is 7<br/> 0011: Unmask LFSR bit [3:0]/triangle wave amplitude is 15<br/> 0100: Unmask LFSR bit [4:0]/triangle wave amplitude is 31<br/> 0101: Unmask LFSR bit [5:0]/triangle wave amplitude is 63<br/> 0110: Unmask LFSR bit [6:0]/triangle wave amplitude is 127<br/> 0111: Unmask LFSR bit [7:0]/triangle wave amplitude is 255<br/> 1000: Unmask LFSR bit [8:0]/triangle wave amplitude is 511<br/> 1001: Unmask LFSR bit [9:0]/triangle wave amplitude is 1023<br/> 1010: Unmask LFSR bit [10:0]/triangle wave amplitude is 2047<br/> ≥1011: Unmask LFSR bit [11:0] / triangle wave amplitude is 4095</p> |
| 28    | DMAENCH2   | R/W | <p>DAC Channel2 DMA Enable</p> <p>0: Disable<br/> 1: Enable</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 29    | DMAUDIEN2  | R/W | <p>DAC Channel2 DMA Underrun Interrupt Enable</p> <p>0: Disable<br/> 1: Enable</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 31:30 | Reserved   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## 29.6.2 DAC software trigger register (DAC\_SWTRG)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                                                                                                                   |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | SWTRG1   | W   | DAC Channel1 Software Trigger Enable<br>This bit can be set to 1 and cleared by software; once the data in the register DAC_DH1 is transferred to the register DAC_DATAOCH1, this bit will be cleared by hardware.<br>0: Disable<br>1: Enable |
| 1     | SWTRG2   | W   | DAC Channel2 Software Trigger Enable<br>This bit can be set to 1 and cleared by software; once the data in the register DAC_DH2 is transferred to the register DAC_DATAOCH2, this bit will be cleared by hardware.<br>0: Disable<br>1: Enable |
| 31:2  | Reserved |     |                                                                                                                                                                                                                                               |

### 29.6.3 DAC Channel 1 12-bit right-aligned data holding register (DAC\_DH12R1)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                   |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 11:0  | DATA     | R/W | DAC Channel1 12-bit Right-Aligned Data<br>This bit is written by the software, representing the data of 12-bit DAC channel 1. |
| 31:12 | Reserved |     |                                                                                                                               |

### 29.6.4 DAC Channel 1 12-bit left-aligned data holding register (DAC\_DH12L1)

Offset address: 0x0C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 3:0   | Reserved |     |                                       |
| 15:4  | DATA     | R/W | DAC Channel1 12-Bit Left-Aligned Data |
| 31:16 | Reserved |     |                                       |

### 29.6.5 DAC Channel 1 8-bit right-aligned data holding register (DAC\_DH8R1)

Offset address: 0x10

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 7:0   | DATA     | R/W | DAC Channel1 8-bit Right-Aligned Data |
| 31:8  | Reserved |     |                                       |

### 29.6.6 DAC Channel 2 12-bit right-aligned data holding register (DAC\_DH12R2)

Offset address: 0x14

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                            |
|-------|----------|-----|----------------------------------------|
| 11:0  | DATA     | R/W | DAC Channel2 12-bit Right-Aligned Data |
| 31:12 | Reserved |     |                                        |

### 29.6.7 DAC Channel 2 12-bit left-aligned data holding register (DAC\_DH12L2)

Offset address: 0x18

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 3:0   | Reserved |     |                                       |
| 15:4  | DATA     | R/W | DAC Channel2 12-Bit Left-Aligned Data |
| 31:16 | Reserved |     |                                       |

### 29.6.8 DAC Channel 2 8-bit right-aligned data holding register (DAC\_DH8R2)

Offset address: 0x1C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 7:0   | DATA     | R/W | DAC Channel2 8-bit Right-Aligned Data |
| 31:8  | Reserved |     |                                       |

### 29.6.9 Dual-DAC 12-bit right-aligned data holding register (DAC\_DH12RDUAL)

Offset address: 0x20

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                            |
|-------|----------|-----|----------------------------------------|
| 11:0  | DATAACH1 | R/W | DAC Channel1 12-bit Right-Aligned Data |
| 15:12 | Reserved |     |                                        |
| 27:16 | DATAACH2 | R/W | DAC Channel2 12-bit Right-Aligned Data |
| 31:28 | Reserved |     |                                        |

### 29.6.10 Dual-DAC 12-bit left-aligned data holding register (DAC\_DH12LDUAL)

Offset address: 0x24

Reset value: 0x0000 0000

| Field | Name     | R/W | Description |
|-------|----------|-----|-------------|
| 3:0   | Reserved |     |             |

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 15:4  | DATACH1  | R/W | DAC Channel1 12-Bit Left-Aligned Data |
| 19:16 | Reserved |     |                                       |
| 31:20 | DATACH2  | R/W | DAC Channel2 12-Bit Left-Aligned Data |

#### 29.6.11 Dual-DAC 8-bit right-aligned data holding register (DAC\_DH8RDUAL)

Offset address: 0x28

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 7:0   | DATACH1  | R/W | DAC Channel1 8-bit Right-Aligned Data |
| 15:8  | DATACH2  | R/W | DAC Channel2 8-bit Right-Aligned Data |
| 31:16 | Reserved |     |                                       |

#### 29.6.12 DAC Channel 1 data output register (DAC\_DATAOCH1)

Offset address: 0x2C

Reset value: 0x0000 0000

| Field | Name     | R/W | Description              |
|-------|----------|-----|--------------------------|
| 11:0  | DATA     | R   | DAC Channel1 Data Output |
| 31:12 | Reserved |     |                          |

#### 29.6.13 DAC Channel 2 data output register (DAC\_DATAOCH2)

Offset address: 0x30

Reset value: 0x0000 0000

| Field | Name     | R/W | Description              |
|-------|----------|-----|--------------------------|
| 11:0  | DATA     | R   | DAC Channel2 Data Output |
| 31:12 | Reserved |     |                          |

#### 29.6.14 DAC state register (DAC\_STS)

Offset address: 0x34

Reset value: 0x0000 0000

| Field | Name      | R/W   | Description                                                   |
|-------|-----------|-------|---------------------------------------------------------------|
| 12:0  | Reserved  |       |                                                               |
| 13    | DMAUDFLG1 | RC_W1 | DAC Channel1 DMA Underrun Flag<br>0: Not occur<br>1: Occurred |
| 28:14 | Reserved  |       |                                                               |
| 29    | DMAUDFLG2 | RC_W1 | DAC Channel2 DMA Underrun Flag<br>0: Not occur<br>1: Occurred |
| 31:30 | Reserved  |       |                                                               |

## 30 Random Number Generator (RNG)

### 30.1 Introduction

RNG is a random number generator, which provides a 32-bit random number in the master reading based on continuous analog noise.

### 30.2 Main characteristics

- (1) Provide 32-bit random number generated by the analog generator
- (2) The interval between two consecutive random numbers is 40 PLLCLK48 clock signal cycles
- (3) Monitor RNG entropy to mark abnormal behaviors
- (4) Disabling RNG can reduce the power consumption

### 30.3 Functional description

The random number generator is achieved by analog circuit. This circuit provides seeds for the linear feedback shift register to generate 32-bit random numbers.

Multiple ring oscillators form an analog circuit, and the seeds are generated by XOR operation through the frequency output by the oscillator. PLLCLK48 is dedicated clock of RNG\_LFSR, and it provides clock information for it at a constant frequency, so the quality of random numbers has nothing to do with the frequency of HCLK. After RNG\_LFSR introduces a large number of seeds, the content will be transferred to RNG\_DATA register. Meanwhile, the system will monitor the seeds and PLLCLK48. The status bit in RNG\_STS register indicates the time when an abnormal sequence occurs on the seed or the PLLCLK48 clock frequency is too low. An interrupt will be generated when an error is detected.

#### 30.3.1 Enable RNG

The setting sequence of enabling RNG is as follows:

- (1) Enable interrupt and an interrupt will be generated when the random number is ready or an error occurs.
- (2) A random number will be generated when RNG\_CTRL[RNGEN]=1. At this time, the analog part, RNG\_LFSR and error detector will be activated.

- (3) At the time of each interrupt, when CLKERINT bit and FSINT bit of RNG\_STS register are set to 0 and DATARDY=1, RNG\_DATA register can be read.

Do not use the first random number generated after RNGEN bit is set, and it should be saved for comparison with the next random number. Each random number needs to be compared with the previous random number. If any pair is equal, it means that the continuous random number generator test fails.

### 30.3.2 Error state

#### 30.3.2.1 Clock error

When a clock error occurs because the PLLCLK48 clock is incorrect, RNG cannot generate random numbers again. Check whether the clock controller is configured correctly to provide RNG clock and clear CLKERINT bit. RNG can work normally when CLKERCSTS=0. The clock error does not affect the last random number, so the random number in RNG\_DATA register can be used.

#### 30.3.2.2 Seed error

In case of a seed error, the interrupt random number will be generated as long as FSCSTS=1. Since the entropy may be insufficient, if there are already data in RNG\_DATA register, the generated interrupt random number cannot be used.

RNGEN bit shall be set after FSINT bit is cleared to reinitialize and restart RNG.

## 30.4 Register address mapping

Table 152 RNG Register Address Mapping

| Register name | Description          | Offset address |
|---------------|----------------------|----------------|
| RNG_CTRL      | RNG control register | 0x00           |
| RNG_STS       | RNG state register   | 0x04           |
| RNG_DATA      | RNG data register    | 0x08           |

## 30.5 Register functional description

### 30.5.1 RNG control register (RNG\_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                           |
|-------|----------|-----|---------------------------------------|
| 1:0   | Reserved |     |                                       |
| 2     | RNGEN    | R/W | RNG Enable<br>0: Disable<br>1: Enable |



| Field | Name     | R/W | Description                                                                                                                                                    |
|-------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3     | INTEN    | R/W | Interrupt Enable<br>0: Disable<br>1: Enable; when any of DATARDY bit, CLKERINT bit and FSINT bit in RNG_STS register is set to 1, an interrupt will be pending |
| 31:4  | Reserved |     |                                                                                                                                                                |

### 30.5.2 RNG state register (RNG\_STS)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name      | R/W   | Description                                                                                                                                                                                                                                                                                                        |
|-------|-----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | DATARDY   | R     | Data Ready<br>0: RNG_ Data register is not ready, and the random data is not available<br>1: RNG_ Data register is ready, and the random data is available<br>An interrupt will be pending when INTEN=1. After reading RNG_DATA register, this bit will be cleared to zero until a new valid value is figured out. |
| 1     | CLKERCSTS | R     | RNGCLK Error Current Status<br>0: PLLCLK48 clock is detected. If CLKERINT bit is set to 1, it means that clock error has been detected and recovered to normal.<br>1: PLLCLK48 clock is not detected                                                                                                               |
| 2     | FSCSTS    | R     | Faulty Sequence Current Status<br>0: Sequence error is not detected. If FSINT bit is set to 1, it means that faulty sequence has been detected and recovered to normal.<br>1: More than 64 0/1 or more than 32 alternate 0 and 1 are detected                                                                      |
| 4:3   | Reserved  |       |                                                                                                                                                                                                                                                                                                                    |
| 5     | CLKERINT  | RC_W0 | RNGCLK Error Interrupt Status<br>0: PLLCLK48 clock is detected<br>1: PLLCLK48 clock is not detected<br>This bit can be set at the same time with CLKERCSTS bit and be cleared by writing 0. An interrupt will be pending when INTEN=1.                                                                             |
| 6     | FSINT     | RC_W0 | Faulty Sequence Interrupt Status<br>0: Faulty sequence is not detected.<br>1: More than 64 0/1 or more than 32 alternate 0 and 1 are detected<br>This bit can be set at the same time with FSCSTS bit and be cleared by writing 0. An interrupt will be pending when INTEN=1.                                      |
| 31:7  | Reserved  |       |                                                                                                                                                                                                                                                                                                                    |

### 30.5.3 RNG data register (RNG\_DATA)

Offset address: 0x08

Reset value: 0x0000 0000

This register is read-only and provides 32-bit random number when reading.

This register can be read only when DATARDY bit is set to 1. After reading, this register will provide new random number within 40 PLLCLK48 clock cycles.

| Field | Name | R/W | Description                        |
|-------|------|-----|------------------------------------|
| 31:0  | DATA | R   | Random Data<br>32-bit data number. |

## 31 Cyclic Redundancy Check (CRC)

### 31.1 Introduction

The cyclic redundancy check (CRC) computing unit can get 32-bit CRC computing result by calculating the input data through a fixed generator polynomial, which is mainly used to detect or verify the correctness and integrity of the data after transmission or storage.

### 31.2 Functional description

#### 31.2.1 Calculation method

Use CRC-32 (Ethernet) polynomial: 0x4C11DB7

$$(X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1)$$

#### 31.2.2 Calculation time

The calculation time is four AHB clock cycles.

Every time a new data is written, the result will be a combination of the last calculation result and the new calculation result. (Execute operation for the whole word). Write operation of CPU will be suspended during calculation, so that "Back-to-back" write or continuous "read" -"write" operation can be performed for the register CRC\_DATA.

### 31.3 Register address mapping

Table 153 CRC Register Address Mapping

| Register name | Description               | Offset address |
|---------------|---------------------------|----------------|
| CRC_DATA      | Data register             | 0x00           |
| CRC_INDATA    | Independent data register | 0x04           |
| CRC_CTRL      | Control register          | 0x08           |

### 31.4 Register functional description

#### 31.4.1 Data register (CRC\_DATA)

Offset address: 0x00

Reset value: 0xFFFF FFFF

| Field | Name | R/W | Description                                                                                                                                                           |
|-------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0  | DATA | R/W | 32-bit Data<br>As the input register: Store the new data of CRC calculator when writing.<br>As the output register: Return the results of CRC computing when reading. |

### 31.4.2 Independent data register (CRC\_INDATA)

Offset address: 0x04

Reset value: 0x0000 0000

| Field | Name      | R/W | Description                                                                                                                                                           |
|-------|-----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0   | INDATA    | R/W | Independent 8-bit Data<br>Can be used for temporary storage of 1-byte data.<br>CRC rest generated by RST bit of the register CRC_CTRL has no effect on this register. |
| 31:8  | Reserved. |     |                                                                                                                                                                       |

Note: This register does not take part in calculation and can store any data.

### 31.4.3 Control register (CRC\_CTRL)

Offset address: 0x08

Reset value: 0x0000 0000

| Field | Name     | R/W | Description                                                                                                                                     |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | RST      | W   | Reset CRC Calculation Unit<br>Set CRC_DATA register to 0xFFFF FFFF. It can only set this bit, which shall be automatically cleared by hardware. |
| 31:1  | Reserved |     |                                                                                                                                                 |

## 32 Chip Electronic Signature

### 32.1 Introduction

The chip electronic signature is used to match the firmware or external device.

### 32.2 Register functional description

#### 32.2.1 96-bit unique chip ID of unique device

Base address: 0x1FFF 7A10

Offset address: 0x00

| Field | Name       | R/W | Description                   |
|-------|------------|-----|-------------------------------|
| 31:0  | U_ID[31:0] | R   | Unique identity flag 31:0 bit |

Offset address: 0x04

Read-only, the value has been prepared before leaving the factory

| Field | Name        | R/W | Description                     |
|-------|-------------|-----|---------------------------------|
| 31:0  | U_ID[63:32] | R   | Unique identity flag 63:32 bits |

Offset address: 0x08

Read-only, the value has been prepared before leaving the factory

| Field | Name        | R/W | Description                     |
|-------|-------------|-----|---------------------------------|
| 31:0  | U_ID[95:64] | R   | Unique identity flag 95:64 bits |

#### 32.2.2 Flash memory capacity register

Base address: 0x1FFF 7A22

Offset address: 0x00

| Field | Name   | R/W | Description                                                                                                              |
|-------|--------|-----|--------------------------------------------------------------------------------------------------------------------------|
| 15:0  | F_SIZE | R   | Flash Memory Capacity<br>Indicate the capacity of main memory area of the product (in KB).<br>For example: 0x0400=1024KB |

## 33 Revision History

Table 154 Document Version History

| Date      | Version | Change History |
|-----------|---------|----------------|
| July 2025 | 1.0     | New            |

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